Infineon Technologies - MB91F522KSCPMC-GSK5E2 Datasheet

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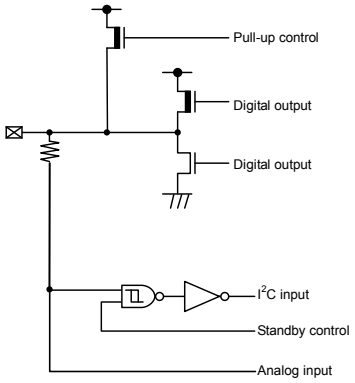
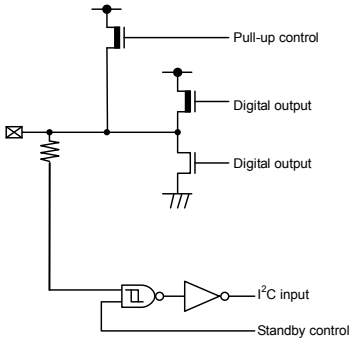
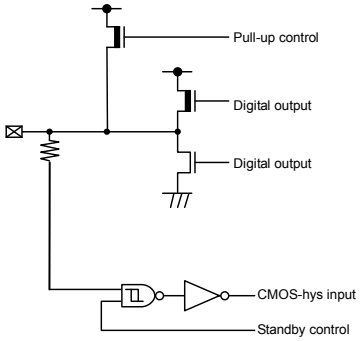
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522kscpmc-gsk5e2

- Power-on reset
- Low-voltage detection reset (independently monitor the external power supply and the internal power supply)
  - The external power supply can select initial value ON/OFF by the part number.
- Device Package : 176/144/120/100/80/64
- CMOS 90nm Technology
- Power supplies
  - 5V Power supply
  - The internal 1.2V is generated from 5V with the voltage step-down circuit

Type	Circuit	Remarks
D		•I2C Analog input, General-purpose I/O port •Output 3mA •Pull-up resistor control 50kΩ •I2C hysteresis input
E		•I2C,General-purpose I/O port •Output 3mA •Pull-up resistor control 50kΩ •I2C hysteresis input
F		•General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •CMOS hysteresis input

- Notes When Writing Data in a Register Having the Status Flag
  When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

  The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

  Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

  Note: These points can be ignored because the bit instructions are already taken the points into consideration.

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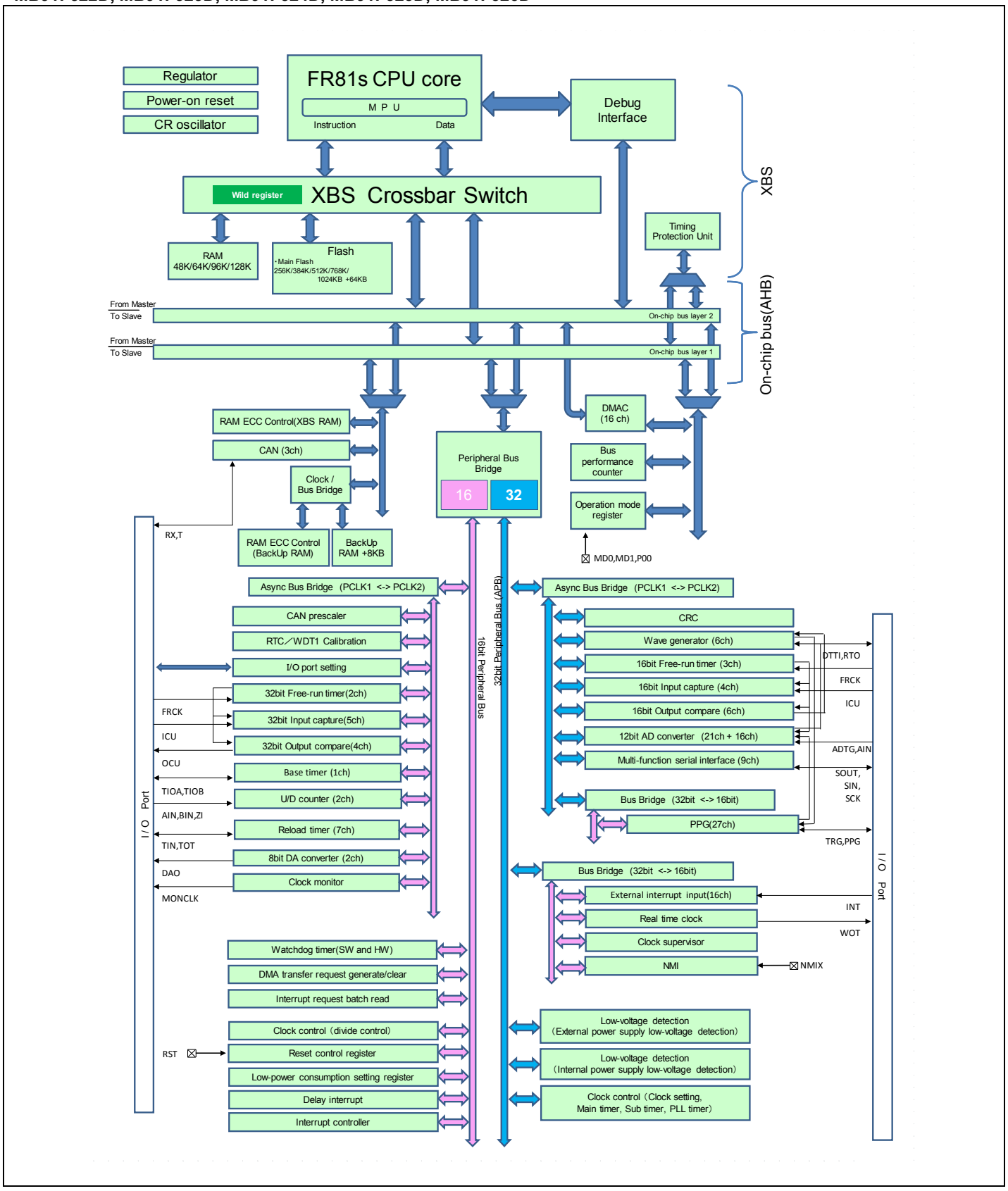


Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00059C$_H$ to 0005BC$_H$	—	—	—	—	Reserved
0005C0$_H$ to 0005FC$_H$	—	—	—	—	Reserved
000600$_H$	ASR0 [R/W] W 00000000 00000000 -------- 1111-001				External Bus Interface [S]
000604$_H$	ASR1 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608$_H$	ASR2 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
00060C$_H$	ASR3 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610$_H$ to 00063C$_H$	—	—	—	—	Reserved [S]
000640$_H$	ACR0 [R/W] W -------- -------- -------- 01--00--				External Bus Interface [S]
000644$_H$	ACR1 [R/W] W -------- -------- -------- XX--XX--				
000648$_H$	ACR2 [R/W] W -------- -------- -------- XX--XX--				
00064C$_H$	ACR3 [R/W] W -------- -------- -------- XX--XX--				
000650$_H$ to 00067C$_H$	—	—	—	—	Reserved [S]
000680$_H$	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External Bus Interface [S]
000684$_H$	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688$_H$	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				External Bus Interface [S]
00068C$_H$	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690$_H$ to 0006FC$_H$	—	—	—	—	Reserved [S]
000700$_H$ to 00070C$_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001200_H	TCGS [R/W] B,H,W ------00	—	—	TCGSE [R/W] B,H,W -----000	16-bit Free-run timer synchronous activation
001204_H	CPCLRB0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 0
001208_H	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00120C_H$	CPCLRB1/CPCLR1 [W] H,W 11111111 11111111		TCDT1 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 1
001210_H	TCCS1 [R/W] B,H,W 00000000 01000000 ----0000 --------				
001214_H	CPCLRB2/CPCLR2 [W] H,W 11111111 11111111		TCDT2 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 2
001218_H	TCCS2 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00121C_H$ to 001230_H	—	—	—	—	Reserved
001234_H	FRS0 [R/W] B,H,W -------- --00--00 --00--00 --00--00				16-bit Free-run timer selection
001238_H	—		FRS1 [R/W] B,H,W --00--00 --00--00		
$00123C_H$	FRS2 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001240_H	FRS3 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001244_H	FRS4 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001248_H	—	—	—	—	Reserved
$00124C_H$	OCCPB0/OCCP0 [R/W] H,W 00000000 00000000		OCCPB1/OCCP1 [R/W] H,W 00000000 00000000		16-bit Output compare 0/1
001250_H	OCS01 [R/W] B,H,W -110--00 00001100		—	OCMOD01 [R/W] B,H,W ------00	
001254_H	OCCPB2/OCCP2 [R/W] H,W 00000000 00000000		OCCPB3/OCCP3 [R/W] H,W 00000000 00000000		16-bit Output compare 2/3
001258_H	OCS23 [R/W] B,H,W -110--00 00001100		—	OCMOD23 [R/W] B,H,W ------00	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00147C$_H$	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000		12-bit A/D converter 2/2 unit
001480$_H$	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		
001484$_H$	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000		
001488$_H$	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000		
00148C$_H$	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000		
001490$_H$	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000		
001494$_H$	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000		
001498$_H$ to 0014B4$_H$	—	—	—	—	Reserved
0014B8$_H$	ADTCS32[R/W] B,H,W 00000000 0010----		ADTCS33[R/W] B,H,W 00000000 0010----		12-bit A/D converter 2/2 unit
0014BC$_H$	ADTCS34[R/W] B,H,W 00000000 0010----		ADTCS35[R/W] B,H,W 00000000 0010----		
0014C0$_H$	ADTCS36[R/W] B,H,W 00000000 0010----		ADTCS37[R/W] B,H,W 00000000 0010----		
0014C4$_H$	ADTCS38[R/W] B,H,W 00000000 0010----		ADTCS39[R/W] B,H,W 00000000 0010----		
0014C8$_H$	ADTCS40[R/W] B,H,W 00000000 0010----		ADTCS41[R/W] B,H,W 00000000 0010----		
0014CC$_H$	ADTCS42[R/W] B,H,W 00000000 0010----		ADTCS43[R/W] B,H,W 00000000 0010----		
0014D0$_H$	ADTCS44[R/W] B,H,W 00000000 0010----		ADTCS45[R/W] B,H,W 00000000 0010----		
0014D4$_H$	ADTCS46[R/W] B,H,W 00000000 0010----		ADTCS47[R/W] B,H,W 00000000 0010----		
0014D8$_H$ to 0014F4$_H$	—	—	—	—	Reserved
0014F8$_H$	ADTCD32[R] B,H,W 10--0000 00000000		ADTCD33[R] B,H,W 10--0000 00000000		12-bit A/D converter 2/2 unit
0014FC$_H$	ADTCD34[R] B,H,W 10--0000 00000000		ADTCD35[R] B,H,W 10--0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002254_H	IF2DTB12 [R/W] B,H,W 00000000 00000000		IF2DTB22 [R/W] B,H,W 00000000 00000000		CAN2 (64msb)
002258_H	—	—	—	—	
$00225C_H$	—	—	—	—	
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H to $00227C_H$	—				
002280_H	TREQR22 [R] B,H,W 00000000 00000000		TREQR12 [R] B,H,W 00000000 00000000		
002284_H	TREQR42 [R] B,H,W 00000000 00000000		TREQR32 [R] B,H,W 00000000 00000000		
002288_H	—	—	—	—	
$00228C_H$	—	—	—	—	
002290_H	NEWDT22 [R] B,H,W 00000000 00000000		NEWDT12 [R] B,H,W 00000000 00000000		
002294_H	NEWDT42 [R] B,H,W 00000000 00000000		NEWDT32 [R] B,H,W 00000000 00000000		
002298_H	—	—	—	—	
$00229C_H$	—	—	—	—	
$0022A0_H$	INTPND22 [R] B,H,W 00000000 00000000		INTPND12 [R] B,H,W 00000000 00000000		
$0022A4_H$	INTPND42 [R] B,H,W 00000000 00000000		INTPND32 [R] B,H,W 00000000 00000000		
$0022A8_H$	—	—	—	—	
$0022AC_H$	—	—	—	—	
$0022B0_H$	MSGVAL22 [R] B,H,W 00000000 00000000		MSGVAL12 [R] B,H,W 00000000 00000000		
$0022B4_H$	MSGVAL42 [R] B,H,W 00000000 00000000		MSGVAL32 [R] B,H,W 00000000 00000000		
$0022B8_H$	—	—	—	—	
$0022BC_H$	—	—	—	—	
$0022C0_H$ to $0022FC_H$	—				

11. Electrical Characteristics

Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage *1,*2		V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog power supply voltage *1,*2		AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC} ≤ V_{CC}
Analog reference voltage *1		AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC}
Input voltage *1		V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage *1		V_{IA5}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage *1		V_o	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current		I_{CLAMP}	-	4.0	mA	*6
Total maximum clamp current		$\Sigma\|I_{CLAMP}\|$	-	20	mA	*6
"L" level maximum output current *3		I_{OL1}	-	15	mA	
		I_{OL2}	-	30	mA	
"L" level average output current *4		I_{OLAV1}	-	4	mA	*9
		I_{OLAV2}	-	12	mA	*10
"L" level total output current *5		ΣI_{OL1}	-	100	mA	
		ΣI_{OL2}	-	120	mA	
"H" level maximum output current*3		I_{OH1}	-	-15	mA	
		I_{OH2}	-	-30	mA	
"H" level average output current*4		I_{OHAV1}	-	-4	mA	*9
		I_{OHAV2}	-	-12	mA	*10
"H" level total output current *5		ΣI_{OH1}	-	-100	mA	
		ΣI_{OH2}	-	-120	mA	
Power consumption	T_A: -40°C to +105°C	P_D	-	882	mW	*8
	T_A: -40°C to +125°C		-	675	mW	*8
Operating temperature		T_A	-40	+105	°C	
			-40	+125	°C	*7
Storage temperature		Tstg	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0V

*2: Caution must be taken that AV_{CC}, AVRH do not exceed V_{CC} upon power-on and under other circumstances.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6:
- Corresponding pins: all general-purpose ports except P035, 041, 093, 122.
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*7: When it is used under this condition, contact your sales representative.

(T_A: -40°C to +125°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	102	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	115	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	115	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	92	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	105	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	105	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	82	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	95	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	95	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	82	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	72	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation , Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

AC Characteristics

(1) Main Clock Timing

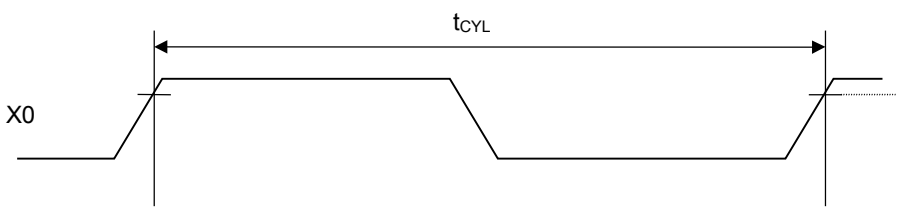
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS} =AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1		-	4	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency*1	F_{CP}	-		2	-	80	MHz	CPU clock
	F_{CPP}			1		40		Peripheral bus clock
	F_{CPT}			1		40		External bus clock (When V_{CC}=5.0V is used) *2
				1		32		External bus clock (When V_{CC}=3.3V is used)
Internal operating clock cycle time*1	t_{CP}	-	-	12.5	-	500	ns	CPU clock
	t_{CPP}			25		1000		Peripheral bus clock
	t_{CPT}			25		1000		External bus clock (When V_{CC}=5.0V is used)
				31.25		1000		External bus clock (When V_{CC}=3.3V is used)
CAN PLL jitter (during lock)	t_{PJ}	-		-10	-	10	ns	F_{CP}=80MHz (4MHz□Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	-		50	100	150	kHz	

*1: The maximum / minimum value is defined when using the main clock and PLL clock.

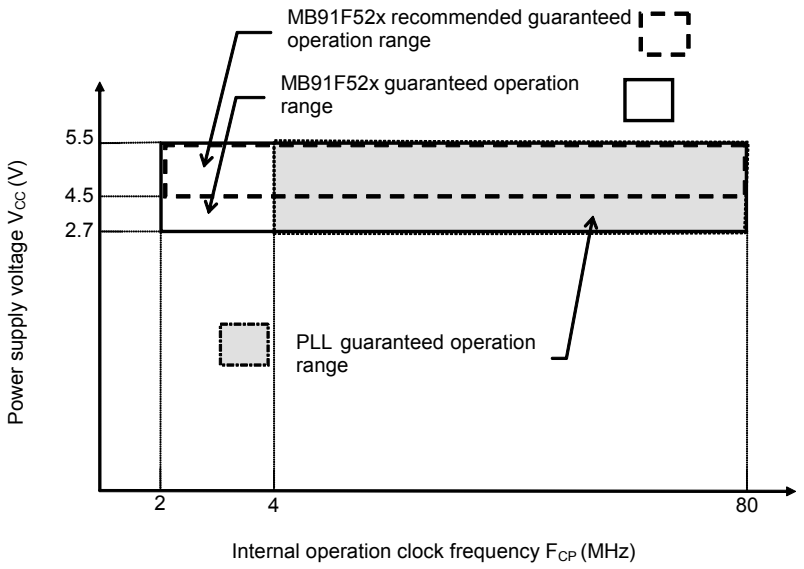
*2: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

• X0,X1 clock timing



- Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage



Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2 , SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS↑→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↓ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

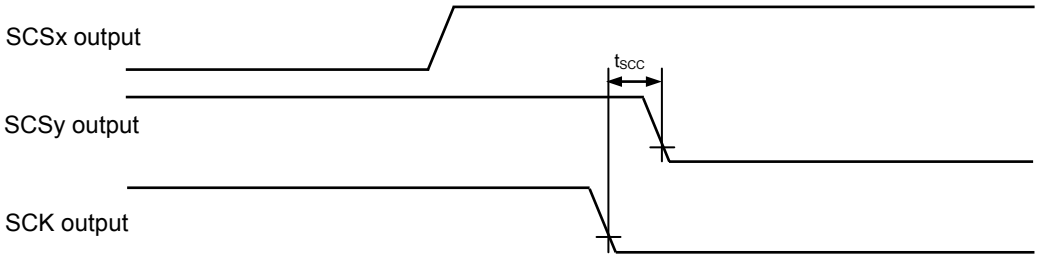
*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3.



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

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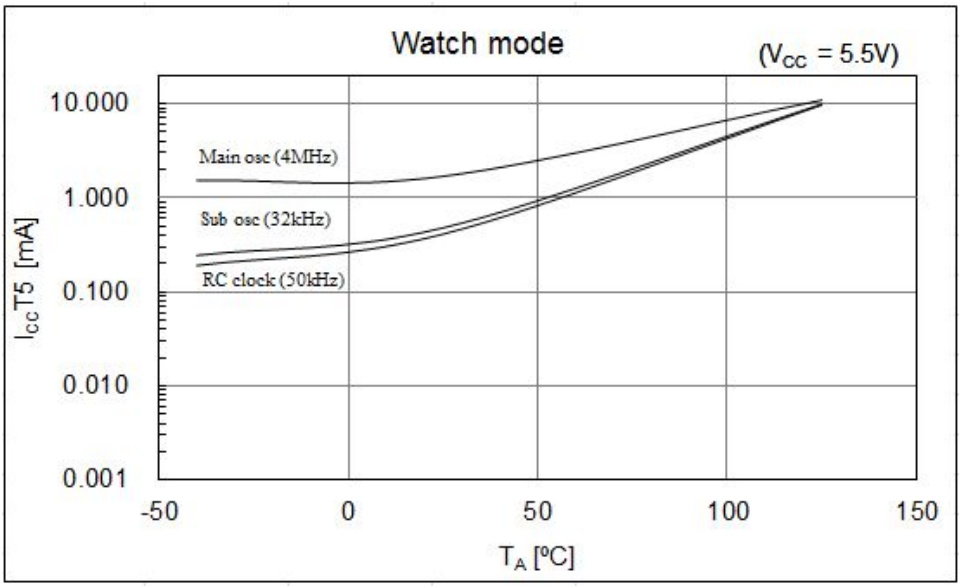
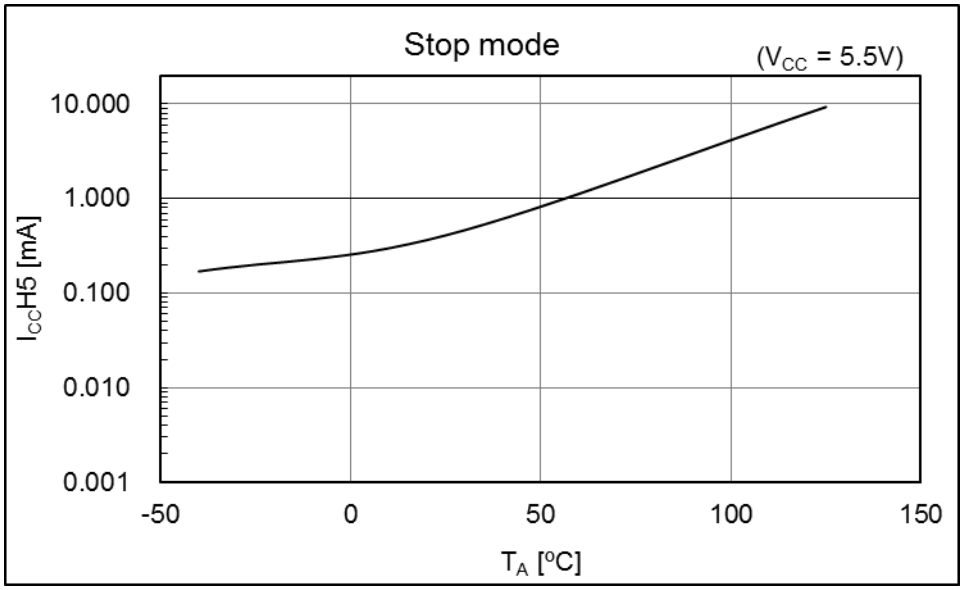

Watch mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC}T5 [mA]
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
-50
0
50
100
150
T_A [°C]


Stop mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC}H5 [mA]
-50
0
50
100
150
T_A [°C]

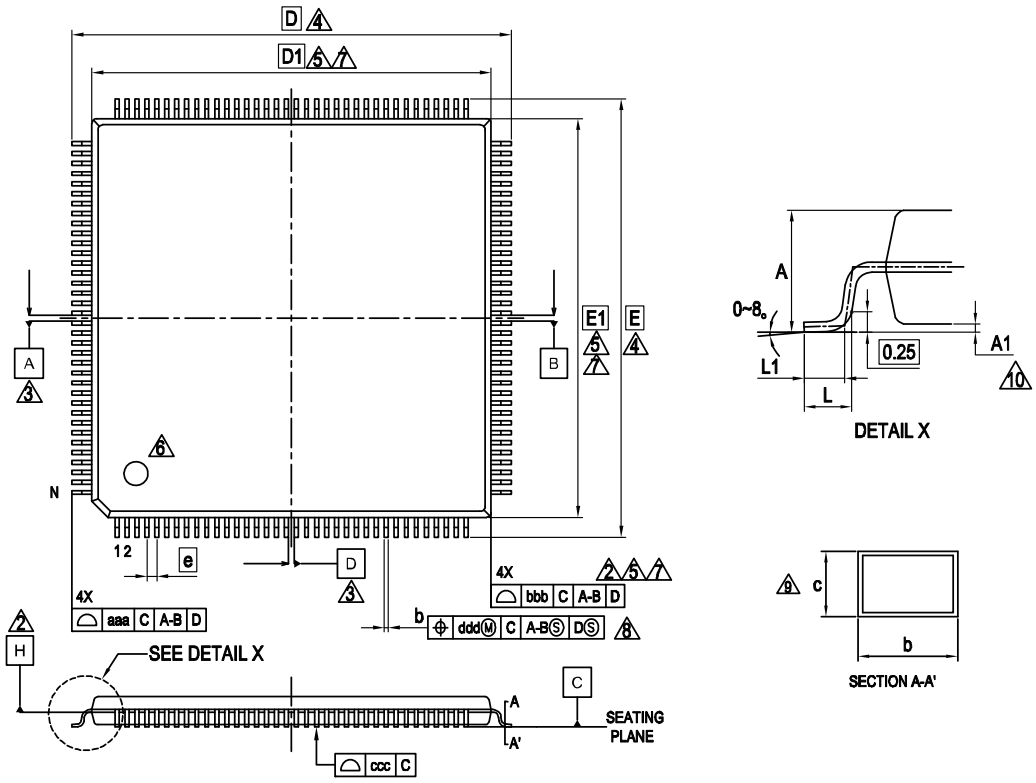
14. Ordering Information MB91F52xxxC[*1]

Part number	Sub clock	CSV Initial value	LVD Initial value	Package[*2]
MB91F526LWCPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LYCPMC			OFF	
MB91F526LJCPMC		OFF	ON	
MB91F526LLCPMC			OFF	
MB91F525LWCPMC		ON	ON	
MB91F525LYCPMC			OFF	
MB91F525LJCPMC		OFF	ON	
MB91F525LLCPMC			OFF	
MB91F524LWCPMC		ON	ON	
MB91F524LYCPMC			OFF	
MB91F524LJCPMC		OFF	ON	
MB91F524LLCPMC			OFF	
MB91F523LWCPMC		ON	ON	
MB91F523LYCPMC			OFF	
MB91F523LJCPMC		OFF	ON	
MB91F523LLCPMC			OFF	
MB91F522LWCPMC		ON	ON	
MB91F522LYCPMC			OFF	
MB91F522LJCPMC		OFF	ON	
MB91F522LLCPMC			OFF	
MB91F526LSCPMC	None	ON	ON	
MB91F526LUCPMC			OFF	
MB91F526LHCPMC		OFF	ON	
MB91F526LKCPMC			OFF	
MB91F525LSCPMC		ON	ON	
MB91F525LUCPMC			OFF	
MB91F525LHCPMC		OFF	ON	
MB91F525LKCPMC			OFF	
MB91F524LSCPMC		ON	ON	
MB91F524LUCPMC			OFF	
MB91F524LHCPMC		OFF	ON	
MB91F524LKCPMC			OFF	
MB91F523LSCPMC		ON	ON	
MB91F523LUCPMC			OFF	
MB91F523LHCPMC		OFF	ON	
MB91F523LKCPMC			OFF	
MB91F522LSCPMC		ON	ON	
MB91F522LUCPMC			OFF	
MB91F522LHCPMC		OFF	ON	
MB91F522LKCPMC			OFF	

15. Ordering Information MB91F52xxxD

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWDPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LJDPMC		OFF	ON	
MB91F525LWDPMC		ON	ON	
MB91F525LJDPMC		OFF	ON	
MB91F524LWDPMC		ON	ON	
MB91F524LJDPMC		OFF	ON	
MB91F523LWDPMC		ON	ON	
MB91F523LJDPMC		OFF	ON	
MB91F522LWDPMC		ON	ON	
MB91F522LJDPMC		OFF	ON	
MB91F526LSDPMC	None	ON	ON	
MB91F526LHDPMC		OFF	ON	
MB91F525LSDPMC		ON	ON	
MB91F525LHDPMC		OFF	ON	
MB91F524LSDPMC		ON	ON	
MB91F524LHDPMC		OFF	ON	
MB91F523LSDPMC		ON	ON	
MB91F523LHDPMC		OFF	ON	
MB91F522LSDPMC		ON	ON	
MB91F522LHDPMC		OFF	ON	
MB91F526KWDPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJDPMC		OFF	ON	
MB91F525KWDPMC		ON	ON	
MB91F525KJDPMC		OFF	ON	
MB91F524KWDPMC		ON	ON	
MB91F524KJDPMC		OFF	ON	
MB91F523KWDPMC		ON	ON	
MB91F523KJDPMC		OFF	ON	
MB91F522KWDPMC		ON	ON	
MB91F522KJDPMC		OFF	ON	
MB91F526KSDPMC	None	ON	ON	
MB91F526KHDPMC		OFF	ON	
MB91F525KSDPMC		ON	ON	
MB91F525KHDPMC		OFF	ON	
MB91F524KSDPMC		ON	ON	
MB91F524KHDPMC		OFF	ON	
MB91F523KSDPMC		ON	ON	
MB91F523KHDPMC		OFF	ON	
MB91F522KSDPMC		ON	ON	
MB91F522KHDPMC		OFF	ON	

LQN144 , 144 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQN144		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.145	0.18	0.215
c	0.115	——	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.40 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.07
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>22, 23</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>28</td><td>P175
TRG9_1</td></tr>
<tr><td>11 *1</td><td>13 *1</td><td>17 *1</td><td>20 *1</td><td>23</td><td>29</td><td>P040
A10 *2, *3, *4, *5
PPG23_1
TOT7_0
AIN1_0
SIN0_1</td></tr>
<tr><td>12 *1</td><td>14 *1</td><td>18 *1</td><td>21 *1</td><td>24</td><td>30</td><td>P041
A11 *2, *3, *4, *5
SIN9_0
ICU9_1
BIN1_0
INT12_0</td></tr>
<tr><td>13 *1</td><td>15 *1</td><td>19 *1</td><td>22 *1</td><td>25</td><td>31</td><td>P042
A12 *2, *3, *4, *5
SOT9_0
AN47
ICU8_1
TRG0_1
ZIN1_0</td></tr>
<tr><td>-</td><td>-</td><td>20 *1</td><td>23 *1</td><td>26</td><td>32</td><td>P043
A13 *4, *5
ICU7_1
TRG1_1</td></tr>
<tr><td>-</td><td>16 *1</td><td>21 *1</td><td>24 *1</td><td>27</td><td>33</td><td>P044
A14 *3, *4, *5
SCS9_0
ICU6_1
TRG2_1</td></tr>
<tr><td>14 *1</td><td>17 *1</td><td>22 *1</td><td>25 *1</td><td>28</td><td>34</td><td>P045
A15 *2, *3, *4, *5
SCK9_0
AN46
ICU5_1
TRG3_1
TOT1_2</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>26 *1</td><td>29</td><td>35</td><td>P046
A16 *5
ICU4_1
TRG4_1</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>36</td><td>P176
TRG10_0</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>34</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table><tr><th>Function*2</th></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit21 I/O (0)</td></tr><tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr><tr><td>A/D converter external trigger input 0 (1)</td></tr><tr><td>INT7 External interrupt input (1)</td></tr><tr><td>(CAN reception data 2 input
MB91F52xB ,MB91F52xD only)</td></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit22 I/O (0)</td></tr><tr><td>Serial chip select 2 I/O (0)</td></tr><tr><td>A/D converter external trigger input 1 (1)</td></tr><tr><td>INT2 External interrupt input (1)</td></tr><tr><td>(CAN transmission data 2 output
MB91F52xB ,MB91F52xD only)</td></tr></table>
(Correct)
<table><tr><th>Function*9</th></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit21 I/O (0)</td></tr><tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr><tr><td>A/D converter external trigger input 0 (1)</td></tr><tr><td>INT7 External interrupt input (1)</td></tr><tr><td>CAN reception data 2 input</td></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit22 I/O (0)</td></tr><tr><td>Serial chip select 2 I/O (0)</td></tr><tr><td>A/D converter external trigger input 1 (1)</td></tr><tr><td>INT2 External interrupt input (1)</td></tr><tr><td>CAN transmission data 2 output</td></tr></table></td></tr>
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