Infineon Technologies - MB91F522KWBPMC-GSK5E2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

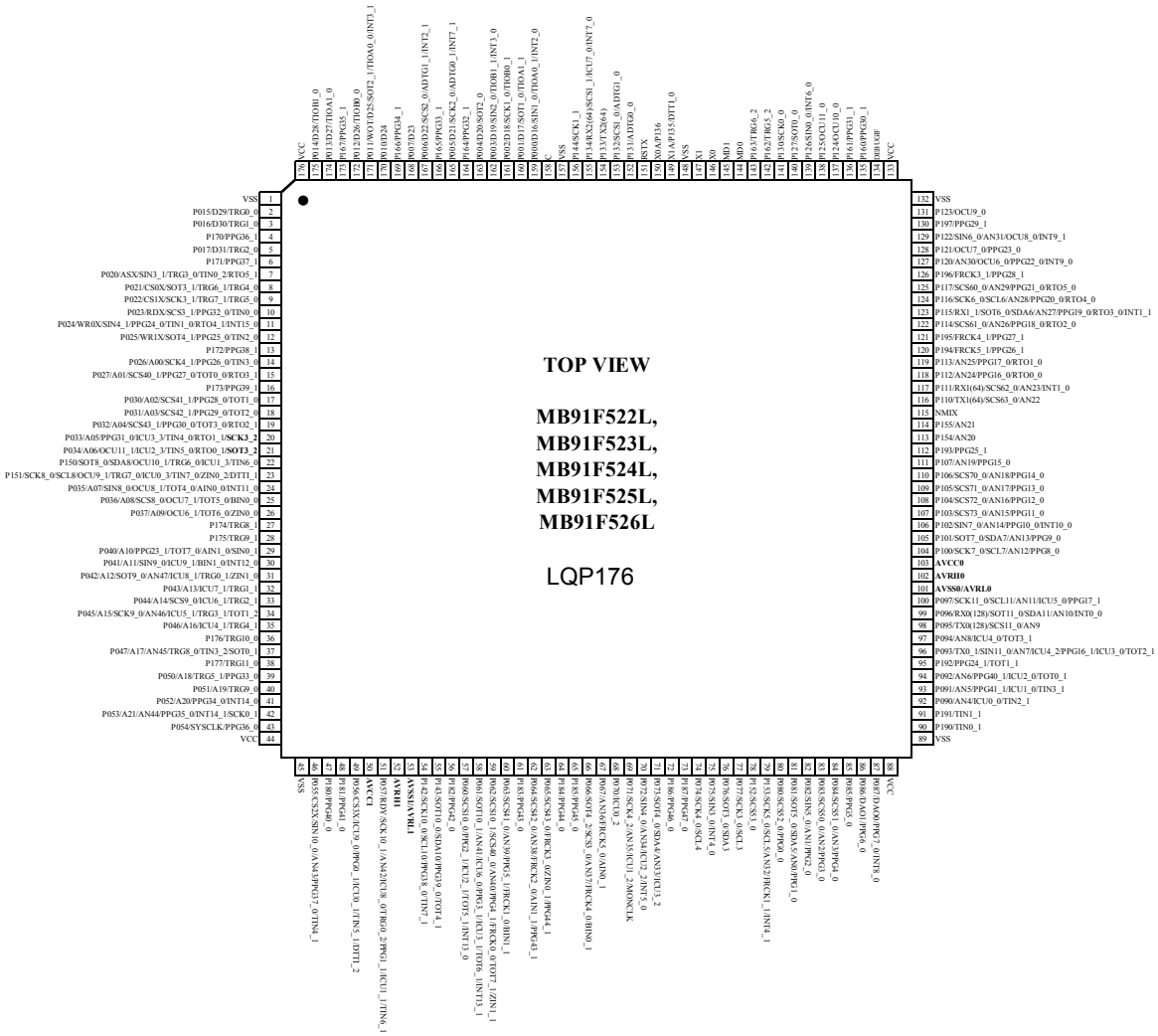
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522kwbpmc-gsk5e2

MB91F52xL

MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L

(TOP VIEW)



* In a single clock product, pin 149 and pin 150 are the general-purpose ports.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
9 *1	11 *1	14 *1	17 *1	20	24	P035	-	I	General-purpose I/O port
						A07 *2, *3, *4, *5	-		External bus/Address bit7 output
						SIN8_0 *2, *3	-		Multi-function serial ch.8 serial data input (0)
						OCU8_1	-		Output compare ch.8 output (1)
						TOT4_0	-		Reload timer ch.4 output (0)
						AIN0_0	-		U/D counter ch.0 AIN input (0)
						INT11_0	-		INT11 External interrupt input (0)
10 *1	12 *1	15 *1	18 *1	21	25	P036	-	A	General-purpose I/O port
						A08 *2, *3, *4, *5	-		External bus/Address bit8 output (0)
						SCS8_0 *2, *3	-		Serial chip select 8 I/O (0)
						OCU7_1	-		Output compare ch.7 output (1)
						TOT5_0	-		Reload timer ch.5 output (0)
						BIN0_0	-		U/D counter ch.0 BIN input (0)
-	-	16 *1	19 *1	22	26	P037	-	A	General-purpose I/O port
						A09 *4, *5	-		External bus/Address bit9 output (0)
						OCU6_1	-		Output compare ch.6 output (1)
						TOT6_0	-		Reload timer ch.6 output (0)
						ZIN0_0	-		U/D counter ch.0 ZIN input (0)
-	-	-	-	-	27	P174	-	A	General-purpose I/O port
						TRG8_1	-		PPG trigger 8 input (1)
-	-	-	-	-	28	P175	-	A	General-purpose I/O port
						TRG9_1	-		PPG trigger 9 input (1)
11 *1	13 *1	17 *1	20 *1	23	29	P040	-	A	General-purpose I/O port
						A10 *2, *3, *4, *5	-		External bus/Address bit10 output (0)
						PPG23_1	-		PPG ch.23 output (1)
						TOT7_0	-		Reload timer ch.7 output (0)
						AIN1_0	-		U/D counter ch.1 AIN input (0)
						SIN0_1	-		Multi-function serial ch.0 serial data input (1)
12 *1	14 *1	18 *1	21 *1	24	30	P041	-	I	General-purpose I/O port
						A11 *2, *3, *4, *5	-		External bus/Address bit11 output (0)
						SIN9_0	-		Multi-function serial ch.9 serial data input (0)
						ICU9_1	-		Input capture ch.9 input (1)
						BIN1_0	-		U/D counter ch.1 BIN input (0)
						INT12_0	-		INT12 External interrupt input (0)

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E3C$_H$	—	—	—	—	Reserved
000E40$_H$	PDDR00 [R] B,H,W XXXXXXXX	PDDR01 [R] B,H,W XXXXXXXX	PDDR02 [R] B,H,W XXXXXXXX	PDDR03 [R] B,H,W XXXXXXXX	Port Direct Read Register
000E44$_H$	PDDR04 [R] B,H,W XXXXXXXX	PDDR05 [R] B,H,W XXXXXXXX	PDDR06 [R] B,H,W XXXXXXXX	PDDR07 [R] B,H,W XXXXXXXX	
000E48$_H$	PDDR08 [R] B,H,W XXXXXXXX	PDDR09 [R] B,H,W XXXXXXXX	PDDR10 [R] B,H,W XXXXXXXX	PDDR11 [R] B,H,W XXXXXXXX	
000E4C$_H$	PDDR12 [R] B,H,W XXXXXXXX	PDDR13 [R] B,H,W -XXXXXXX	PDDR14 [R] B,H,W ---XXX--	PDDR15 [R] B,H,W --XXXXXX	
000E50$_H$	—	—	—	—	
000E54$_H$	—	—	—	—	
000E58$_H$	PDDR16 [R] B,H,W XXXXXXXX	PDDR17 [R] B,H,W XXXXXXXX	PDDR18 [R] B,H,W XXXXXXXX	PDDR19 [R] B,H,W XXXXXXXX	
000E5C$_H$	—	—	—	—	Reserved
000E60$_H$	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ----0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
000E64$_H$	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---00000	
000E68$_H$	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W ----0000	EPFR11 [R/W] B,H,W ----0000	
000E6C$_H$	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W ------00	EPFR14 [R/W] B,H,W ------00	EPFR15 [R/W] B,H,W -----000	
000E70$_H$	—	—	—	—	
000E74$_H$	—	—	—	—	
000E78$_H$	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0----	
000E7C$_H$	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
000E80$_H$	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	
000E84$_H$	EPFR36 [R/W] B,H,W ----000-	—	—	—	
000E88$_H$	—	—	EPFR42 [R/W] B,H,W ------00	EPFR43 [R/W] B,H,W 0--0000-	
000E8C$_H$	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
000E90$_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00125C$_H$	OCCPB4/OCCP4 [R/W] H,W 00000000 00000000		OCCPB5/OCCP5 [R/W] H,W 00000000 00000000		16-bit Output compare 4/5
001260$_H$	OCS45 [R/W] B,H,W -110--00 00001100		—	OCMOD45 [R/W] B,H,W ------00	
001264$_H$ to 001278$_H$	—	—	—	—	Reserved
00127C$_H$	IPCP0 [R] H,W 00000000 00000000		IPCP1 [R] H,W 00000000 00000000		16-bit Input capture 0/1
001280$_H$	ICS01 [R/W] B,H,W ------00 00000000		—	LSYNS [R/W] B,H,W ----0000	
001284$_H$	IPCP2 [R] H,W 00000000 00000000		IPCP3 [R] H,W 00000000 00000000		16-bit Input capture 2/3
001288$_H$	ICS23 [R/W] B,H,W ------00 00000000		—	—	
00128C$_H$ to 001298$_H$	—	—	—	—	Reserved
00129C$_H$	—	—	—	—	Reserved
0012A0$_H$	TMRR0 [R/W] H,W 00000000 00000001		TMRR1 [R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0012A4$_H$	TMRR2 [R/W] H,W 00000000 00000001		—	—	
0012A8$_H$	DTSCR0 [R/W] B,H,W 00000000	DTSCR1 [R/W] B,H,W 00000000	DTSCR2 [R/W] B,H,W 00000000	—	
0012AC$_H$	—	DTIR0 [R/W] B,H,W 000000--	—	DTMNS0 [R/W] B,H,W 00---000	
0012B0$_H$	—	SIGCR10 [R/W] B,H,W 00000000	—	SIGCR20 [R/W] B,H,W 000000-1	
0012B4$_H$	PICS0 [R/W] B,H,W 000000-- -------- -------- --------				
0012B8$_H$ to 0012CC$_H$	—	—	—	—	Reserved
0012D0$_H$	FRS5 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001750H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754H	— /(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001758H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175CH	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W -------- -------- *3 *4		
001760H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W -------- *3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W -------- *3	— /(SCSTR10) /(SFLR10) [R/W] B,H,W -------- *3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W -------- *3	
001764H	—	— /(SCSFR20) [R/W] B,H,W -------- *3	— /(SCSFR10) [R/W] B,H,W -------- *3	— /(SCSFR00) [R/W] B,H,W -------- *3	
001768H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -------- *3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W -------- *3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -------- *3	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
00176CH	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W -------- *2	— /(ISBA0) [R/W] B,H,W -------- *2	
001770H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	
001778H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W] B,H,W 00000000	Multi-UART1
00177CH	— /(RDR11/(TDR11))[R/W] B,H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
001780H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset.
001784H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W -------- -------- *3 *4		
001788H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W -------- *3	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W -------- *3	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W -------- *3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W -------- *3	
00178CH	—	— /(SCSFR21)[R/W] B,H,W -------- *3	— /(SCSFR11) [R/W] B,H,W -------- *3	— /(SCSFR01) [R/W] B,H,W -------- *3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001B78_H$	PCN216 [R/W] B,H,W --000000 -----110		PSDR16 [R/W] H,W 00000000 00000000		PPG16
$001B7C_H$	PTPC16 [R/W] H,W 00000000 00000000		—	—	
$001B80_H$	PCN17 [R/W] B,H,W 00000000 000000-0		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
$001B84_H$	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PTMR17 [R] H,W 11111111 11111111		
$001B88_H$	PCN217 [R/W] B,H,W --000000 -----110		PSDR17 [R/W] H,W 00000000 00000000		
$001B8C_H$	PTPC17 [R/W] H,W 00000000 00000000		—	—	
$001B90_H$	PCN18 [R/W] B,H,W 00000000 000000-0		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
$001B94_H$	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PTMR18 [R] H,W 11111111 11111111		
$001B98_H$	PCN218 [R/W] B,H,W --000000 -----110		PSDR18 [R/W] H,W 00000000 00000000		
$001B9C_H$	PTPC18 [R/W] H,W 00000000 00000000		—	—	
$001BA0_H$	PCN19 [R/W] B,H,W 00000000 000000-0		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
$001BA4_H$	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PTMR19 [R] H,W 11111111 11111111		
$001BA8_H$	PCN219 [R/W] B,H,W --000000 -----110		PSDR19 [R/W] H,W 00000000 00000000		
$001BAC_H$	PTPC19 [R/W] H,W 00000000 00000000		—	—	
$001BB0_H$	PCN20 [R/W] B,H,W 00000000 000000-0		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
$001BB4_H$	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PTMR20 [R] H,W 11111111 11111111		
$001BB8_H$	PCN220 [R/W] B,H,W --000000 -----110		PSDR20 [R/W] H,W 00000000 00000000		
$001BBC_H$	PTPC20 [R/W] H,W 00000000 00000000		—	—	
$001BC0_H$	PCN21 [R/W] B,H,W 00000000 000000-0		PCSR21 [W] H,W XXXXXXXX XXXXXXXX		PPG21
$001BC4_H$	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PTMR21 [R] H,W 11111111 11111111		
$001BC8_H$	PCN221 [R/W] B,H,W --000000 -----110		PSDR21 [R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001D20_H$	PCN43 [R/W] B,H,W 00000000 000000-0		PCSR43 [W] H,W XXXXXXXX XXXXXXXX		PPG43
$001D24_H$	PDUT43 [W] H,W XXXXXXXX XXXXXXXX		PTMR43 [R] H,W 11111111 11111111		
$001D28_H$	PCN243 [R/W] B,H,W --000000 -----110		PSDR43 [R/W] H,W 00000000 00000000		
$001D2C_H$	PTPC43 [R/W] H,W 00000000 00000000		—	—	
$001D30_H$	PCN44 [R/W] B,H,W 00000000 000000-0		PCSR44 [W] H,W XXXXXXXX XXXXXXXX		PPG44
$001D34_H$	PDUT44 [W] H,W XXXXXXXX XXXXXXXX		PTMR44 [R] H,W 11111111 11111111		
$001D38_H$	PCN244 [R/W] B,H,W --000000 -----110		PSDR44 [R/W] H,W 00000000 00000000		
$001D3C_H$	PTPC44 [R/W] H,W 00000000 00000000		—	—	
$001D40_H$	PCN45 [R/W] B,H,W 00000000 000000-0		PCSR45 [W] H,W XXXXXXXX XXXXXXXX		PPG45
$001D44_H$	PDUT45 [W] H,W XXXXXXXX XXXXXXXX		PTMR45 [R] H,W 11111111 11111111		
$001D48_H$	PCN245 [R/W] B,H,W --000000 -----110		PSDR45 [R/W] H,W 00000000 00000000		
$001D4C_H$	PTPC45 [R/W] H,W 00000000 00000000		—	—	
$001D50_H$	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXX XXXXXXXX		PPG46
$001D54_H$	PDUT46 [W] H,W XXXXXXXX XXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
$001D58_H$	PCN246 [R/W] B,H,W --000000 -----110		PSDR46 [R/W] H,W 00000000 00000000		
$001D5C_H$	PTPC46 [R/W] H,W 00000000 00000000		—	—	
$001D60_H$	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXX XXXXXXXX		PPG47
$001D64_H$	PDUT47 [W] H,W XXXXXXXX XXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
$001D68_H$	PCN247 [R/W] B,H,W --000000 -----110		PSDR47 [R/W] H,W 00000000 00000000		
$001D6C_H$	PTPC47 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002150_H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		CAN1 (64msb)
002154_H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158_H	—	—	—	—	
$00215C_H$	—	—	—	—	
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H to $00217C_H$	—				
002180_H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184_H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188_H	—	—	—	—	
$00218C_H$	—	—	—	—	
002190_H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194_H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198_H	—	—	—	—	
$00219C_H$	—	—	—	—	
$0021A0_H$	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
$0021A8_H$	—	—	—	—	
$0021AC_H$	—	—	—	—	
$0021B0_H$	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		
$0021B8_H$	—	—	—	—	
$0021BC_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
006000_H to $00EFFC_H$	—	—	—	—	Reserved
$00F000_H$ to $00FEFC_H$	—	—	—	—	Reserved [S]
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—				Reserved [S]
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF18_H$ to $00FFF4_H$	—				Reserved [S]
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
- -	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

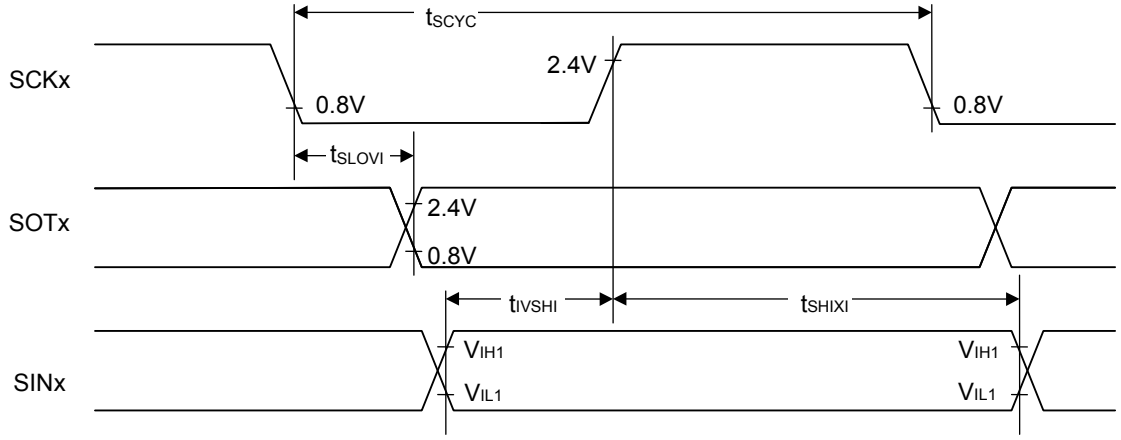
*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

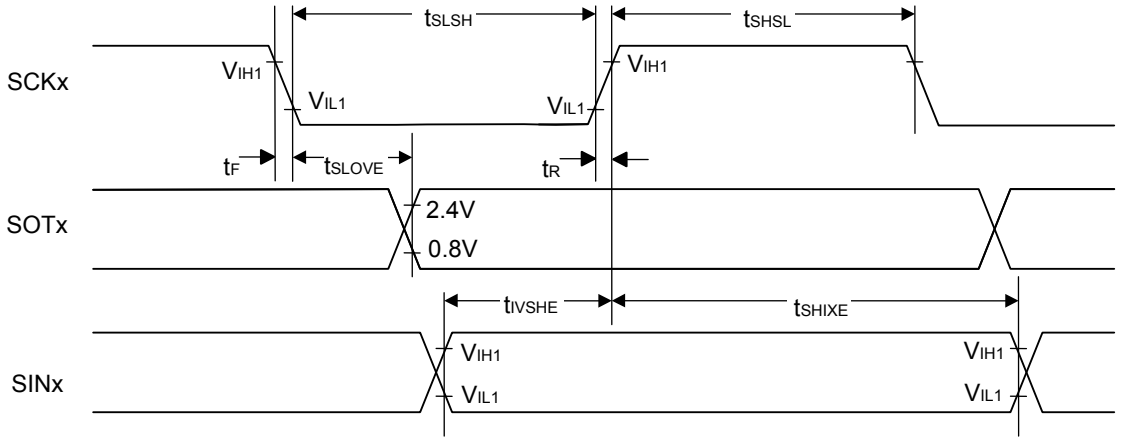
144 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

- Internal shift clock mode



- External shift clock mode

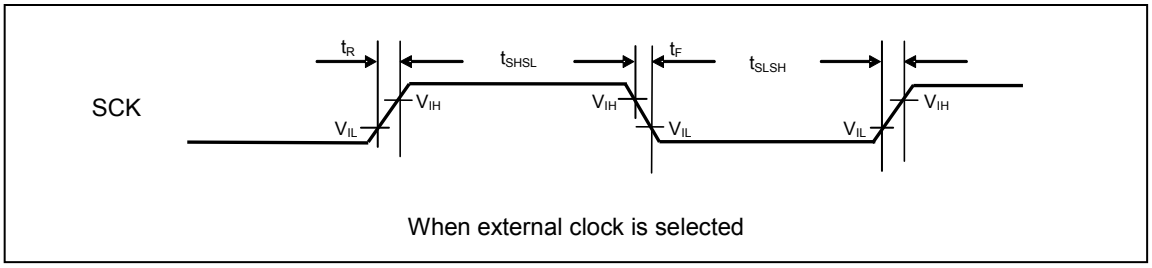


(4-1-5) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↑→SCS↑ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	

(4-3) LIN Interface (v2.1)(Asynchronous Serial Interface for LIN (v2.1)) timing
Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

A/D Converter

(1) 12-bit A/D Converter Electrical Characteristics

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±12	LSB	
Linearity error	-	-	-	-	± 4.0	LSB	
Differential linearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN47	AVRL-11.5LSB	-	AVRL+12.5LSB	V	1LSB= (V_{FST}-V_{OT})/4094
Full-scale transition voltage	V_{FST}	AN0 to AN47	AVRH-13.5LSB	-	AVRH+10.5LSB	V	
Sampling time	t_{SMP}	-	0.7	-	-	µs	*1
Compare time	t_{CMP}	-	0.7	-	-	µs	*1
A/D conversion time	t_{CNV}	-	1.4	-	-	µs	*1
Analog port input current	I_{AIN}	AN0 to AN47	-1.0	-	+1.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN47	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH	3.0	-	5.5	V	
	AVRL	AVSS/AVRL	-	0.0	-	V	
Power supply current	I_A	AVCC*3	-	0.47	0.63	mA	Per unit T_A: +105°C
			-	0.47	0.7	mA	Per unit T_A: +125°C
	I_{AH}		-	-	2.5	µA	*2
	I_R	AVRH	-	1	1.96	mA	Per unit
	I_{RH}		-	-	1.6	µA	*2
Variation between channels	-	AN0 to AN47	-	-	4	LSB	

*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

*3: The power supply current described only current value on A/D converter.
The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.

(Note) Please use the clock of 0.5MHz-20MHz for the output clock of A/D converter to guarantee accuracy.

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526JWBPMC	Yes	ON	ON	LQM・120 pin, Plastic
MB91F526JYBPMC			OFF	
MB91F526JJBPMC		OFF	ON	
MB91F526JLBPMC			OFF	
MB91F525JWBPMC		ON	ON	
MB91F525JYBPMC			OFF	
MB91F525JJBPMC		OFF	ON	
MB91F525JLBPMC			OFF	
MB91F524JWBPMC		ON	ON	
MB91F524JYBPMC			OFF	
MB91F524JJBPMC		OFF	ON	
MB91F524JLBPMC			OFF	
MB91F523JWBPMC		ON	ON	
MB91F523JYBPMC			OFF	
MB91F523JJBPMC		OFF	ON	
MB91F523JLBPMC			OFF	
MB91F522JWBPMC		ON	ON	
MB91F522JYBPMC			OFF	
MB91F522JJBPMC		OFF	ON	
MB91F522JLBPMC			OFF	
MB91F526JSBPMC	None	ON	ON	
MB91F526JUBPMC			OFF	
MB91F526JHBPMC		OFF	ON	
MB91F526JKBPMC			OFF	
MB91F525JSBPMC		ON	ON	
MB91F525JUBPMC			OFF	
MB91F525JHBPMC		OFF	ON	
MB91F525JKBPMC			OFF	
MB91F524JSBPMC		ON	ON	
MB91F524JUBPMC			OFF	
MB91F524JHBPMC		OFF	ON	
MB91F524JKBPMC			OFF	
MB91F523JSBPMC		ON	ON	
MB91F523JUBPMC			OFF	
MB91F523JHBPMC		OFF	ON	
MB91F523JKBPMC			OFF	
MB91F522JSBPMC		ON	ON	
MB91F522JUBPMC			OFF	
MB91F522JHBPMC		OFF	ON	
MB91F522JKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526BWBPMC1	Yes	ON	ON	LQD・64 pin, Plastic
MB91F526BYBPMC1			OFF	
MB91F526BJBPMC1		OFF	ON	
MB91F526BLBPMC1			OFF	
MB91F525BWBPMC1		ON	ON	
MB91F525BYBPMC1			OFF	
MB91F525BJBPMC1		OFF	ON	
MB91F525BLBPMC1			OFF	
MB91F524BWBPMC1		ON	ON	
MB91F524BYBPMC1			OFF	
MB91F524BJBPMC1		OFF	ON	
MB91F524BLBPMC1			OFF	
MB91F523BWBPMC1		ON	ON	
MB91F523BYBPMC1			OFF	
MB91F523BJBPMC1		OFF	ON	
MB91F523BLBPMC1			OFF	
MB91F522BWBPMC1		ON	ON	
MB91F522BYBPMC1			OFF	
MB91F522BJBPMC1		OFF	ON	
MB91F522BLBPMC1			OFF	
MB91F526BSBPMC1	None	ON	ON	
MB91F526BUBPMC1			OFF	
MB91F526BHBPMC1		OFF	ON	
MB91F526BKBPMC1			OFF	
MB91F525BSBPMC1		ON	ON	
MB91F525BUBPMC1			OFF	
MB91F525BHBPMC1		OFF	ON	
MB91F525BKBPMC1			OFF	
MB91F524BSBPMC1		ON	ON	
MB91F524BUBPMC1			OFF	
MB91F524BHBPMC1		OFF	ON	
MB91F524BKBPMC1			OFF	
MB91F523BSBPMC1		ON	ON	
MB91F523BUBPMC1			OFF	
MB91F523BHBPMC1		OFF	ON	
MB91F523BKBPMC1			OFF	
MB91F522BSBPMC1		ON	ON	
MB91F522BUBPMC1			OFF	
MB91F522BHBPMC1		OFF	ON	
MB91F522BKBPMC1			OFF	

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
*2: For details of the package, see "■ PACKAGE DIMENSIONS ".

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>21, 22</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="7">7</td><td rowspan="7">9</td><td rowspan="7">11</td><td rowspan="7">14</td><td rowspan="7">17</td><td rowspan="7">21</td><td>P034</td></tr>
<tr><td>A06</td></tr>
<tr><td>OCU11_1</td></tr>
<tr><td>ICU2_3</td></tr>
<tr><td>TIN5_0</td></tr>
<tr><td>RTO0_1</td></tr>
<tr><td>SOT3_2</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="8">8</td><td rowspan="8">10</td><td rowspan="8">13</td><td rowspan="8">16</td><td rowspan="8">19</td><td rowspan="8">23</td><td>P151</td></tr>
<tr><td>SCK8_0/ SCL8</td></tr>
<tr><td>OCU9_1</td></tr>
<tr><td>TRG7_0</td></tr>
<tr><td>ICU0_3</td></tr>
<tr><td>TIN7_0</td></tr>
<tr><td>ZIN0_2</td></tr>
<tr><td>DTTI_1</td></tr>
<tr><td rowspan="7">9</td><td rowspan="7">11</td><td rowspan="7">14</td><td rowspan="7">17</td><td rowspan="7">20</td><td rowspan="7">24</td><td>P035</td></tr>
<tr><td>A07</td></tr>
<tr><td>SIN8_0</td></tr>
<tr><td>OCU8_1</td></tr>
<tr><td>TOT4_0</td></tr>
<tr><td>AIN0_0</td></tr>
<tr><td>INT11_0</td></tr>
<tr><td rowspan="7">10</td><td rowspan="7">12</td><td rowspan="7">15</td><td rowspan="7">18</td><td rowspan="7">21</td><td rowspan="7">25</td><td>P036</td></tr>
<tr><td>A08</td></tr>
<tr><td>SCS8_0</td></tr>
<tr><td>OCU7_1</td></tr>
<tr><td>TOT5_0</td></tr>
<tr><td>BIN0_0</td></tr>
<tr><td rowspan="6">-</td><td rowspan="6">-</td><td rowspan="6">16</td><td rowspan="6">19</td><td rowspan="6">22</td><td rowspan="6">26</td><td>P037</td></tr>
<tr><td>A09</td></tr>
<tr><td>OCU6_1</td></tr>
<tr><td>TOT6_0</td></tr>
<tr><td>ZIN0_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">27</td><td>P174</td></tr>
<tr><td>TRG8_1</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>141</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 176pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45 *5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
<tr><td>141</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 176pins.

(Error)
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>142</td><td>■Electrical Characteristics
1. Absolute Maximum Ratings</td><td>The remarks of "L" level average output current" and "H" level average output current" modified as follows.

(Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td rowspan="2">"L" level average output current *4</td><td>I_{OLAV1}</td><td>-</td><td>4</td><td>mA</td><td rowspan="2"></td></tr>
<tr><td>I_{OLAV2}</td><td>-</td><td>12</td><td>mA</td></tr>
<tr><td rowspan="2">"H" level average output current *4</td><td>I_{OHAV1}</td><td>-</td><td>-4</td><td>mA</td><td></td></tr>
<tr><td>I_{OHAV2}</td><td>-</td><td>-12</td><td>mA</td><td></td></tr>
</table>

(Correct)
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<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
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<tr><td rowspan="2">"H" level average output current *4</td><td>I_{OHAV1}</td><td>-</td><td>-4</td><td>mA</td><td>*9</td></tr>
<tr><td>I_{OHAV2}</td><td>-</td><td>-12</td><td>mA</td><td>*10</td></tr>
</table>
</td></tr>
</table>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Package ↓ Package*2 Added the following description. *1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products. Corrected the following description. For details of the package, see "■ PACKAGE DIMENSIONS ". ↓ *2: For details of the package, see "■ PACKAGE DIMENSIONS ". Added the following description. • ORDERING INFORMATION MB91F52xxxC Company name and layout design change
*A	4999456	JHMU	11/13/2015	Updated to Cypress template. Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in “Absolute Maximum Ratings” of “ELECTRICAL CHARACTERISTICS”. *9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106. Added Errata section.
*B	5112138	KUME	01/28/2016	Fixed some clerical errors. For details, please see the chapter 18. Major Changes.
*C	5196285	KUME	04/28/2016	For details, please see the chapter 19. Major Changes.
*D	5318862	KUME	06/23/2016	For details, please see the chapter 19. Major Changes.