Infineon Technologies - MB91F523BSCPMC1-GTE1 Datasheet

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What is "Embedded - Microcontrollers"?

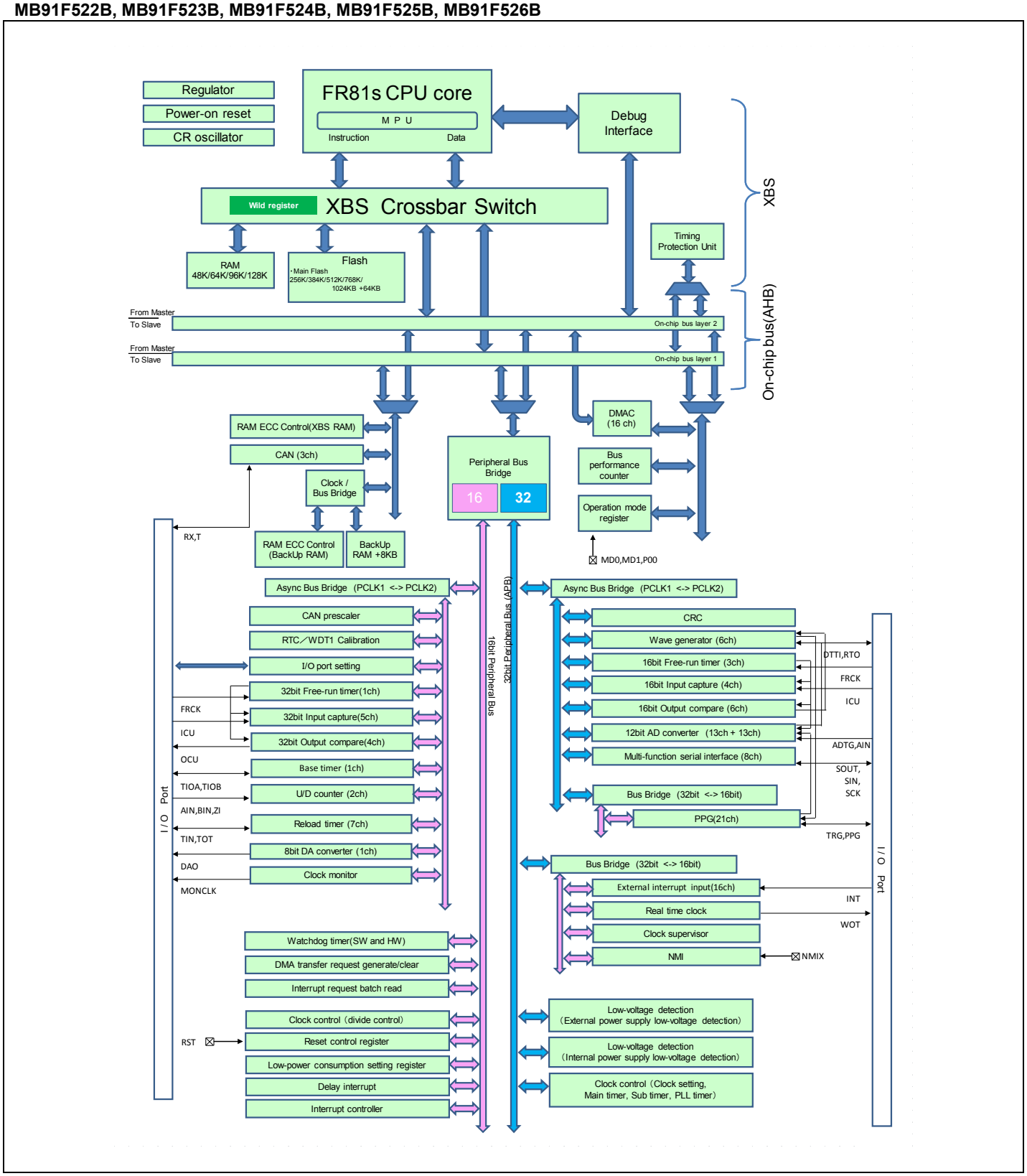
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f523bscpmc1-gte1

7. Block Diagram

MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B



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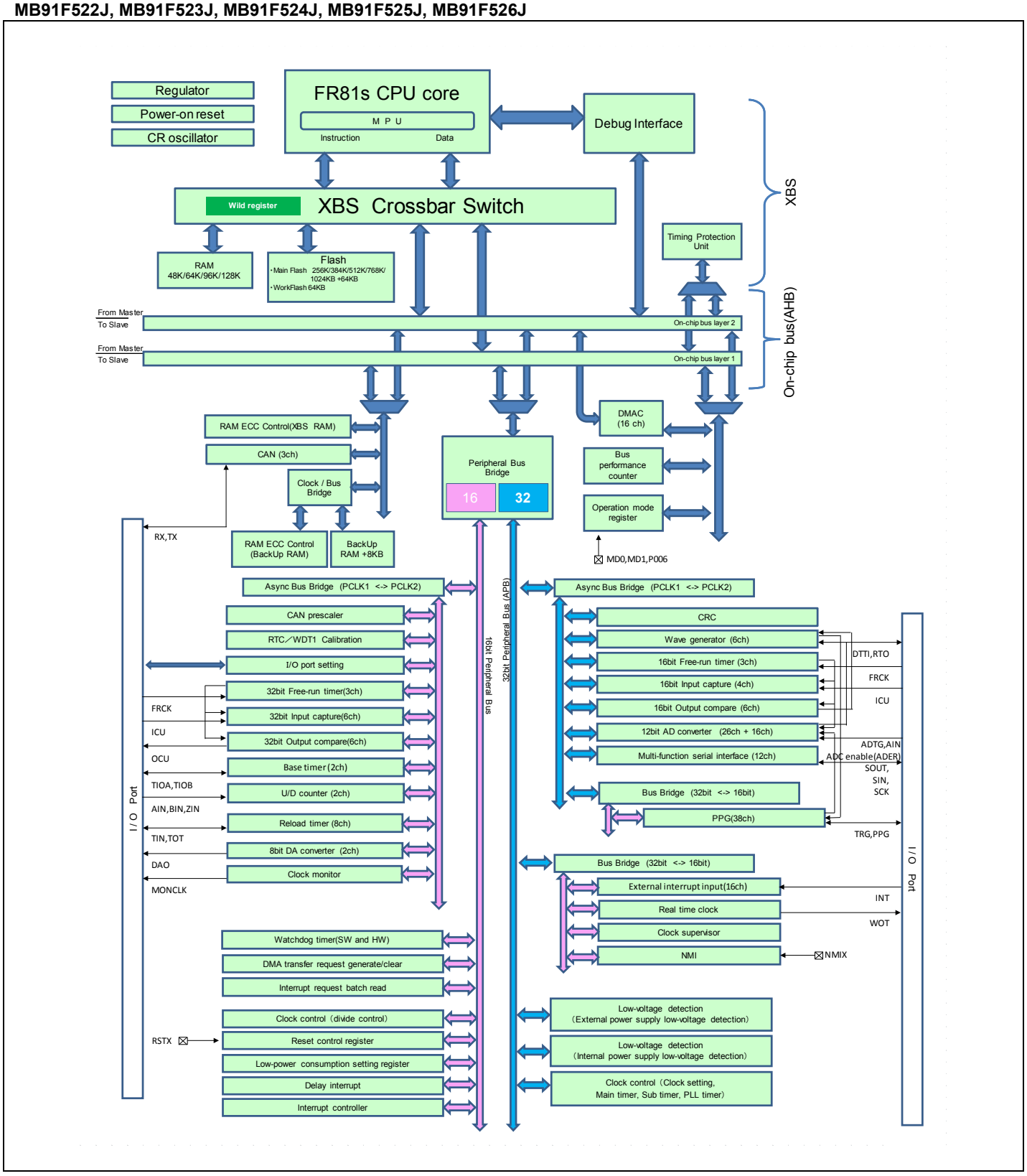


Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E3C$_H$	—	—	—	—	Reserved
000E40$_H$	PDDR00 [R] B,H,W XXXXXXXX	PDDR01 [R] B,H,W XXXXXXXX	PDDR02 [R] B,H,W XXXXXXXX	PDDR03 [R] B,H,W XXXXXXXX	Port Direct Read Register
000E44$_H$	PDDR04 [R] B,H,W XXXXXXXX	PDDR05 [R] B,H,W XXXXXXXX	PDDR06 [R] B,H,W XXXXXXXX	PDDR07 [R] B,H,W XXXXXXXX	
000E48$_H$	PDDR08 [R] B,H,W XXXXXXXX	PDDR09 [R] B,H,W XXXXXXXX	PDDR10 [R] B,H,W XXXXXXXX	PDDR11 [R] B,H,W XXXXXXXX	
000E4C$_H$	PDDR12 [R] B,H,W XXXXXXXX	PDDR13 [R] B,H,W -XXXXXXX	PDDR14 [R] B,H,W ---XXX--	PDDR15 [R] B,H,W --XXXXXX	
000E50$_H$	—	—	—	—	
000E54$_H$	—	—	—	—	
000E58$_H$	PDDR16 [R] B,H,W XXXXXXXX	PDDR17 [R] B,H,W XXXXXXXX	PDDR18 [R] B,H,W XXXXXXXX	PDDR19 [R] B,H,W XXXXXXXX	
000E5C$_H$	—	—	—	—	Reserved
000E60$_H$	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ----0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
000E64$_H$	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---00000	
000E68$_H$	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W ----0000	EPFR11 [R/W] B,H,W ----0000	
000E6C$_H$	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W ------00	EPFR14 [R/W] B,H,W ------00	EPFR15 [R/W] B,H,W -----000	
000E70$_H$	—	—	—	—	
000E74$_H$	—	—	—	—	
000E78$_H$	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0----	
000E7C$_H$	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
000E80$_H$	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	
000E84$_H$	EPFR36 [R/W] B,H,W ----000-	—	—	—	
000E88$_H$	—	—	EPFR42 [R/W] B,H,W ------00	EPFR43 [R/W] B,H,W 0--0000-	
000E8C$_H$	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
000E90$_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0012D4$_H$	FRS6 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare
0012D8$_H$	FRS7 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
0012DC$_H$ to 0012FC$_H$	—	—	—	—	Reserved
001300$_H$	—				Reserved
001304$_H$	ADTSS0[R/W] B,H,W -------0	—	—	—	12-bit A/D converter 1/2 unit
001308$_H$	ADTSE0[R/W] B,H,W 00000000 00000000 00000000 00000000				
00130C$_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001310$_H$	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
001314$_H$	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
001318$_H$	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
00131C$_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
001320$_H$	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
001324$_H$	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001328$_H$	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		
00132C$_H$	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001330$_H$	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
001334$_H$	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001338$_H$	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
00133C$_H$	ADCOMP24/ADCOMPB24[R/W] H,W 00000000 00000000		ADCOMP25/ADCOMPB25[R/W] H,W 00000000 00000000		
001340$_H$	ADCOMP26/ADCOMPB26[R/W] H,W 00000000 00000000		ADCOMP27/ADCOMPB27[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001750H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754H	— /(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001758H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175CH	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W -------- -------- *3 *4		
001760H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W -------- *3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W -------- *3	— /(SCSTR10) /(SFLR10) [R/W] B,H,W -------- *3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W -------- *3	
001764H	—	— /(SCSFR20) [R/W] B,H,W -------- *3	— /(SCSFR10) [R/W] B,H,W -------- *3	— /(SCSFR00) [R/W] B,H,W -------- *3	
001768H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -------- *3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W -------- *3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -------- *3	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
00176CH	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W -------- *2	— /(ISBA0) [R/W] B,H,W -------- *2	
001770H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	
001778H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W] B,H,W 00000000	Multi-UART1
00177CH	— /(RDR11/(TDR11))[R/W] B,H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
001780H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset.
001784H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W -------- -------- *3 *4		
001788H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W -------- *3	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W -------- *3	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W -------- *3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W -------- *3	
00178CH	—	— /(SCSFR21)[R/W] B,H,W -------- *3	— /(SCSFR11) [R/W] B,H,W -------- *3	— /(SCSFR01) [R/W] B,H,W -------- *3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002254_H	IF2DTB12 [R/W] B,H,W 00000000 00000000		IF2DTB22 [R/W] B,H,W 00000000 00000000		CAN2 (64msb)
002258_H	—	—	—	—	
$00225C_H$	—	—	—	—	
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H to $00227C_H$	—				
002280_H	TREQR22 [R] B,H,W 00000000 00000000		TREQR12 [R] B,H,W 00000000 00000000		
002284_H	TREQR42 [R] B,H,W 00000000 00000000		TREQR32 [R] B,H,W 00000000 00000000		
002288_H	—	—	—	—	
$00228C_H$	—	—	—	—	
002290_H	NEWDT22 [R] B,H,W 00000000 00000000		NEWDT12 [R] B,H,W 00000000 00000000		
002294_H	NEWDT42 [R] B,H,W 00000000 00000000		NEWDT32 [R] B,H,W 00000000 00000000		
002298_H	—	—	—	—	
$00229C_H$	—	—	—	—	
$0022A0_H$	INTPND22 [R] B,H,W 00000000 00000000		INTPND12 [R] B,H,W 00000000 00000000		
$0022A4_H$	INTPND42 [R] B,H,W 00000000 00000000		INTPND32 [R] B,H,W 00000000 00000000		
$0022A8_H$	—	—	—	—	
$0022AC_H$	—	—	—	—	
$0022B0_H$	MSGVAL22 [R] B,H,W 00000000 00000000		MSGVAL12 [R] B,H,W 00000000 00000000		
$0022B4_H$	MSGVAL42 [R] B,H,W 00000000 00000000		MSGVAL32 [R] B,H,W 00000000 00000000		
$0022B8_H$	—	—	—	—	
$0022BC_H$	—	—	—	—	
$0022C0_H$ to $0022FC_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002300_H	DFCTLR [R/W] B,H,W -0------ --------		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304_H	—	—	—	—	
002308_H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W --------	FLIFFER2 [R/W] B,H,W --------	Flash / WorkFlash
$00230C_H$ to $0023FC_H$	—				Reserved
002400_H	SEEARX [R] B,H,W -0000000 00000000		DEEARX [R] B,H,W -0000000 00000000		XBS RAM ECC control
002404_H	EECSRX [R/W] B,H,W ----00--	—	EFEARX [R/W] B,H,W -0000000 00000000		
002408_H	—	EFECRX [R/W] B,H,W -------0 00000000 00000000			
$00240C_H$ to $002FFC_H$	—				Reserved
003000_H	SEEARA [R] B,H,W -----000 00000000		DEEARA [R] B,H,W -----000 00000000		Backup RAM ECC control
003004_H	EECSRA [R/W] B,H,W ----00--	—	EFEARA [R/W] B,H,W -----000 00000000		
003008_H	—	EFECRA [R/W] B,H,W -------0 00000000 00000000			
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- -0000000 00000000				RAM/ diagnosis XBS RAM
003010_H	TEAR1X[R] B,H,W 000----- -------- -0000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- -0000000 00000000				
003018_H	TAEARX [R/W] B,H,W -1111111 11111111		TASARX [R/W] B,H,W -0000000 00000000		
$00301C_H$	TFECRX [R/W] B,H,W ----0000	TICRX [R/W] B,H,W ----0000	TTCRX [R/W] B,H,W ------00 00001100		
003020_H	TSRCRX [W] B,H,W 0-------	—	—	TKCCRX [R/W] B,H,W 00----00	
003024_H to $00302C_H$	—				Reserved

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU 6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40

(T_A: -40°C to +125°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	102	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	115	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	115	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	92	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	105	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	105	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	82	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	95	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	95	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	82	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	72	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation , Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

AC Characteristics

(1) Main Clock Timing

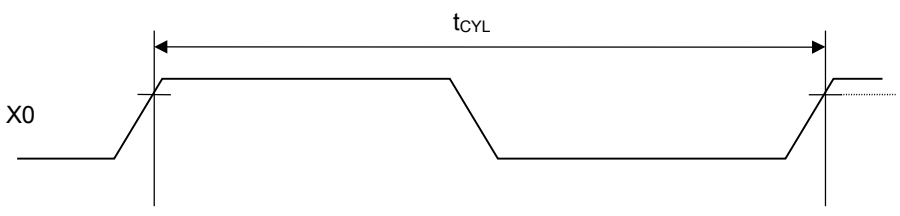
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS} =AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1		-	4	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency*1	F_{CP}	-		2	-	80	MHz	CPU clock
	F_{CPP}			1		40		Peripheral bus clock
	F_{CPT}			1		40		External bus clock (When V_{CC}=5.0V is used) *2
				1		32		External bus clock (When V_{CC}=3.3V is used)
Internal operating clock cycle time*1	t_{CP}	-	-	12.5	-	500	ns	CPU clock
	t_{CPP}			25		1000		Peripheral bus clock
	t_{CPT}			25		1000		External bus clock (When V_{CC}=5.0V is used)
				31.25		1000		External bus clock (When V_{CC}=3.3V is used)
CAN PLL jitter (during lock)	t_{PJ}	-		-10	-	10	ns	F_{CP}=80MHz (4MHz□Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	-		50	100	150	kHz	

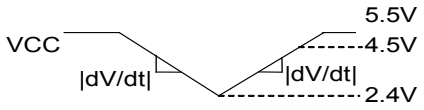
*1: The maximum / minimum value is defined when using the main clock and PLL clock.

*2: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

• X0,X1 clock timing



・Maximum ramp rate guaranteed to not generate power-on reset



Flash memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbytes sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbytes sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbytes sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbytes sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A=+85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.

In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc at 2.7V or more within the duration calculated by the following expression:

$$Td^{*}[\mu s] + (\text{period of PCLK } [\mu s] \times 257) + 50\ [\mu s]$$

*: See “4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) ”

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KYBPMC			OFF	
MB91F526KJBPMC		OFF	ON	
MB91F526KLBPMC			OFF	
MB91F525KWBPMC		ON	ON	
MB91F525KYBPMC			OFF	
MB91F525KJBPMC		OFF	ON	
MB91F525KLBPMC			OFF	
MB91F524KWBPMC		ON	ON	
MB91F524KYBPMC			OFF	
MB91F524KJBPMC		OFF	ON	
MB91F524KLBPMC			OFF	
MB91F523KWBPMC		ON	ON	
MB91F523KYBPMC			OFF	
MB91F523KJBPMC		OFF	ON	
MB91F523KLBPMC			OFF	
MB91F522KWBPMC		ON	ON	
MB91F522KYBPMC			OFF	
MB91F522KJBPMC		OFF	ON	
MB91F522KLBPMC			OFF	
MB91F526KSBPMC	None	ON	ON	
MB91F526KUBPMC			OFF	
MB91F526KHBPMC		OFF	ON	
MB91F526KKBPMC			OFF	
MB91F525KSBPMC		ON	ON	
MB91F525KUBPMC			OFF	
MB91F525KHBPMC		OFF	ON	
MB91F525KKBPMC			OFF	
MB91F524KSBPMC		ON	ON	
MB91F524KUBPMC			OFF	
MB91F524KHBPMC		OFF	ON	
MB91F524KKBPMC			OFF	
MB91F523KSBPMC		ON	ON	
MB91F523KUBPMC			OFF	
MB91F523KHBPMC		OFF	ON	
MB91F523KKBPMC			OFF	
MB91F522KSBPMC		ON	ON	
MB91F522KUBPMC			OFF	
MB91F522KHBPMC		OFF	ON	
MB91F522KKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYBPMC1			OFF	
MB91F526KJBPMC1		OFF	ON	
MB91F526KLBPMC1			OFF	
MB91F525KWBPMC1		ON	ON	
MB91F525KYBPMC1			OFF	
MB91F525KJBPMC1		OFF	ON	
MB91F525KLBPMC1			OFF	
MB91F524KWBPMC1		ON	ON	
MB91F524KYBPMC1			OFF	
MB91F524KJBPMC1		OFF	ON	
MB91F524KLBPMC1			OFF	
MB91F523KWBPMC1		ON	ON	
MB91F523KYBPMC1			OFF	
MB91F523KJBPMC1		OFF	ON	
MB91F523KLBPMC1			OFF	
MB91F522KWBPMC1		ON	ON	
MB91F522KYBPMC1			OFF	
MB91F522KJBPMC1		OFF	ON	
MB91F522KLBPMC1			OFF	
MB91F526KSBPMC1	None	ON	ON	
MB91F526KUBPMC1			OFF	
MB91F526KHBPMC1		OFF	ON	
MB91F526KKBPMC1			OFF	
MB91F525KSBPMC1		ON	ON	
MB91F525KUBPMC1			OFF	
MB91F525KHBPMC1		OFF	ON	
MB91F525KKBPMC1			OFF	
MB91F524KSBPMC1		ON	ON	
MB91F524KUBPMC1			OFF	
MB91F524KHBPMC1		OFF	ON	
MB91F524KKBPMC1			OFF	
MB91F523KSBPMC1		ON	ON	
MB91F523KUBPMC1			OFF	
MB91F523KHBPMC1		OFF	ON	
MB91F523KKBPMC1			OFF	
MB91F522KSBPMC1		ON	ON	
MB91F522KUBPMC1			OFF	
MB91F522KHBPMC1		OFF	ON	
MB91F522KKBPMC1			OFF	

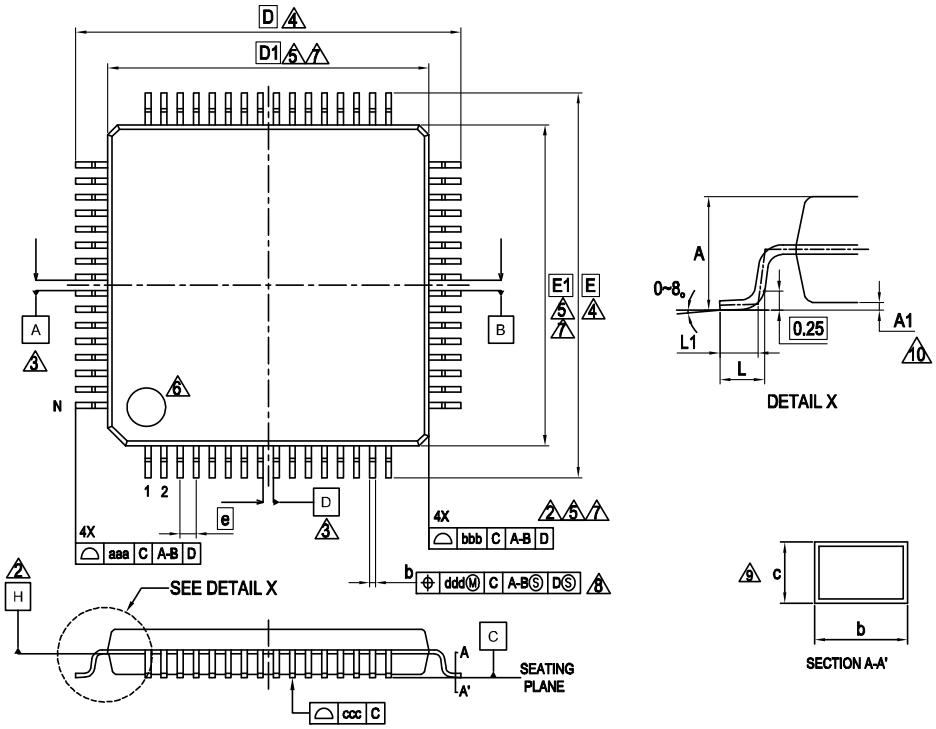
Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526BWCPMC1	Yes	ON	ON	LQD・64 pin, Plastic
MB91F526BYCPMC1			OFF	
MB91F526BJCPMC1		OFF	ON	
MB91F526BLCPMC1			OFF	
MB91F525BWCPMC1		ON	ON	
MB91F525BYCPMC1			OFF	
MB91F525BJCPMC1		OFF	ON	
MB91F525BLCPMC1			OFF	
MB91F524BWCPMC1		ON	ON	
MB91F524BYCPMC1			OFF	
MB91F524BJCPMC1		OFF	ON	
MB91F524BLCPMC1			OFF	
MB91F523BWCPMC1		ON	ON	
MB91F523BYCPMC1			OFF	
MB91F523BJCPMC1		OFF	ON	
MB91F523BLCPMC1			OFF	
MB91F522BWCPMC1		ON	ON	
MB91F522BYCPMC1			OFF	
MB91F522BJCPMC1		OFF	ON	
MB91F522BLCPMC1			OFF	
MB91F526BSCPMC1	None	ON	ON	
MB91F526BUCPMC1			OFF	
MB91F526BHCPMC1		OFF	ON	
MB91F526BKCPMC1			OFF	
MB91F525BSCPMC1		ON	ON	
MB91F525BUCPMC1			OFF	
MB91F525BHCPMC1		OFF	ON	
MB91F525BKCPMC1			OFF	
MB91F524BSCPMC1		ON	ON	
MB91F524BUCPMC1			OFF	
MB91F524BHCPMC1		OFF	ON	
MB91F524BKCPMC1			OFF	
MB91F523BSCPMC1		ON	ON	
MB91F523BUCPMC1			OFF	
MB91F523BHCPMC1		OFF	ON	
MB91F523BKCPMC1			OFF	
MB91F522BSCPMC1		ON	ON	
MB91F522BUCPMC1			OFF	
MB91F522BHCPMC1		OFF	ON	
MB91F522BKCPMC1			OFF	

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
*2: For details of the package, see "■ PACKAGE DIMENSIONS ".

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526KWDPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KJDPMC1		OFF	ON	
MB91F525KWDPMC1		ON	ON	
MB91F525KJDPMC1		OFF	ON	
MB91F524KWDPMC1		ON	ON	
MB91F524KJDPMC1		OFF	ON	
MB91F523KWDPMC1		ON	ON	
MB91F523KJDPMC1		OFF	ON	
MB91F522KWDPMC1		ON	ON	
MB91F522KJDPMC1		OFF	ON	
MB91F526KSDPMC1	None	ON	ON	
MB91F526KHDPMC1		OFF	ON	
MB91F525KSDPMC1		ON	ON	
MB91F525KHDPMC1		OFF	ON	
MB91F524KSDPMC1		ON	ON	
MB91F524KHDPMC1		OFF	ON	
MB91F523KSDPMC1		ON	ON	
MB91F523KHDPMC1		OFF	ON	
MB91F522KSDPMC1		ON	ON	
MB91F522KHDPMC1		OFF	ON	
MB91F526JWDPMC	Yes	ON	ON	LQM・120 pin, Plastic
MB91F526JJDPMC		OFF	ON	
MB91F525JWDPMC		ON	ON	
MB91F525JJDPMC		OFF	ON	
MB91F524JWDPMC		ON	ON	
MB91F524JJDPMC		OFF	ON	
MB91F523JWDPMC		ON	ON	
MB91F523JJDPMC		OFF	ON	
MB91F522JWDPMC		ON	ON	
MB91F522JJDPMC		OFF	ON	
MB91F526JSDPMC	None	ON	ON	
MB91F526JHDPMC		OFF	ON	
MB91F525JSDPMC		ON	ON	
MB91F525JHDPMC		OFF	ON	
MB91F524JSDPMC		ON	ON	
MB91F524JHDPMC		OFF	ON	
MB91F523JSDPMC		ON	ON	
MB91F523JHDPMC		OFF	ON	
MB91F522JSDPMC		ON	ON	
MB91F522JHDPMC		OFF	ON	

17. Package Dimensions

LQD064 , 64 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQD64		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	0.20	0.25
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	64		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Page	Section	Change Results
8	■Product Lineup	Corrected the following description for Product lineup comparison(100 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
8	■Product Lineup	Added the following sentences under Product lineup comparison(100 pin) *1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
9	■Product Lineup	Corrected the following description for Product lineup comparison(120 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
9	■Product Lineup	Added the following sentences under Product lineup comparison(120 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
10	■Product Lineup	Corrected the following description for Product lineup comparison(144 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
10	■Product Lineup	Added the following sentences under Product lineup comparison(144 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).
11	■Product Lineup	Corrected the following description for Product lineup comparison(176 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
11	■Product Lineup	Added the following sentences under Product lineup comparison(176 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Corrected the following description to "Type D, E". I^2C Schmitt input → I^2C hysteresis input Block Diagram Corrected the following description. • MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B • MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D • MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F • MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J • MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K • MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L Electrical Characteristics 2. Recommended operating conditions: *1 of the operation guarantee),contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset Electrical Characteristics 3.DC characteristics Corrected the value of "ICCT5 When using sub clock 32kHz TA=+25°C ". Max 1420µA → Max 2000µA Corrected the value of "Power supply voltage range". (TA:-40°C to +105°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V) ↓ (T_A:-40°C to +105°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,V_{SS}=AV_{SS}=0.0V) Corrected the value of "Power supply voltage range". (T_A:-40°C to +125°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V) ↓ (T_A:-40°C to +125°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,V_{SS}=AV_{SS}=0.0V) Corrected the value of " Pull-up resistance R_{UP1}". Vcc=3.3V±0.3V Min 49 Max 140 →Min 45 Max 140 Corrected the following description. Pull-up resistance R_{UP2} Port pin other than P035,041,093,122 → P073,074,076,077 Corrected the value of " Pull-up resistance R_{UP2}". VCC=5.0V±10% Min 25 Max 100 →Min 25 Max 60 VCC=3.3V±0.3V Min 49 Max 140 →Min 33 Max 90 Added the value of " Pull-up resistance R_{UP3}". Pin name : Port pin other than P035,041,073,074,076,077,093,122 VCC=5.0V±10% Min 25 Max 100 VCC=3.3V±0.3V Min 45 Max 140 Electrical Characteristics 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-1),(4-1-2),(4-1-3),(4-1-4) (4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVI} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVI} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Value: Min -30 Max 30 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min -30 Max 30 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min -300 Max 300 (4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time t_{IVSHI} (4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time t_{IVSLI} Corrected the following description. Pin name: SCK0 to SCK11 SIN0 to SIN11 Value: Min 34 Max - ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11 Value: Min 34 Max - Pin name: SCK3,SCK4,SIN3,SIN4 Value: Min 300 Max – (4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVE} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVE} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min - Max 33 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min - Max 33 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min - Max 300 (4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time t_F Corrected the following description. Pin name: SCK0 to SCK2,SCK5 to SCK11 Value: Min - Max 5 Pin name: SCK3,SCK4 Value: Min - Max 250 ↓ Pin name: SCK0 to SCK11 Value: Min - Max 5 (4-1-5)SCS↓⇒SCK↓ setup time t_{CSSI} (4-1-6)SCS↓⇒SCK↑ setup time t_{CSSI} (4-1-7)SCS↑⇒SCK↓ setup time t_{CSSI} (4-1-8)SCS↑⇒SCK↑ setup time t_{CSSI} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSSU}+0 Max t_{CSSU}+50 ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSSU}-50 Max t_{CSSU}+0 Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min t_{CSSU}-50 Max t_{CSSU}+300