Infineon Technologies - MB91F523FWCPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

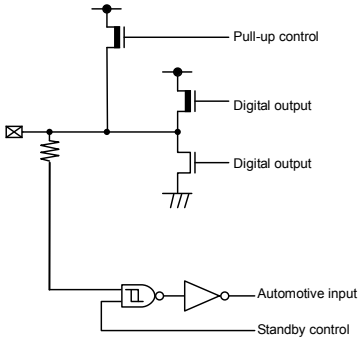
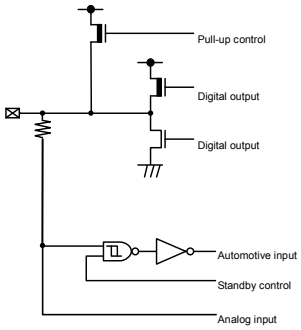
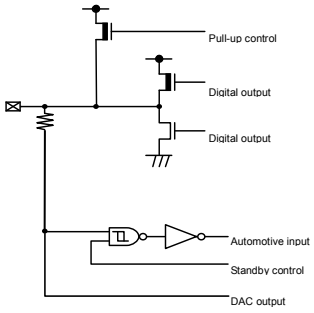
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f523fwcpmc-gse1

- D/A converter (R-2R type)
  - 8-bit resolution : 2ch
- External interrupt input: 8 channels × 2 units total 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max.12 channels
  - 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
    < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detection functions provided
  - DMA transfer support
    <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detection function is provided
  - DMA transfer support
  - Serial chip select SPI function
    <LIN (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - LIN protocol revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support
  - Hard assist function
    < I^2C >
  - 2 channels ch.3 , ch.4 Standard mode/fast mode supported.
  - 6 channels ch.5 to ch.8, ch.10, ch.11 Standard mode supported.
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (CAN) : 3 channels
  - Transfer speed : Up to 1Mbps
  - 128-transmission/reception message buffering :
    1 channel (ch.0),
    64-transmission/reception message buffering :
    2 channels (ch.1 and ch.2)
- PPG: 16-bit × Max. 48 channels
  - LED drive output 4 channels 11ch to 14ch
  - Reload timer : 16-bit × Max.8 channels
  - Free-run timer :
    16-bit × 3 channels
    32-bit × Max 3 channels
- Input capture :
  16-bit × 4 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Output compare :
  16-bit × 6 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Waveform generator : 6 channels
- Up/Down counter
  - 8/16-bit Up/Down counter × 2 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main or sub oscillation frequency can be selected for the operation clock
- Calibration: Real-time clock (RTC) of the subclock drive
  - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (by damaged quartz, etc.) of suboscillation (32kHz) (dual clock products) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
  - Initial value ON/OFF can be selected by the part number.
- Base timer : Max.2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascade mode
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog (possible to set the valid range for counter clearing)
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
  - The interrupt existence from two or more peripherals can be read by a series of register.
- I/O relocation
  - Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode

4. I/O Circuit Type

Type	Circuit	Remarks
A		•General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input
B		•Analog input, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input
C		•DAC output, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0008A0_H$	WRAR04 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
$0008A4_H$	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C8_H$	WRAR09 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008CC_H$	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0013E8_H$	ADTECS14[R/W] B,H,W -------0 ---00000		ADTECS15[R/W] B,H,W -------0 ---00000		12-bit A/D converter 1/2 unit
$0013EC_H$	ADTECS16[R/W] B,H,W -------0 ---00000		ADTECS17[R/W] B,H,W -------0 ---00000		
$0013F0_H$	ADTECS18[R/W] B,H,W -------0 ---00000		ADTECS19[R/W] B,H,W -------0 ---00000		
$0013F4_H$	ADTECS20[R/W] B,H,W -------0 ---00000		ADTECS21[R/W] B,H,W -------0 ---00000		
$0013F8_H$	ADTECS22[R/W] B,H,W -------0 ---00000		ADTECS23[R/W] B,H,W -------0 ---00000		
$0013FC_H$	ADTECS24[R/W] B,H,W -------0 ---00000		ADTECS25[R/W] B,H,W -------0 ---00000		
001400_H	ADTECS26[R/W] B,H,W -------0 ---00000		ADTECS27[R/W] B,H,W -------0 ---00000		
001404_H	ADTECS28[R/W] B,H,W -------0 ---00000		ADTECS29[R/W] B,H,W -------0 ---00000		
001408_H	ADTECS30[R/W] B,H,W -------0 ---00000		ADTECS31[R/W] B,H,W -------0 ---00000		
$00140C_H$	ADRCUT0[R/W] B,H,W ----0000 00000000		ADRCLT0[R/W] B,H,W ----0000 00000000		
001410_H	ADRCUT1[R/W] B,H,W ----0000 00000000		ADRCLT1[R/W] B,H,W ----0000 00000000		
001414_H	ADRCUT2[R/W] B,H,W ----0000 00000000		ADRCLT2[R/W] B,H,W ----0000 00000000		
001418_H	ADRCUT3[R/W] B,H,W ----0000 00000000		ADRCLT3[R/W] B,H,W ----0000 00000000		
$00141C_H$	ADRCCS0[R/W] B,H,W 00000000	ADRCCS1[R/W] B,H,W 00000000	ADRCCS2[R/W] B,H,W 00000000	ADRCCS3[R/W] B,H,W 00000000	
001420_H	ADRCCS4[R/W] B,H,W 00000000	ADRCCS5[R/W] B,H,W 00000000	ADRCCS6[R/W] B,H,W 00000000	ADRCCS7[R/W] B,H,W 00000000	
001424_H	ADRCCS8[R/W] B,H,W 00000000	ADRCCS9[R/W] B,H,W 00000000	ADRCCS10[R/W] B,H,W 00000000	ADRCCS11[R/W] B,H,W 00000000	
001428_H	ADRCCS12[R/W] B,H,W 00000000	ADRCCS13[R/W] B,H,W 00000000	ADRCCS14[R/W] B,H,W 00000000	ADRCCS15[R/W] B,H,W 00000000	
$00142C_H$	ADRCCS16[R/W] B,H,W 00000000	ADRCCS17[R/W] B,H,W 00000000	ADRCCS18[R/W] B,H,W 00000000	ADRCCS19[R/W] B,H,W 00000000	
001430_H	ADRCCS20[R/W] B,H,W 00000000	ADRCCS21[R/W] B,H,W 00000000	ADRCCS22[R/W] B,H,W 00000000	ADRCCS23[R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001804_H	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001808_H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
$00180C_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810_H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814_H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818_H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00181C_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820_H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824_H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828_H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
$00182C_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830_H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834_H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838_H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
$00183C_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

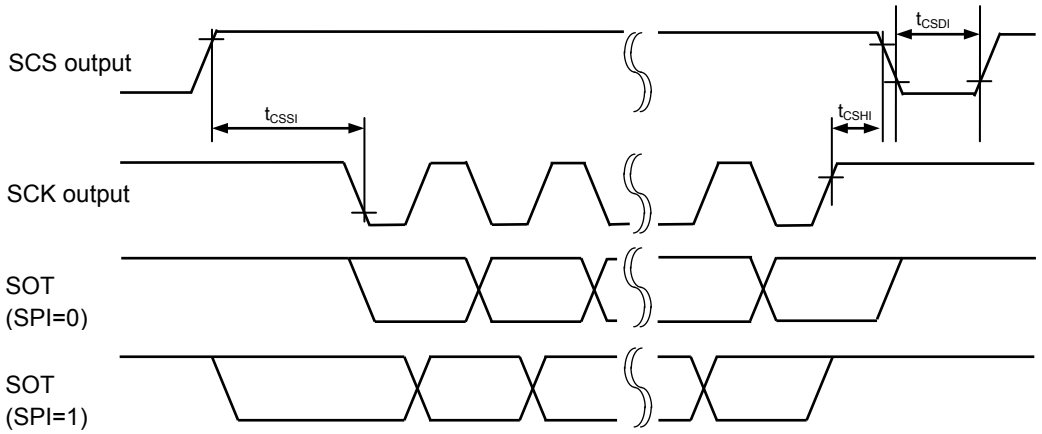
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001D70$_H$ to 001FFC$_H$	—	—	—	—	Reserved
002000$_H$	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0 [R/W] B,H,W -------- 00000000		CAN0 (128msb)
002004$_H$	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W -0100011 00000001		
002008$_H$	INTR0 [R] B,H,W 00000000 00000000		TESTR0 [R/W] B,H,W -------- X00000--		
00200C$_H$	BRPER0 [R/W] B,H,W -------- ----0000		—	—	
002010$_H$	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014$_H$	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018$_H$	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00201C$_H$	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002020$_H$	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
002024$_H$	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028$_H$	—	—	—	—	
00202C$_H$	—	—	—	—	
002030$_H$, 002034$_H$	Reserved(IF1 data mirror)				
002038$_H$	—	—	—	—	
00203C$_H$	—	—	—	—	
002040$_H$	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044$_H$	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048$_H$	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
00204C$_H$	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002050$_H$	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed) / Multi-function serial interface ch.4 (status)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed) / Multi-function serial interface ch.5 (status)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed) / Multi-function serial interface ch.6 (status)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1 / RAM diagnosis end / RAM initialization completion / Error generation during RAM diagnosis / Backup RAM diagnosis end / Backup RAM initialization completion / Error generation during Backup RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-
CAN2 / Up/down counter 0 / Up/down counter 1	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed) / Multi-function serial interface ch.7 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*1
16-bit Free-running timer 0 (0 detection) / (compare clear) / Multi-function serial interface ch.7 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/21/30/31 / 16-bit Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
PPG 2/3/12/13/23/32/43 / 16-bit Free-run timer 2 (0 detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*3
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3

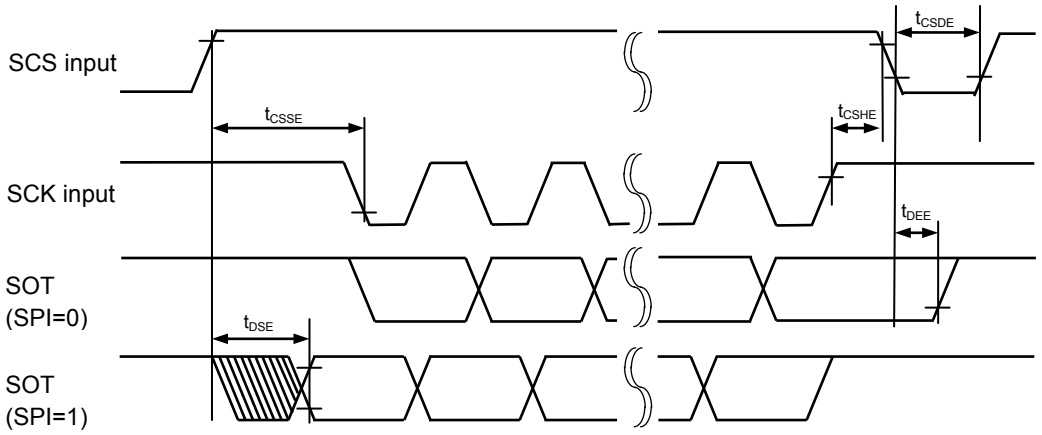
(4-1-3) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=0, SCR:SPI=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
SOT→SCK↓ delay time	t_{SOVLI}	SCK0 to SCK11 SOT0 to SOT11		$2t_{CPP}$ -30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+ 10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$ -10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
External shift clock mode

(4-1-8) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used: SCSCR:CSEN=1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↓→SCS↓ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	

Flash memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbytes sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbytes sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbytes sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbytes sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A=+85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.

In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc at 2.7V or more within the duration calculated by the following expression:

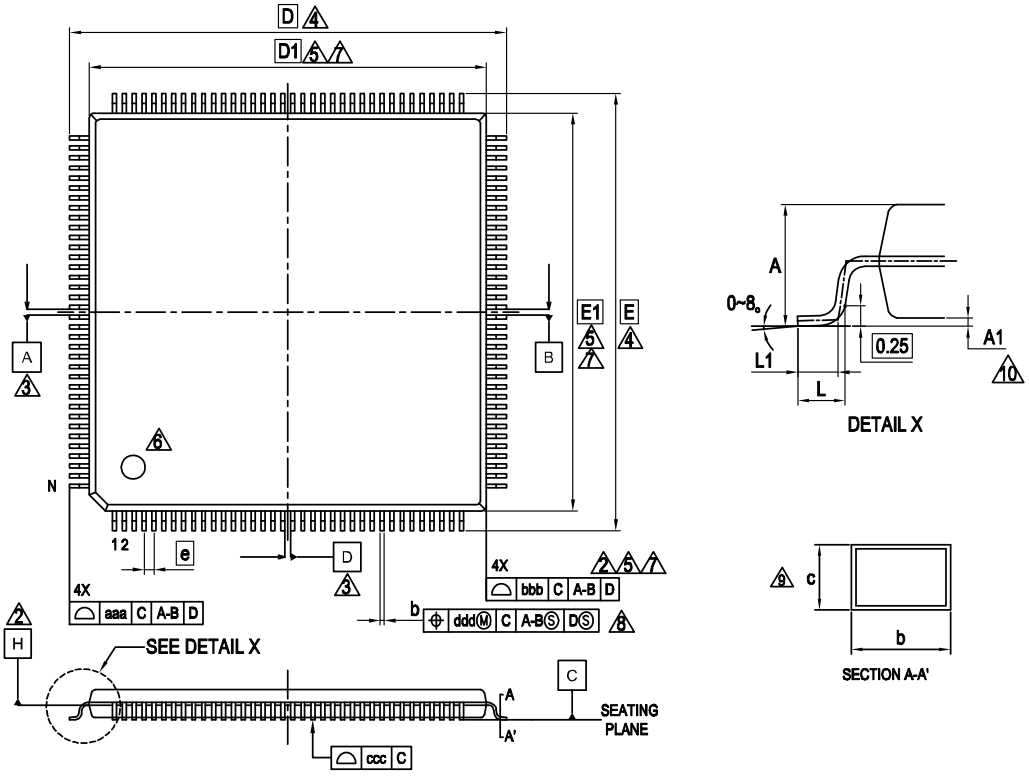
$$Td^{*}[\mu s] + (\text{period of PCLK } [\mu s] \times 257) + 50\ [\mu s]$$

*: See “4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) ”

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYBPMC1			OFF	
MB91F526KJBPMC1		OFF	ON	
MB91F526KLBPMC1			OFF	
MB91F525KWBPMC1		ON	ON	
MB91F525KYBPMC1			OFF	
MB91F525KJBPMC1		OFF	ON	
MB91F525KLBPMC1			OFF	
MB91F524KWBPMC1		ON	ON	
MB91F524KYBPMC1			OFF	
MB91F524KJBPMC1		OFF	ON	
MB91F524KLBPMC1			OFF	
MB91F523KWBPMC1		ON	ON	
MB91F523KYBPMC1			OFF	
MB91F523KJBPMC1		OFF	ON	
MB91F523KLBPMC1			OFF	
MB91F522KWBPMC1		ON	ON	
MB91F522KYBPMC1			OFF	
MB91F522KJBPMC1		OFF	ON	
MB91F522KLBPMC1			OFF	
MB91F526KSBPMC1	None	ON	ON	
MB91F526KUBPMC1			OFF	
MB91F526KHBPMC1		OFF	ON	
MB91F526KKBPMC1			OFF	
MB91F525KSBPMC1		ON	ON	
MB91F525KUBPMC1			OFF	
MB91F525KHBPMC1		OFF	ON	
MB91F525KKBPMC1			OFF	
MB91F524KSBPMC1		ON	ON	
MB91F524KUBPMC1			OFF	
MB91F524KHBPMC1		OFF	ON	
MB91F524KKBPMC1			OFF	
MB91F523KSBPMC1		ON	ON	
MB91F523KUBPMC1			OFF	
MB91F523KHBPMC1		OFF	ON	
MB91F523KKBPMC1			OFF	
MB91F522KSBPMC1		ON	ON	
MB91F522KUBPMC1			OFF	
MB91F522KHBPMC1		OFF	ON	
MB91F522KKBPMC1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWEPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FJEPMC		OFF	ON	
MB91F525FWEPMC		ON	ON	
MB91F525FJEPMC		OFF	ON	
MB91F524FWEPMC		ON	ON	
MB91F524FJEPMC		OFF	ON	
MB91F523FWEPMC		ON	ON	
MB91F523FJEPMC		OFF	ON	
MB91F522FWEPMC		ON	ON	
MB91F522FJEPMC		OFF	ON	
MB91F526FSEPMC	None	ON	ON	
MB91F526FHEPMC		OFF	ON	
MB91F525FSEPMC		ON	ON	
MB91F525FHEPMC		OFF	ON	
MB91F524FSEPMC		ON	ON	
MB91F524FHEPMC		OFF	ON	
MB91F523FSEPMC		ON	ON	
MB91F523FHEPMC		OFF	ON	
MB91F522FSEPMC		ON	ON	
MB91F522FHEPMC		OFF	ON	
MB91F526DWEPMC	Yes	ON	ON	LQH・80 pin, Plastic
MB91F526DJEPMC		OFF	ON	
MB91F525DWEPMC		ON	ON	
MB91F525DJEPMC		OFF	ON	
MB91F524DWEPMC		ON	ON	
MB91F524DJEPMC		OFF	ON	
MB91F523DWEPMC		ON	ON	
MB91F523DJEPMC		OFF	ON	
MB91F522DWEPMC		ON	ON	
MB91F522DJEPMC		OFF	ON	
MB91F526DSEPMC	None	ON	ON	
MB91F526DHEPMC		OFF	ON	
MB91F525DSEPMC		ON	ON	
MB91F525DHEPMC		OFF	ON	
MB91F524DSEPMC		ON	ON	
MB91F524DHEPMC		OFF	ON	
MB91F523DSEPMC		ON	ON	
MB91F523DHEPMC		OFF	ON	
MB91F522DSEPMC		ON	ON	
MB91F522DHEPMC		OFF	ON	

LQS144 , 144 Lead Plastic Low Profile Quad Flat Package



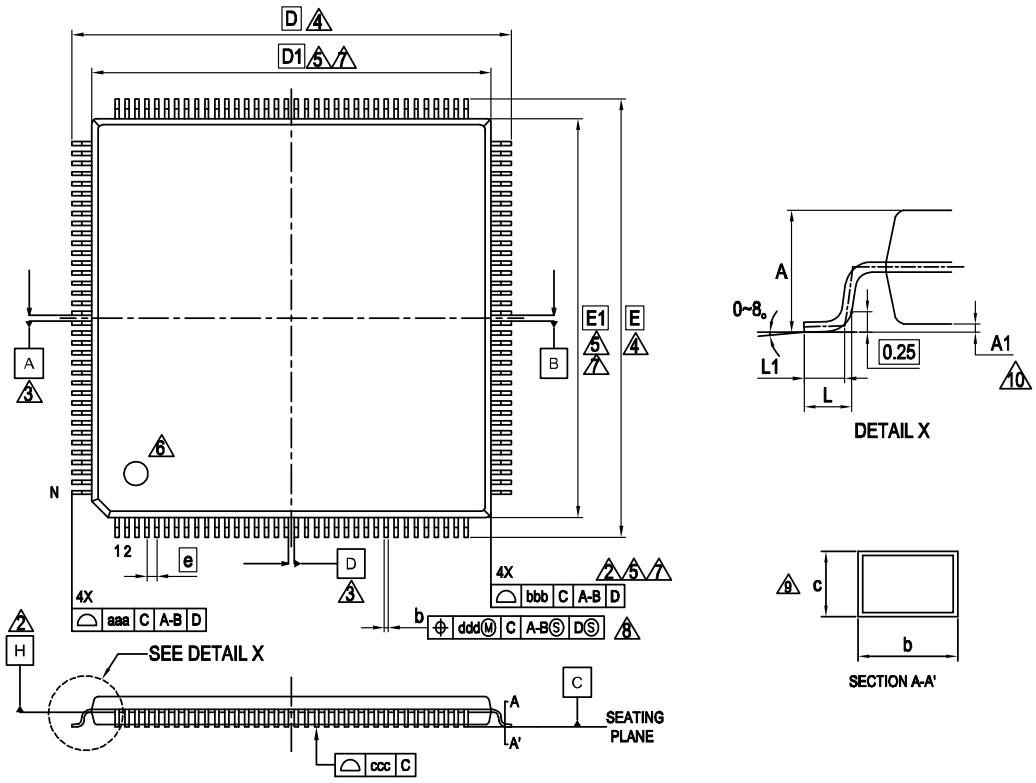
PACKAGE	LQS144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.06	—	0.26
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC.		
D1	20.00 BSC.		
e	0.50 BSC		
E	22.00 BSC.		
E1	20.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQN144 , 144 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQN144		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.145	0.18	0.215
c	0.115	——	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.40 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.07
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

■ **Scope of Impact**

For the affected parts, when the Power-On Reset and Internal Low Voltage Detection are not generated, the MCU may set invalid package and sub clock option information. Therefore, the MCU may operate with an invalid pin configuration.

■ **Workaround**

For the affected parts, it is necessary to satisfy at least one of the Power-On Reset requirements for any Power-On event as given below:

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate is less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

If the customer system does not satisfy the condition above-mentioned, Cypress will releases new version D, so Cypress recommends the version D for MB91F52x. The new version prevents the limitation when an external reset signal is asserted at pin RSTX anytime the supply voltage (VCC) is turned on.

■ **Fix Status**

Will be fixed in production silicon version D, E

2. Limitation for Watch mode (power off)

■ **Problem Definition**

If the below all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

■ **Trigger Conditions**

(1) Using the watch mode (power off)

(2) Interrupt levels that are used as sources for recovering from the watch mode (power off) are ‘16’ to ‘30’, or using NMIX pin as source for recovering from the watch mode (power off)

(3) The sources for recovering from the watch mode (power off) are generated between PCLK 1 cycle and PMUCLK 3 cycles (*), after CPU state changes to the watch mode (power off)
(*): In case of PCLK = 0.5 MHz and PMUCLK = 32 kHz, it is approx. 2 µs to 100 µs

■ **Scope of Impact**

If the all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

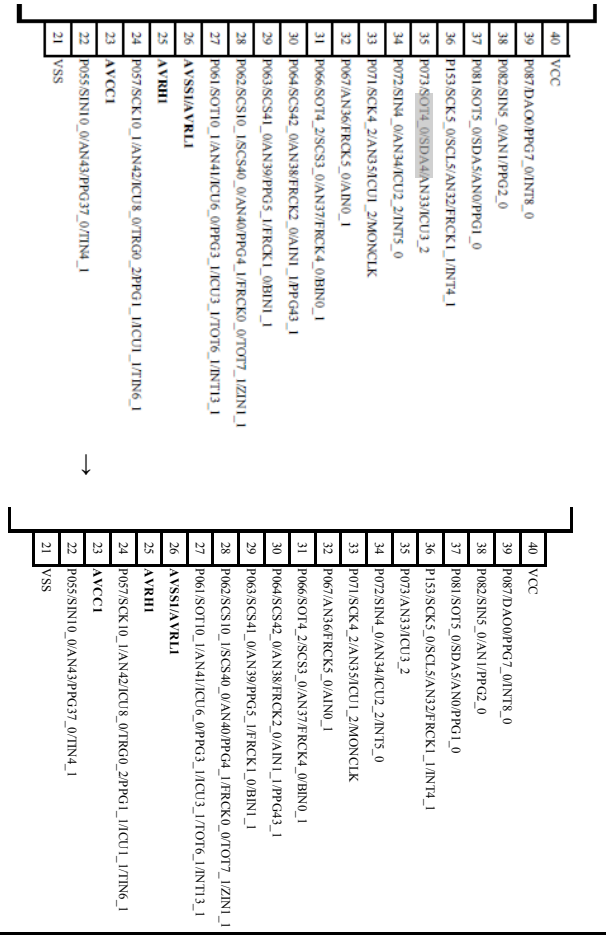
WTCRH, WTCRM, WTCRL

CSELR.SCEN

CMONR.SCRDY

CCRTSELR.CST

CCRTSELR.CSC

Page	Section	Change Results
14	■Pin Assignment MB91F52xD	- Bottom 

Page	Section	Change Results
19	■PIN Description	(Continued) (Correct)

Pin no.						Pin Name
64	80	100	120	144	176	
-	-	-	-	2	2	P015 D29 TRG0_0
-	-	-	-	3	3	P016 D30 TRG1_0
-	-	-	-	-	4	P170 PPG36_1
-	-	-	-	4	5	P017 D31 TRG2_0
-	-	-	-	-	6	P171 PPG37_1
2 *1	2 *1	2 *1	2 *1	5	7	P020 ASX *2, *3, *4, *5 SIN3_1 TRG3_0 TIN0_2 RTO5_1
-	-	-	3 *1	6	8	P021 CS0X *5 SOT3_1 TRG6_1 TRG4_0
-	-	-	4 *1	7	9	P022 CS1X *5 SCK3_1 TRG7_1 TRG5_0
-	-	-	5 *1	8	10	P023 RDX *5 SCS3_1 PPG32_0 TIN0_0
3 *1	3 *1	3 *1	6 *1	9	11	P024 WR0X *2, *3, *4, *5 SIN4_1 PPG24_0 TIN1_0 RTO4_1 INT15_0

Page	Section	Change Results
46	■During Power-on	The following sentence modified as following: (Error) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.
142,143	11. Electrical Characteristics Recommended operating conditions	The following sentence modified as following: (Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset. (Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
156, 157	11. Electrical Characteristics AC Characteristics	Added (3-2) Power-on Conditions for MB91F52xxxE