

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f523fwcpmc-gse1

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

MB91520 Series



- D/A converter (R-2R type)
 8-bit resolution : 2ch
- External interrupt input: 8 channels × 2 units total 16 channels
 - Level ("H" / "L"), or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max.12 channels
 - 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
 VART (Asynchronous serial interface) >
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - □ Parity or no parity is selectable.
 - □ Built-in dedicated baud rate generator
 - □ An external clock can be used as the transfer clock
 - □ Parity, frame, and overrun error detection functions provided
 - DMA transfer support
 <CSIO (Synchronous serial interface) >
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - □ SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
 - Built-in dedicated baud rate generator (Master operation)
 - □ An external clock can be entered. (Slave operation)
 - □ Overrun error detection function is provided
 - DMA transfer support
 - Serial chip select SPI function <LIN (Asynchronous Serial Interface for LIN) >
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - □ LIN protocol revision 2.1 supported
 - □ Master and slave systems supported
 - □ Framing error and overrun error detection
 - □ LIN synch break generation and detection; LIN synch delimiter generation
 - □ Built-in dedicated baud rate generator
 - An external clock can be adjusted by the reload counter
 - DMA transfer support
 - $\square \quad \text{Hard assist function} \\ < |^2C >$
 - □ 2 channels ch.3 , ch.4 Standard mode/fast mode supported.
 - 6 channels ch.5 to ch.8, ch.10, ch.11 Standard mode supported.
 - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
 - □ Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported
 - DMA transfer supported (for transmission only)
- CAN Controller (CAN) : 3 channels
 - □ Transfer speed : Up to 1Mbps
 - □ 128-transmission/reception message buffering : 1 channel (ch.0),

64-transmission/reception message buffering : 2 channels (ch.1 and ch.2)

- PPG: 16-bit × Max. 48 channels
 - □ LED drive output 4 channels 11ch to 14ch
 - □ Reload timer : 16-bit × Max.8 channels
 - Free-run timer : 16-bit × 3 channels 32-bit × Max 3 channels
- Input capture : 16-bit × 4 channels (linked to the free-run timer) 32-bit × Max 6 channels (linked to the free-run timer)
- Output compare : 16-bit × 6 channels (linked to the free-run timer) 32-bit × Max 6 channels (linked to the free-run timer)
- Waveform generator : 6 channels
- Up/Down counter
 - □ 8/16-bit Up/Down counter × 2 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
 Main or sub oscillation frequency can be selected for the operation clock
- Calibration: Real-time clock (RTC) of the subclock drive
 The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
 - Monitoring abnormality (by damaged quartz, etc.) of suboscillation (32kHz) (dual clock products) of the outside and main oscillation (4 MHz)
 - □ When abnormality is detected, it switches to the CR clock.
 - □ Initial value ON/OFF can be selected by the part number.
- Base timer : Max.2 channels
 - □ 16-bit timer
 - □ Any of four PWM/PPG/PWC/reload timer functions can be selected and used
 - □ As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascade mode
- CRC generation
- Watchdog timer
 - □ Hardware watchdog
 - Software watchdog (possible to set the valid range for counter clearing)
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
 - □ The interrupt existence from two or more peripherals can be read by a series of register.
- I/O relocation
 - □ Peripheral function pins can be reassigned.
- Low-power consumption mode
 - □ Sleep / Stop / Watch / Sub RUN mode
 - Stop (power shutdown) / Watch (power shutdown) mode



4. I/O Circuit Type

Туре	Circuit	Remarks
A	Pull-up control	•General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input
В	Pull-up control Digital output Digital output TH Digital output Automotive input Analog input	 Analog input, General-purpose I/O port Output 4mA Pull-up resistor control 50kΩ Automotive input
С	Pul-up control Digital output Digital output T// Digital output T// Digital output Standby control DAC output	 •DAC output, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •Automotive input



5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.



	Address offset value / Register name					
Address	+0	+1	+2	+3	- Block	
0008A0 _H		WRAR(04 [R/W] W XXXXXXXX XXXXXX-	-		
0008A4 _H		WRDRO XXXXXXXX XXXXXXX	04 [R/W] W X XXXXXXX XXXX	xxx		
0008A8 _H		WRAR(XXXXXX >	05 [R/W] W (XXXXXXX XXXXXX-	-		
0008AC _H		WRDRO XXXXXXXX XXXXXXX	05 [R/W] W X XXXXXXX XXXX	xxx		
0008B0 _H		WRAR(XXXXXX >	06 [R/W] W XXXXXXXX XXXXXX-	-	_	
0008B4 _H		WRDR(XXXXXXXX XXXXXXX	06 [R/W] W X XXXXXXX XXXX	xxx		
0008B8 _H		WRAR(XXXXXX >)7 [R/W] W (XXXXXXX XXXXXX-	-		
0008BC _н		WRDR(XXXXXXXX XXXXXXX	07 [R/W] W X XXXXXXXX XXXX	xxx		
0008C0 _H		WRAR(XXXXXX >	08 [R/W] W (XXXXXXX XXXXXX-	-]	
0008C4 _H		WRDRO XXXXXXXX XXXXXXX	08 [R/W] W X XXXXXXXX XXXX	xxx		
0008C8 _H		WRAR09 [R/W] W XXXXXX XXXXXXX XXXXXX				
0008CC _н		WRDR(XXXXXXXX XXXXXXX	09 [R/W] W X XXXXXXXX XXXX	xxx		
0008D0 _H		WRAR XXXXXX >	10 [R/W] W (XXXXXXX XXXXXX-	-		
0008D4 _H		WRDR ⁻ XXXXXXXX XXXXXXX	10 [R/W] W X XXXXXXX XXXX	xxx	_	
0008D8 _H		WRAR XXXXXX >	11 [R/W] W XXXXXXXX XXXXXX-		_	
0008DC _H		WRDR XXXXXXXX XXXXXXX	11 [R/W] W X XXXXXXXX XXXX	xxx		
0008E0 _H		-				
0008E4 _H		_				
0008E8 _H		WRAR? XXXXXX >	13 [R/W] W XXXXXXXX XXXXXX-		_	
0008EC _H		WRDR XXXXXXXX XXXXXXX	13 [R/W] W X XXXXXXXX XXXX	xxx	_	
0008F0 _H		WRAR ۲ ۲XXXXXX -	14 [R/W] W XXXXXXX XXXXXX-	-		





A d due e e	Address offset value / Register name					
Address	+0 +1 +2 +3				BIOCK	
0013E8 _Н	ADTECS14 0 -	R/W] B,H,W 00000	ADTECS15 0 -	[R/W] B,H,W 00000		
0013EC _н	ADTECS16 0 -	R/W] B,H,W 00000	ADTECS17 0 -	[R/W] B,H,W 00000		
0013F0 _Н	ADTECS18 0 -	R/W] B,H,W 00000	ADTECS19 0 -	[R/W] B,H,W 00000		
0013F4 _H	ADTECS20 0 -	R/W] B,H,W 00000	ADTECS21	[R/W] B,H,W 00000		
0013F8 _Н	ADTECS22 0 -	R/W] B,H,W 00000	ADTECS23	[R/W] B,H,W 00000		
0013FC _н	ADTECS24 0 -	R/W] B,H,W 00000	ADTECS25 0 -	[R/W] B,H,W 00000		
001400 _H	ADTECS26 0 -	R/W] B,H,W 00000	ADTECS27 0 -	[R/W] B,H,W 00000		
001404 _H	ADTECS28 0 -	R/W] B,H,W 00000	ADTECS29	[R/W] B,H,W 00000	-	
001408 _H	ADTECS30[R/W] B,H,W		ADTECS31[R/W] B,H,W 000000			
00140C _Н	ADRCUT0[R/W] B,H,W		ADRCLT0[R/W] B,H,W 0000 00000000		-	
001410 _H	ADRCUT1[R/W] B,H,W 0000 00000000		ADRCLT1[I 0000 (R/W] B,H,W 00000000	12-bit A/D converter 1/2 unit	
001414 _H	ADRCUT2[0000 (ADRCUT2[R/W] B,H,W 0000 00000000		R/W] B,H,W 00000000	-	
001418 _Н	ADRCUT3[0000 (R/W] B,H,W 00000000	ADRCLT3[I 0000 (R/W] B,H,W 20000000		
00141C _н	ADRCCS0[R/W] B,H,W 00000000	ADRCCS1[R/W] B,H,W 00000000	ADRCCS2[R/W] B,H,W 00000000	ADRCCS3[R/W] B,H,W 00000000		
001420 _Н	ADRCCS4[R/W] B,H,W 00000000	ADRCCS5[R/W] B,H,W 00000000	ADRCCS6[R/W] B,H,W 00000000	ADRCCS7[R/W] B,H,W 00000000		
001424 _H	ADRCCS8[R/W] B,H,W 00000000	ADRCCS9[R/W] B,H,W 00000000	ADRCCS10[R/W] B,H,W 00000000	ADRCCS11[R/W] B,H,W 00000000		
001428 _Н	ADRCCS12[R/W] B,H,W 00000000	ADRCCS13[R/W] B,H,W 00000000	ADRCCS14[R/W] B,H,W 00000000	ADRCCS15[R/W] B,H,W 00000000		
00142C _н	ADRCCS16[R/W] B,H,W 00000000	ADRCCS17[R/W] B,H,W 00000000	ADRCCS18[R/W] B,H,W 00000000	ADRCCS19[R/W] B,H,W 00000000		
001430 _н	ADRCCS20[R/W] B,H,W 00000000	ADRCCS21[R/W] B,H,W 00000000	ADRCCS22[R/W] B,H,W 00000000	ADRCCS23[R/W] B,H,W 00000000		



Addroop	Address offset value / Register name					
Address	+0	+1	+2	+3	DIOCK	
001804 _Н	_	— /(SCSFR24) [R/W] B,H,W *3	— /(SCSFR14) [R/W] B,H,W *3	— /(SCSFR04) [R/W] B,H,W ^{*3}	Multi-UART4	
001808 _Н	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W ^{*3}	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W ^{*3}	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	*3: Reserved because CSIO mode is not set immediately after reset.	
00180Cн	BGR4[R/ 00000000	W] H, W 00000000	— /(ISMK4)[R/W] B,H,W ^{*2}	— /(ISBA4)[R/W] B,H,W ^{*2}	*4: Reserved because LIN2.1	
001810 _н	FCR14[R/W] B,H,W 00100	FCR04[R/W] B,H,W -0000000	FBYTE4[F 00000000	2/W] B,H,W 00000000	mode is not set immediately after reset.	
001814 _H	FTICR4[R 00000000	W] B,H,W 00000000	—	—		
001818 _Н	SCR5/(IBCR5) [R/W] B,H,W 000000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000		
00181C _H	— /(RDR15/(TDR 	215))[R/W] B,H,W ^{*3}	RDR05/(TDR0 0 00	5)[R/W] B,H,W 0000000 ^{*1}	Multi-UART5	
001820 _H	SACSR5[R 0000 (2/W] B,H,W 00000000	STMR5[00000000	R] B,H,W 00000000	*1: Byte access is possible only for	
001824 _H	STMCR5[F 00000000	2/W] B,H,W 00000000	— /(SCSCR5/SF	UR5)[R/W] B,H,W ^{*3 *4}	access to lower 8 bits.	
001828 _Н	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W	*2: Reserved because I ² C mode is not set	
00182C _Н	_	— /(SCSFR25) [R/W] B,H,W ^{*3}	— /(SCSFR15) [R/W] B,H,W *3	— /(SCSFR05) [R/W] B,H,W *3	reset. *3: Reserved	
001830 _H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W ^{*3}	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W ^{*3}	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W ^{*3}	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	because CSIO mode is not set immediately after reset.	
001834 _Н	BGR5[R/ 00000000	W] H, W 00000000	— /(ISMK5)[R/W] B,H,W ^{*2}	SMK5)[R/W] /(ISBA5)[R/W] B,H,W B,H,W *2 *2		
001838 _H	FCR15[R/W] B,H,W 00100	FCR05[R/W] B,H,W -0000000	FBYTE5[F 00000000	2/W] B,H,W 00000000	reset.	
00183C _Н	FTICR5[R 00000000	W] B,H,W 00000000	_	_		





	Address offset value / Register name					
Address	+0	+1	+2	+3	– Block	
001D70 _н to 001FFC _H	_	_	_	_	Reserved	
002000 _H	CTRLR0 [F 0	R/W] B,H,W 000-0001	STATR0	[R/W] B,H,W - 00000000		
002004 _H	ERRCNT0 00000000) [R] B,H,W 00000000	BTR0 [-01000	R/W] B,H,W 11 00000001		
002008 _H	INTR0 [I 00000000	R] B,H,W 00000000	TESTRO) [R/W] B,H,W - X00000		
00200C _H	BRPER0 [I	R/W] B,H,W 0000	_	_		
002010 _H	IF1CREQ0 00	[R/W] B,H,W 0000001	IF1CMSK	0 [R/W] B,H,W - 00000000		
002014 _H	IF1MSK20 11-11111	[R/W] B,H,W 11111111	IF1MSK1 111111	0 [R/W] B,H,W 11 1111111		
002018 _Н	IF1ARB20 00000000	[R/W] B,H,W 00000000	IF1ARB1 000000	0 [R/W] B,H,W 00 0000000		
00201C _H	IF1MCTR0 0000000	[R/W] B,H,W 0 00000	_	_		
002020 _Н	IF1DTA10 [00000000	R/W] B,H,W 00000000	IF1DTA2 000000	0 [R/W] B,H,W 00 0000000		
002024 _H	IF1DTB10 [00000000	R/W] B,H,W 00000000	IF1DTB2 000000	0 [R/W] B,H,W 00 00000000	CAN0 (128msb)	
002028 _Н	_	_	_	_		
00202C _Н	_	—	_	—		
002030 _н , 002034 _Н		Reserved(IF	1 data mirror)	_		
002038 _Н	—	—	—	—		
00203C _Н	—	—	—	—		
002040 _Н	IF2CREQ0 [R/W] B,H,W 0 00000001		IF2CMSK0 [R/W] B,H,W 00000000			
002044 _Н	IF2MSK20 [R/W] B,H,W 11-11111 1111111		IF2MSK1 111111	0 [R/W] B,H,W 11 1111111		
002048 _Н	IF2ARB20 00000000	[R/W] B,H,W 00000000	IF2ARB1 000000	0 [R/W] B,H,W 00 00000000		
00204C _Н	IF2MCTR0 0000000	[R/W] B,H,W 0 00000	_	—		
002050 _Н	IF2DTA10 [00000000	R/W] B,H,W 00000000	IF2DTA2 000000	0 [R/W] B,H,W 00 00000000		



Interrupt factorDecimalHexadecimalIntervelOffset address for RN TRRNull-function serial interface c.h.4 (transmission completed)271BICR11390,000FFF90,11Multi-function serial interface c.h.4 (transmission completed)281CICR1238C,000FFF8C,12.1Multi-function serial interface c.h.4 (transmission completed)291DICR13388,000FFF8C,13Multi-function serial interface c.h.5 (reception completed)301EICR14380,000FFF8C,14.1Multi-function serial interface c.h.5 (reception completed)311FICR15380,000FFF8C,15Multi-function serial interface c.h.6 (transmission completed)311FICR1637C,000FFF8C,16.1Multi-function serial interface c.h.6 (transmission completed)3321ICR1637C,000FFF7C,16.1Multi-function serial interface c.h.6 (transmission completed)3321ICR1637H,000FFF7A,17CAN1CAN13622ICR1837H,000FFF7A,11CAN1CAN13622ICR1837H,000FFF6C,1CAN1CAN13826ICR2036H,000FFF6C,2CAN2CAN2Generation during RAM diagnosis3826ICR2136H,000FFF6C,2CAN1CAN13826ICR2236H,000FFF6C,221 <th></th> <th colspan="2">Interrupt number</th> <th>Interrunt</th> <th></th> <th>Default</th> <th></th>		Interrupt number		Interrunt		Default	
Null-function serial interface ch.4 (transmission completed) 27 1B ICR11 390, 000FFF90, 11 000FFF90, 12 11 Mull-function serial interface ch.4 (transmission completed) 28 1C ICR12 38C, 000FFF80, 12 000FFF80, 12 12 Mull-function serial interface ch.4 (transmission completed) 29 1D ICR13 388, 000FFF80, 14 000FFF80, 14 14 Mull-function serial interface ch.5 (reception completed) 30 1E ICR14 380, 000FFF80, 15 000FFF80, 15 15 Mull-function serial interface ch.5 (reception completed) 31 1F ICR16 37C, 16 000FFF80, 37C, 16 15 Mull-function serial interface ch.6 (reception completed) 33 21 ICR16 37C, 16 000FFF70, 17 16 AM diagnosis end Error generation during RAM diagnosis Error generation during RAM diagnosis end Error generation m	Interrupt factor	Decimal	Hexadecimal	level	Offset	address for TBR	RN
ch.3 (transmission completed) 27 1B ICR11 390+ 000FFF80+ 11 Multi-function serial interface ch.4 (teception completed) 28 1C ICR12 38C+ 000FFF80+ 12* Multi-function serial interface 29 1D ICR13 388+ 000FFF80+ 13 Multi-function serial interface 29 1D ICR13 388+ 000FFF80+ 14* Multi-function serial interface 30 1E ICR14 384+ 000FFF80+ 15 Multi-function serial interface 31 1F ICR15 380+ 000FFF80+ 15 Multi-function serial interface 32 20 ICR16 37C+ 000FFF70+ 16*1 Multi-function serial interface 33 21 ICR16 374+ 000FFF70+ - CAN0 34 22 ICR18 374+ 000FFF70+ - RAM diagnosis end 36 24 ICR20 36C+ 000FFF70+ - Read time clock	Multi-function serial interface	07	45	10044	000	00055500	
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	ch.3 (transmission completed)	27	IB	ICRIT	390 _H	000FFF90H	11
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Multi-function serial interface						
Multi-function serial interface 28 1C ICR12 38C _H 000FFF8C _H 12* Multi-function serial interface 29 1D ICR13 388 _H 000FFF86 _H 13 Multi-function serial interface 30 1E ICR14 384 _H 000FFF86 _H 14* Auti-function serial interface 30 1E ICR15 380 _H 000FFF86 _H 15 Multi-function serial interface 31 1F ICR16 37C _H 000FFF86 _H 15 Multi-function serial interface 31 1F ICR16 37C _H 000FFF76 _H 16* ch.6 (reception completed) 32 20 ICR16 37C _H 000FFF76 _H 16* whulti-function serial interface 33 21 ICR17 378 _H 000FFF76 _H 17 CAN1 RAM initialization completion 33 23 ICR19 370 _H 000FFF76 _H - RAM initialization completion 36 24 ICR20 366 _H 000FFF66 _H -	ch.4 (reception completed)		10	10040		00055500	10+1
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Multi-function serial interface	28	1C	ICR12	38C ^H	000FFF8C _H	12*
Multi-function serial interface ch.4 (transmission completed) 29 1D ICR13 388 _H 000FFF88 _H 13 Multi-function serial interface ch.5 (status) 30 1E ICR14 384 _H 000FFF84 _H 14* Multi-function serial interface ch.5 (status) 31 1F ICR15 380 _H 000FFF84 _H 15 Multi-function serial interface ch.6 (status) 32 20 ICR16 37C _H 000FFF76 _H 16* ¹ Multi-function serial interface ch.6 (status) 32 20 ICR18 37C _H 000FFF76 _H 16* ¹ Multi-function serial interface ch.6 (status) 33 21 ICR18 37C _H 000FFF76 _H 17 CAN1 RAM diagnosis end 34 22 ICR18 37d _H 000FFF70 _H - Backup RAM diagnosis end 35 23 ICR19 370 _H 000FFF64 _H - Up/down counter 0 36 24 ICR20 36C _H 000FFF64 _H - Up/down counter 1 39 27 ICR21	ch.4 (status)						
ch.4 (transmission completed) 29 10 ICR13 388, 000FFR8,, 13 Multi-function serial interface	Multi-function serial interface		45	10040		00055500	40
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	ch.4 (transmission completed)	29	1D	ICR13	388 ^H	000FFF88H	13
ch.5 (reception completed) 30 1E ICR14 384,n 000FFF84,n 14*1 Multi-function serial interface 31 1F ICR15 380,n 000FFF84,n 15 Multi-function serial interface 31 1F ICR16 380,n 000FFF84,n 15 Multi-function serial interface 32 20 ICR16 37C,n 000FFF7C,n 16*1 Auti-function serial interface 33 21 ICR17 37B,n 000FFF7C,n 16*1 A.6. (status) 34 22 ICR18 374,n 000FFF7C,n 16*1 A.6. (status) 34 22 ICR18 374,n 000FFF7C,n 1 CAN0 34 22 ICR18 374,n 000FFF7C,n - RAM initialization completion 35 23 ICR19 370,n 000FFF7C,n - Backup RAM diagnosis end 36 24 ICR20 36C,n 000FFF6C,n - Up/down counter 1 0 38 26<	Multi-function serial interface						
Multi-function serial interface 30 TE ICR14 384 _H 000FFF84 _H 14* Audit-function serial interface 31 TF ICR15 380 _H 000FFF80 _H 15 Multi-function serial interface	ch.5 (reception completed)	20	45	10044	004	00055504	4 4 + 1
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Multi-function serial interface	30	IE	ICR14	384 _H	000FFF84 _H	14
Multi-function serial interface 31 1F ICR15 380+ 000FFF80+ 15 A.5 (transmission completed) 32 20 ICR16 37C+ 000FFF7C+ 16*1 Multi-function serial interface 33 21 ICR16 37C+ 000FFF7C+ 16*1 AMUIt-function serial interface 33 21 ICR17 378+ 000FFF7C+ 16*1 CAN0 34 22 ICR18 374+ 000FFF7C+ 1 CAN0 34 22 ICR18 374+ 000FFF7C+ 1 RAM diagnosis end 35 35 23 ICR19 370+ 000FFF7C+ 1 Backup RAM diagnosis end 36 24 ICR20 36C+ 000FFF6C+ 1 Backup RAM diagnosis end 37 25 ICR21 368+ 000FFF6C+ 1 Up/down counter 0 36 24 ICR20 36C+ 000FFF6C+ 2 Multi-function serial interface 37 25 ICR21	ch.5 (status)						
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Multi-function serial interface	24	45		200	00055500	45
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	ch.5 (transmission completed)	31	IF	ICRIS	380 _H	000FFF80H	15
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Multi-function serial interface						
Multi-function serial interface 32 20 ICR18 37CH 000FFF7CH 16 Multi-function serial interface 33 21 ICR17 378H 000FFF76H 17 CAN0 34 22 ICR18 374H 000FFF76H - CAN1	ch.6 (reception completed)	20	20		270	00055570	40*1
$\begin{array}{c c c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c c c c } \mbox{characle}{ \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Multi-function serial interface	32	20	ICRID	37 CH	UUUFFF7CH	10
Multi-function serial interface ch.6 (transmission completed) 33 21 ICR17 378 _H 000FFF78 _H 17 CAN0 34 22 ICR18 374 _H 000FFF78 _H - CAN0 34 22 ICR18 374 _H 000FFF78 _H - RAM diagnosis end 35 23 ICR19 370 _H 000FFF70 _H - Backup RAM initialization completion 36 24 ICR20 36C _H 000FFF6C _H - Error generation during Backup RAM diagnosis 36 24 ICR20 36C _H 000FFF6C _H - Up/down counter 0 10p/down counter 1 38 26 ICR21 368 _H 000FFF64 _H 22 ⁺¹ Multi-function serial interface 38 26 ICR22 364 _H 000FFF64 _H 22 ⁺¹ Multi-function serial interface 39 27 ICR23 360 _H 000FFF64 _H 23 6.7. (rtasmission completed) 40 28 ICR24 35C _H 000FFF56 _H 24 ⁺³ <td>ch.6 (status)</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	ch.6 (status)						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Multi-function serial interface	22	01		070	00055570	47
CAN0 34 22 ICR18 374 _H 000FFF74 _H - CAN1 RAM diagnosis end Addiagnosis Addiagnosis end Addiagnosis Addiagnosis Addiagnosis end Addiagnosis	ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78H	17
$ \begin{array}{ c c c c c c } \hline CAN1 & & & & & & & & & & & & & & & & & & &$	CAN0	34	22	ICR18	374 _Н	000FFF74 _H	-
RAM diagnosis end AM initialization completion AM initialization completion AM initialization completion ATT A completi	CAN1						
RAM initialization completion 35 23 ICR19 370 _H 000FFF70 _H - Backup RAM diagnosis end 36 23 ICR19 370 _H 000FFF70 _H - Backup RAM initialization completion 36 24 ICR19 370 _H 000FFF6C _H - Error generation during Backup RAM diagnosis 36 24 ICR20 36C _H 000FFF6C _H - Up/down counter 0 36 24 ICR20 36C _H 000FFF6C _H - Up/down counter 1 37 25 ICR21 368 _H 000FFF6A _H - Multi-function serial interface 37 25 ICR22 364 _H 000FFF6A _H 22*1 16-bit Free-running timer 0 (0 detection) / 38 26 ICR23 360 _H 000FFF60 _H 23 Multi-function serial interface 7 39 27 ICR23 360 _H 000FFF60 _H 23 6-bit Free-run timer 1 (0 detection) / 40 28 ICR24 35C _H 000FFF5C _H 24*3 <td>RAM diagnosis end</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	RAM diagnosis end						
Error generation during RAM diagnosis 35 23 ICR19 370 _H 000FFF70 _H - Backup RAM diagnosis end 36 24 ICR19 370 _H 000FFF70 _H - Backup RAM initialization completion 36 24 ICR20 36C _H 000FFF6C _H - Up/down counter 0 36 24 ICR20 36C _H 000FFF6C _H - Up/down counter 1 Real time clock 37 25 ICR21 368 _H 000FFF68 _H - Multi-function serial interface 37 25 ICR22 364 _H 000FFF64 _H 22* ¹ Multi-function serial interface 38 26 ICR22 364 _H 000FFF60 _H 23 6.h? (reansmission completed) 39 27 ICR23 360 _H 000FFF50 _H 23 16-bit Free-run timer 1 (0 detection) / 40 28 ICR24 35C _H 000FFF5C _H 24* ³ 16-bit Free-run timer 2 (0 detection) / 41 29 ICR25 358 _H 000FFF58 _H	RAM initialization completion						
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Error generation during RAM diagnosis	35	23	ICR19	370 _H	000FFF70 _H	-
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Backup RAM diagnosis end						
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Backup RAM initialization completion						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Error generation during Backup RAM diagnosis						
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	CAN2						
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Up/down counter 0	36	24	ICR20	36Cн	000FFF6C _H	-
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Up/down counter 1						
Multi-function serial interface 38 26 ICR22 364_{H} $000FFF64_{H}$ 22^{*1} Multi-function serial interface 364_{H} $000FFF64_{H}$ 22^{*1} 16-bit Free-running timer 0 (0 detection) / 39 27 ICR23 360_{H} $000FFF60_{H}$ 23 Multi-function serial interface 39 27 ICR23 360_{H} $000FFF60_{H}$ 23 Multi-function serial interface 39 27 ICR23 360_{H} $000FFF60_{H}$ 23 PFG 1/10/11/20/21/30/31 40 28 ICR24 $35C_{H}$ $000FFF5C_{H}$ 24^{*3} (compare clear) 40 28 ICR25 358_{H} $000FFF58_{H}$ 25^{*3} 16-bit Free-run timer 2 (0 detection) / 41 29 ICR25 358_{H} $000FFF58_{H}$ 25^{*3} PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354_{H} $000FFF50_{H}$ 27^{*3}	Real time clock	37	25	ICR21	368 _н	000FFF68 _H	-
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Multi-function serial interface						
Multi-function serial interface 38 26 ICR22 364_{H} $000FFF64_{H}$ 22^{**} 16-bit Free-running timer 0 (0 detection) / (compare clear) 39 27 ICR23 360_{H} $000FFF60_{H}$ 23 Multi-function serial interface 39 27 ICR23 360_{H} $000FFF60_{H}$ 23 PPG 1/10/11/20/21/30/31 39 28 ICR24 $35C_{H}$ $000FFF5C_{H}$ 24^{*3} 16-bit Free-run timer 1 (0 detection) / (compare clear) 40 28 ICR24 $35C_{H}$ $000FFF5C_{H}$ 24^{*3} 16-bit Free-run timer 2 (0 detection) / (compare clear) 41 29 ICR25 358_{H} $000FFF58_{H}$ 25^{*3} PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354_{H} $000FFF50_{H}$ 27^{*3} PPG 6/7/16/17/26/27/37 43 2B ICR27 350_{H} $000FFF50_{H}$ 27^{*3} PPG 8/9/18/19/28/29 44 2C ICR28 $34C_{H}$ $000FFF4C_{H}$ 28^{*3}	ch.7 (reception completed)						aa+1
$ \begin{array}{c} \text{ch.7 (status)} & \text{I} & I$	Multi-function serial interface	38	26	ICR22	364 _Н	000FFF64 _H	22*1
$\begin{array}{c cccc} 16-bit \ {\rm Free-running \ timer \ 0 \ (0 \ detection) \ / \ (compare \ clear)} \\ \hline Multi-function \ {\rm serial \ interface \ ch.7 \ (transmission \ completed) \ \\ \hline PPG \ 1/10/11/20/21/30/31 \\ 16-bit \ {\rm Free-run \ timer \ 1 \ (0 \ detection) \ / \ (compare \ clear) \ \\ \hline PPG \ 2/3/12/13/23/32/43 \\ 16-bit \ {\rm Free-run \ timer \ 2 \ (0 \ detection) \ / \ \\ (compare \ clear) \ \\ \hline PPG \ 4/5/14/15/24/25/35/44 \ \\ PPG \ 6/7/16/17/26/27/37 \ \\ \hline PPG \ 8/9/18/19/28/29 \ \\ \hline \end{array} \begin{array}{c} 39 \\ 27 \\ \hline 1CR23 \\ 360_H \\ 20 \\ \hline 1CR23 \\ 360_H \\ 000FFF60_H \\ 23 \\ 000FFF60_H \\ 23 \\ 000FFF5C_H \ 24^{*3} \\ 24^{*3} \\ 24^{*3} \\ 24^{*3} \\ 24^{*3} \\ 24^{*3} \\ 28 \\ \hline 1CR25 \\ 358_H \\ 000FFF58_H \ 25^{*3} \\ 000FFF58_H \ 25^{*3} \\ 25^{*3} \\ 000FFF54_H \ 26^{*3} \\ 27^{*3} \\ 28 \\ \hline 1CR26 \ 354_H \ 000FFF54_H \ 26^{*3} \\ 000FFF54_H \ 27^{*3} \\ 27^{*3} \\ 28 \\ \hline 1CR27 \ 350_H \ 000FFF50_H \ 27^{*3} \\ 000FFF50_H \ 27^{*3} \\ 27^{*3} \\ \hline 27 \\ \hline 28 \\ \hline 1CR28 \ 34C_H \ 000FFF4C_H \ 28^{*3} \\ \hline 28 \\ \hline 1CR28 \ 34C_H \ 000FFF4C_H \ 28^{*3} \\ \hline 28 \\ \hline 28$	ch.7 (status)						
(compare clear) 39 27 ICR23 360 _H 000FFF60 _H 23 Multi-function serial interface	16-bit Free-running timer 0 (0 detection) /						
Multi-function serial interface 39 27 ICR23 360 _H 000FFF60 _H 23 Multi-function serial interface 29 1CR23 360 _H 000FFF60 _H 23 PPG 1/10/11/20/21/30/31 40 28 ICR24 35C _H 000FFF5C _H 24* ³ 16-bit Free-run timer 1 (0 detection) / 40 28 ICR24 35C _H 000FFF5C _H 24* ³ 16-bit Free-run timer 2 (0 detection) / 41 29 ICR25 358 _H 000FFF58 _H 25* ³ (compare clear) PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354 _H 000FFF54 _H 26* ³ PPG 6/7/16/17/26/27/37 43 2B ICR27 350 _H 000FFF50 _H 27* ³ PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28* ³	(compare clear)						
ch.7 (transmission completed) Image: ch.7 (transmission complete) Image: ch.7 (transmi	Multi-function serial interface	39	27	ICR23	360 _H	000FFF60 _H	23
PPG 1/10/11/20/21/30/31 40 28 ICR24 35C _H 000FFF5C _H 24*3 16-bit Free-run timer 1 (0 detection) / (compare clear) 40 28 ICR24 35C _H 000FFF5C _H 24*3 PPG 2/3/12/13/23/32/43 41 29 ICR25 358 _H 000FFF58 _H 25*3 16-bit Free-run timer 2 (0 detection) / (compare clear) 41 29 ICR25 358 _H 000FFF58 _H 25*3 PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354 _H 000FFF54 _H 26*3 PPG 6/7/16/17/26/27/37 43 2B ICR27 350 _H 000FFF50 _H 27*3 PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28*3	ch.7 (transmission completed)						
16-bit Free-run timer 1 (0 detection) / (compare clear) 40 28 ICR24 35C _H 000FFF5C _H 24* ³ PPG 2/3/12/13/23/32/43 41 29 ICR25 358 _H 000FFF58 _H 25* ³ 16-bit Free-run timer 2 (0 detection) / (compare clear) 41 29 ICR25 358 _H 000FFF58 _H 25* ³ PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354 _H 000FFF54 _H 26* ³ PPG 6/7/16/17/26/27/37 43 2B ICR27 350 _H 000FFF50 _H 27* ³ PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28* ³	PPG 1/10/11/20/21/30/31						
(compare clear) Image: Compare clear (Compare clear) Image: C	16-bit Free-run timer 1 (0 detection) /	40	28	ICR24	35Cн	000FFF5Cн	24* ³
PPG 2/3/12/13/23/32/43 41 29 ICR25 358 _H 000FFF58 _H 25* ³ 16-bit Free-run timer 2 (0 detection) / (compare clear) 41 29 ICR25 358 _H 000FFF58 _H 25* ³ PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354 _H 000FFF54 _H 26* ³ PPG 6/7/16/17/26/27/37 43 2B ICR27 350 _H 000FFF50 _H 27* ³ PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28* ³	(compare clear)						
16-bit Free-run timer 2 (0 detection) / (compare clear) 41 29 ICR25 358 _H 000FFF58 _H 25* ³ PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354 _H 000FFF54 _H 26* ³ PPG 6/7/16/17/26/27/37 43 2B ICR27 350 _H 000FFF50 _H 27* ³ PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28* ³	PPG 2/3/12/13/23/32/43						
(compare clear) Image: Compare clear Image: Compare	16-bit Free-run timer 2 (0 detection) /	41	29	ICR25	358н	000FFF58 _н	25* ³
PPG 4/5/14/15/24/25/35/44 42 2A ICR26 354 _H 000FFF54 _H 26* ³ PPG 6/7/16/17/26/27/37 43 2B ICR27 350 _H 000FFF50 _H 27* ³ PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28* ³	(compare clear)						
PPG 6/7/16/17/26/27/37 43 2B ICR27 350 _H 000FFF50 _H 27* ³ PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28* ³	PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354н	000FFF54	26* ³
PPG 8/9/18/19/28/29 44 2C ICR28 34C _H 000FFF4C _H 28* ³	PPG 6/7/16/17/26/27/37	43	2B	ICR27	350 _н	000FFF50 _H	27* ³
	PPG 8/9/18/19/28/29	44	2C	ICR28	34Cн	000FFF4C _H	28* ³



Value Parameter Symbol Pin name Conditions Unit Remarks Min Max SCK0 to SCK11 Serial clock cycle time t_{SCYC} 4t_{CPP} _ ns SCK0 to SCK2. SCK5 to SCK11 -30 30 ns SOT0 to SOT2, $SCK \uparrow \rightarrow$ tshovi SOT5 to SOT11 SOT delay time SCK3, SCK4 -300 300 ns SOT3, SOT4 SCK0 to SCK2. Internal shift clock SCK5 to SCK11 mode output pin : 34 ns _ Valid SIN \rightarrow SIN0 to SIN2. C_L=50pF t_{IVSLI} SIN5 to SIN11 SCK ↓ setup time SCK3, SCK4 300 _ ns SIN3, SIN4 SCK0 to SCK11 $SCK \perp \rightarrow$ 0 _ t_{SLIXI} ns Valid SIN hold time SIN0 to SIN11 SOT→SCK↓ SCK0 to SCK11 2t_{CPP} t_{SOVLI} _ ns delay time SOT0 to SOT11 -30 Serial clock tcpp+ tsusi ns "H"pulse width 10 SCK0 to SCK11 Serial clock 2t_{CPP} t_{SLSH} _ ns "L" pulse width -10 SCK0 to SCK2. SCK5 to SCK11 33 _ ns $SCK \uparrow \rightarrow$ SOT0 to SOT2, t_{SHOVE} SOT5 to SOT11 SOT delay time SCK3, SCK4 _ 300 ns External shift clock SOT3, SOT4 mode output pin: C_L=50pF Valid SIN → **t**_{IVSHE} 10 _ ns SCK ↓ setup time SCK0 to SCK11 SIN0 to SIN11 $SCK \downarrow \rightarrow$ 20 **t**_{SLIXE} _ ns Valid SIN hold time SCK fall time SCK0 to SCK11 5 t⊧ ns _ SCK rise time SCK0 to SCK11 5 t_R _ ns

(4-1-3) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=0, SCR:SPI=1 (T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.









(4-1-8) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0, When Serial chip select is used: SCSCR:CSEN=1, Serial clock output mark level "L" : SMR,SCSFR:SCINV=1, Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0 (T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Doromotor	Cumhal	Din nome Conditions	Va	lue	Unit	Domorko	
Parameter	Symbol	Pin name	Conditions	Min	Мах	Unit	Remarks
SCS↑→SCK↑ setup time	tcssi	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{cssu} -50 ⁺1	t _{cssu} +0 ⁺1	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSSU} -50 *1	t _{CSSU} +300 *1	ns	
SCK↓→SCS↓ hold time	t _{сsнi}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	tcsн⊡-10 ⁺2	t _{CSHD} +50 *2	ns	Internal shift clock mode output pin : C∟=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSHD} -300 *2	t _{сsнD} +50 *2	ns	
SCS deselect time	tcspi	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{csbs} -50 ⁺3	t _{CSDS} +50 ⁺3	ns	



Flash memory

(1) Electrical Characteristics

Devenetor	Value			Unit	Domorko	
Parameter	Min	Тур	Max	Unit	Remarks	
	-	200	800	ms	8 Kbytes sector* ¹ , excluding internal preprogramming time	
	-	300	1100	ms	8 Kbytes sector* ¹ , including internal preprogramming time	
Sector erase time	_	400	2000	ms	64 Kbytes sector* ¹ , excluding internal preprogramming time	
	– 700 3700 ms		ms	64 Kbytes sector* ¹ , including internal preprogramming time		
8-bit writing time	-	9	288	μs	Exclusive of overhead time at system level* ¹	
16-bit writing time	-	12	384	μs	Exclusive of overhead time at system level* ¹	
ECC writing time	-	9	288	μs	Exclusive of overhead time at system level* ¹	
Erase cycle ^{*2} / Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	_	_	_	Average T _A =+85°C* ³	

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.

In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection

voltage (V_{DL}^{*}), hold Vcc at 2.7V or more within the duration calculated by the following expression:

 $Td^{*}[\mu s] + (period of PCLK [\mu s] \times 257) + 50 [\mu s]$

*: See "4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) "



Part number	Sub clock	CSV Initial value	LVD Initial value	Package* ²
MB91F526KWBPMC1	Yes	ON	ON	
MB91F526KYBPMC1			OFF	
MB91F526KJBPMC1		OFF	ON	
MB91F526KLBPMC1			OFF	
MB91F525KWBPMC1		ON	ON	
MB91F525KYBPMC1			OFF	
MB91F525KJBPMC1		OFF	ON	
MB91F525KLBPMC1			OFF	
MB91F524KWBPMC1		ON	ON	
MB91F524KYBPMC1			OFF	
MB91F524KJBPMC1		OFF	ON	
MB91F524KLBPMC1			OFF	
MB91F523KWBPMC1		ON	ON	
MB91F523KYBPMC1			OFF	
MB91F523KJBPMC1		OFF	ON	
MB91F523KLBPMC1			OFF	
MB91F522KWBPMC1		ON	ON	
MB91F522KYBPMC1			OFF	
MB91F522KJBPMC1		OFF	ON	
MB91F522KLBPMC1			OFF	LQN • 144 pin, (Lead pitch 0 4mm)
MB91F526KSBPMC1	None	ON	ON	Plastic
MB91F526KUBPMC1			OFF	
MB91F526KHBPMC1		OFF	ON	
MB91F526KKBPMC1			OFF	
MB91F525KSBPMC1		ON	ON	
MB91F525KUBPMC1			OFF	
MB91F525KHBPMC1		OFF	ON	
MB91F525KKBPMC1			OFF	
MB91F524KSBPMC1		ON	ON	
MB91F524KUBPMC1			OFF	
MB91F524KHBPMC1		OFF	ON	
MB91F524KKBPMC1			OFF	
MB91F523KSBPMC1		ON	ON	
MB91F523KUBPMC1			OFF	
MB91F523KHBPMC1		OFF	ON	
MB91F523KKBPMC1			OFF	
MB91F522KSBPMC1		ON	ON	
MB91F522KUBPMC1			OFF	
MB91F522KHBPMC1		OFF	ON	
MB91F522KKBPMC1			OFF	



Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWEPMC	Yes	ON	ON	
MB91F526FJEPMC		OFF	ON	
MB91F525FWEPMC		ON	ON	
MB91F525FJEPMC		OFF	ON	
MB91F524FWEPMC		ON	ON	
MB91F524FJEPMC		OFF	ON	
MB91F523FWEPMC		ON	ON	
MB91F523FJEPMC		OFF	ON	
MB91F522FWEPMC		ON	ON	
MB91F522FJEPMC		OFF	ON	LQI ⋅ 100 pin,
MB91F526FSEPMC	None	ON	ON	Plastic
MB91F526FHEPMC		OFF	ON	
MB91F525FSEPMC		ON	ON	
MB91F525FHEPMC		OFF	ON	
MB91F524FSEPMC		ON	ON	
MB91F524FHEPMC		OFF	ON	
MB91F523FSEPMC		ON	ON	
MB91F523FHEPMC		OFF	ON	
MB91F522FSEPMC		ON	ON	
MB91F522FHEPMC		OFF	ON	
MB91F526DWEPMC	Yes	ON	ON	
MB91F526DJEPMC		OFF	ON	
MB91F525DWEPMC		ON	ON	
MB91F525DJEPMC		OFF	ON	
MB91F524DWEPMC		ON	ON	
MB91F524DJEPMC		OFF	ON	
MB91F523DWEPMC		ON	ON	
MB91F523DJEPMC		OFF	ON	
MB91F522DWEPMC		ON	ON	
MB91F522DJEPMC		OFF	ON	LQH • 80 pin,
MB91F526DSEPMC	None	ON	ON	Plastic
MB91F526DHEPMC		OFF	ON	
MB91F525DSEPMC		ON	ON	
MB91F525DHEPMC		OFF	ON	
MB91F524DSEPMC		ON	ON	
MB91F524DHEPMC		OFF	ON	
MB91F523DSEPMC		ON	ON	
MB91F523DHEPMC		OFF	ON	
MB91F522DSEPMC		ON	ON	
MB91F522DHEPMC		OFF	ON	



LQS144, 144 Lead Plastic Low Profile Quad Flat Package



PACKAGE		LQS144			
SYMBOL	MIN.	NOM.	MAX.		
A		—	1.70		
A1	0.06	—	0.26		
b	0.17	0.22	0.27		
c	0.09	—	0.20		
D	2	2.00 BSC) .		
D1	2	0.00 BSC).		
e		0.50 BSC	;		
E	2	2.00 BSC) .		
E1	2	0.00 BSC).		
L	0.45	0.60	0.75		
L1	0.30	0.50	0.70		
aaa	—	—	0.20		
bbb			0.10		
000			0.08		
ddd	0.08				
N		144			

NOTES

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- ADATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- ADIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- ▲ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- ▲ DIMENSION & DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (\$) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED & MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

▲ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.







PACKAGE		LQN144		
SYMBOL	MIN.	NOM.	MAX.	
A	—	—	1.70	
A1	0.05	—	0.15	
b	0.145	0.18	0.215	
C	0.115		0.195	
D	18.00 BSC.			
D1	16.00 BSC.			
e	0.40 BSC			
E	18.00 BSC.			
E1	16.00 BSC.			
L	0.45	0.60	0.75	
L1	0.30	0.50	0.70	
aaa	—	_	0.20	
bbb	—		0.10	
000			0.08	
ddd			0.07	
N	144			

NOTES

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- ▲ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- ADATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- ADETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- ⚠ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- ▲ DIMENSION 5 DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (5) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 5 MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- ▲ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- 1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.





Scope of Impact

For the affected parts, when the Power-On Reset and Internal Low Voltage Detection are not generated, the MCU may set invalid package and sub clock option information. Therefore, the MCU may operate with an invalid pin configuration.

Workaround

For the affected parts, it is necessary to satisfy at least one of the Power-On Reset requirements for any Power-On event as given below:

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate is less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

If the customer system does not satisfy the condition above-mentioned, Cypress will releases new version D, so Cypress recommends the version D for MB91F52x. The new version prevents the limitation when an external reset signal is asserted at pin RSTX anytime the supply voltage (VCC) is turned on.

Fix Status

Will be fixed in production silicon version D, E

2. Limitation for Watch mode (power off)

Problem Definition

If the below all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

Trigger Conditions

- (1) Using the watch mode (power off)
- (2) Interrupt levels that are used as sources for recovering from the watch mode (power off) are '16' to '30', or using NMIX pin as source for recovering from the watch mode (power off)
- (3) The sources for recovering from the watch mode (power off) are generated between PCLK 1 cycle and PMUCLK 3 cycles (*), after CPU state changes to the watch mode (power off)
 (*): In case of PCLK = 0.5 MHz and PMUCLK = 32 kHz, it is approx. 2 μs to 100 μs

Scope of Impact

If the all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

WTCRH, WTCRM, WTCRL CSELR.SCEN CMONR.SCRDY CCRTSELR.CST CCRTSELR.CSC

MB91520 Series



Page	Section	Change Results
		- Bottom
14	■Pin Assignment MB91F52xD	40 VCC 33 P087/DAOD/PPG7_0INT8_0 34 P081/SOT5_0/SDA/S/AN0/PPG1_0 35 P073/SOT4_0/SDA/S/AN0/PPG1_0 36 P153/SCK5_0/SCL5/AN32/FRCKL_UINT4_1 37 P081/SOT5_0/SDA/S/AN0/PPG1_0 38 P072/SIN4_0/AN34/CU2_2/INT5_0 39 P071/SCK4_2/AN33/CU1_2/MONCLK 31 P066/SOT4_2/SCS3_0/AN3/FRCK2_0/ANN_1_IPFG43_1 32 P067/AN3/6FRCK5_0/ANN0_1 31 P066/SOT4_2/SCS3_0/AN3/FRCK1_0/BIN1_1 32 P067/AN3/6FRCK5_0/ANN0_FG4_/IFRCK0_0/OTOT7_1/ZIN1_1 33 P071/SC40_0/AN40/PPG4_I/FRCK0_0/TOT7_1/ZIN1_1 34 P064/SC32_0/AN3/FRCK1_0/BIN1_1 35 P064/SC32_0/AN3/FRCK1_0/BIN1_1 36 PO7/SCK10_1/AN41/I/CU6_0/PPG4_1/FRCK0_0/TOT6_1/I/TIN6_1 37 P064/SC42_I/AN42/PPG3_0/TIN4_1 36 AVCC1 37 P057/SCK10_1/AN42/PPG3_0/TIN4_1 38 P07/SCK10_1/AN42/PPG3_0/TIN4_1
		40 VCC 39 P087/DA00PPG7_0INT8_0 39 P087/DA00PPG7_0INT8_0 37 P081/S0T5_0/SNL1PPG2_0 38 P082/SIN5_0/SNL5/SN2EFRCK1_I/INT4_1 39 P081/SOT5_0/SN3EFRCK1_UNT4_1 39 P073/SN3GU3_2 31 P073/SN36FRCK5_0/SUNO_1 32 P067/N136FRCK5_0/AIN0_1 31 P068/SOT5_0/AISFFRCK2_0/AIN1_1/PFG43_1 39 P063/SCS41_0/N39/FRCK2_0/AIN1_1/PFG43_1 39 P063/SCS10_1/SCS40_0/NA40/PFG4_1/FRCK0_0/TOT7_1/ZIN1_1 31 P063/SCS10_1/SCS40_0/AA40/PFG4_1/FRCK0_0/TOT7_1/ZIN1_1 32 P063/SCS10_1/SCS40_0/AA40/PFG4_1/FRCK0_0/TOT7_1/ZIN1_1_1 34 P063/SCS10_1/AA42/ICU8_0/TRG6_2/PFG1_1/ICU1_1/TIN6_1 35 AVSC11 36 AVSS1I/AVRL1 37 P063/SCSL0_1/AN42/ICU8_0/TRG6_2/PFG1_1/ICU1_1/TIN6_1 32 P067/SCK10_1/AN42/ICU8_0/TRG6_2/PFG1_1/ICU1_1/ITN6_1 31 P067/SCK10_0/AN43/PFG37_0/TIN4_1



$(Continued) \\ (Correct) \\ \hline \\ $	Page	Section	Change Results						
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$			(Contin	ued)					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			(Correct)						
$ \left[\begin{array}{cccccccccccccccccccccccccccccccccccc$					Pin	no.			Pin
$\left[\begin{array}{cccccccccccccccccccccccccccccccccccc$			64	80	100	120	144	176	Name
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$									P015
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		-	-		-	2	2	D29	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$								TRG0_0	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$							•		P016
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			-	-	-	-	3	3	D30
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$									P170
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			-	-	-	-	-	4	PPG36_1
- - - 4 5 D31 TRG2_0 - - - 6 P171 PPG37_1									P017
6 TRG2_0 PPG37_1			-	-	-	-	4	5	D31
6 <u>P171</u> PPG37 1									TRG2_0
PPG37 1								6	P171
			-	-	-	-	-	0	PPG37_1
<u>Ρ020</u> ΔSX ^{*2, *3, *4, *5}	19 ■PIN Description							P020	
		*1	- *1	- *1	- *1	_	_	SIN3 1	
2 2 2 2 2 5 7 TRG3 0		2 '	2 '	2 '	2 '	5	7	TRG3 0	
TIN0_2								TIN0_2	
19 PIN Description RTO5_1								RTO5_1	
P021			-	-		3 ^{*1}	6	8	P021
									CS0X °
$ 3 - 6 - 8 - \frac{SO13 - 1}{TDOC 4}$									<u>SOI3_1</u>
									P022
			-	-	-	4 ^{*1}	7	9	CS1X ^{*5}
4 ^{*1} 7 9 SCK3 1									SCK3 1
TRG7_1									TRG7_1
TRG5_0									TRG5_0
P023									P023
					-	5 ^{*1}	8		RDX ³
$\begin{vmatrix} - & - & - & 5 \end{vmatrix} = 8 \begin{vmatrix} 10 & SCS3 \\ DEDOOD & 0 \end{vmatrix}$			-	-				10	SCS3_1
									PPG32_0
									P024
WR0X ^{+2,+3,+4,}					3 ^{*1}	6 ^{*1}		11	WR0X ^{*2,*3,*4,}
									-5
3^{11} 3^{11} 3^{11} 3^{11} 9 11 SIN4_1			3 ^{*1}	3 ^{*1}			9		SIN4_1
				-					PPG24_0
INT15 0								INT15 0	





Page	Section	Change Results
46	■During Power-on	The following sentence modified as following: (Error) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during nower-on
142,143	11. Electrical Characteristics Recommended operating conditions	 The following sentence modified as following: (Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset. (Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
156, 157	11. Electrical Characteristics AC Characteristics	Added (3-2) Power-on Conditions for MB91F52xxxE