Infineon Technologies - MB91F523KSCPMC1-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f523kscpmc1-gse2

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	28 *1	31	39	P050	-	A	General-purpose I/O port
						A18 *5	-		External bus/Address bit18 output
						TRG5_1	-		PPG trigger 5 input (1)
						PPG33_0	-		PPG ch.33 output (0)
-	-	-	-	32	40	P051	-	A	General-purpose I/O port
						A19	-		External bus/Address bit19 output
						TRG9_0	-		PPG trigger 9 input (0)
-	-	-	-	33	41	P052	-	A	General-purpose I/O port
						A20	-		External bus/Address bit20 output
						PPG34_0	-		PPG ch.34 output (0)
						INT14_0	-		INT14 External interrupt input (0)
16 *1	19 *1	24 *1	29 *1	34	42	P053	-	B	General-purpose I/O port
						A21 *2, *3, *4, *5	-		External bus/Address bit21 output
						AN44	-		ADC analog 44 input
						PPG35_0	-		PPG ch.35 output (0)
						INT14_1	-		INT14 External interrupt input (1)
						SCK0_1	-		Multi-function serial ch.0 clock I/O (1)
-	-	-	-	35	43	P054	-	A	General-purpose I/O port
						SYSCLK	-		External bus/System clock output
						PPG36_0	-		PPG ch.36 output (0)
17 *1	22 *1	27 *1	32 *1	38	46	P055	-	G	General-purpose I/O port
						CS2X *2, *3, *4, *5	-		External bus chip select 2 output
						SIN10_0	-		Multi-function serial ch.10 serial data input (0)
						AN43	-		ADC analog 43 input
						PPG37_0	-		PPG ch.37 output (0)
						TIN4_1	-		Reload timer ch.4 event input (1)
-	-	-	-	-	47	P180	-	A	General-purpose I/O port
						PPG40_0	-		PPG ch.40 output (0)
-	-	-	-	-	48	P181	-	A	General-purpose I/O port
						PPG41_0	-		PPG ch.41 output (0)
-	-	-	33 *1	39	49	P056	-	A	General-purpose I/O port
						CS3X *5	-		External bus chip select 3 output
						ICU9_0	-		Input capture ch.9 input (0)
						PPG0_1	-		PPG ch.0 output (1)
						ICU0_1	-		Input capture ch.0 input (1)
						TIN5_1	-		Reload timer ch.5 event input (1)
						DTTI_2	-		Waveform generator ch.0-ch.5 input pin (2)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	76	94	P092	-	B	General-purpose I/O port
						AN6	-		ADC analog 6 input
						PPG40_1	-		PPG ch.40 output (1)
						ICU2_0	-		Input capture ch.2 input (0)
						TOT0_1	-		Reload timer ch.0 output (1)
-	-	-	-	-	95	P192	-	A	General-purpose I/O port
						PPG24_1	-		PPG ch.24 output (1)
						TOT1_1	-		Reload timer ch.1 output (1)
34 *1	42 *1	52	62	77	96	P093	-	J	General-purpose I/O port
						TX0_1	-		CAN transmission data 0 output (1)
						SIN11_0	-		Multi-function serial ch.11 serial data input (0)
						AN7	-		ADC analog 7 input
						ICU4_2	-		Input capture ch.4 input (2)
						PPG16_1	-		PPG ch.16 output (1)
						ICU3_0	-		Input capture ch.3 input (0)
						TOT2_1 *2, *3	-		Reload timer ch.2 output (1)
-	-	-	-	78	97	P094	-	B	General-purpose I/O port
						AN8	-		ADC analog 8 input
						ICU4_0	-		Input capture ch.4 input (0)
						TOT3_1	-		Reload timer ch.3 output (1)
-	-	53	63	79	98	P095	-	B	General-purpose I/O port
						TX0(128)	-		CAN transmission data 0 output
						SCS11_0	-		Serial chip select 11 I/O (0)
						AN9	-		ADC analog 9 input
35	43	54	64	80	99	P096	-	G	General-purpose I/O port
						RX0(128)	-		CAN reception data 0 input
						SOT11_0 / SDA11	-		Multi-function serial ch.11 serial data output (0)/I^2C bus serial data I/O
						AN10	-		ADC analog 10 input
						INT0_0	-		INT0 External interrupt input (0)
36	44	55	65	81	100	P097	-	G	General-purpose I/O port
						SCK11_0 / SCL11	-		Multi-function serial ch.11 clock I/O (0)/ I^2C bus serial clock I/O
						AN11	-		ADC analog 11 input
						ICU5_0	-		Input capture ch.5 input (0)
						PPG17_1	-		PPG ch.17 output (1)

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001804_H	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001808_H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
$00180C_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810_H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814_H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818_H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00181C_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820_H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824_H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828_H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
$00182C_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830_H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834_H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838_H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
$00183C_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001878_H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W -------- *3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W -------- *3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W -------- *3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W -------- *3	Multi-UART7 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00187C_H$	—	— /(SCSFR27) [R/W] B,H,W -------- *3	— /(SCSFR17) [R/W] B,H,W -------- *3	— /(SCSFR07) [R/W] B,H,W -------- *3	
001880_H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W -------- *3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W -------- *3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W -------- *3	TBYTE07/(LAMRID7) / (LAMTID7) [R/W] B,H,W 00000000	
001884_H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -------- *2	— /(ISBA7)[R/W] B,H,W -------- *2	Multi-UART7
001888_H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
$00188C_H$	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890_H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894_H	— /(RDR18/(TDR18))[R/W] B,H,W -------- -------- *3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000 *1		
001898_H	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
$00189C_H$	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- -------- *3 *4		
$0018A0_H$	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -------- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -------- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -------- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -------- *3	
$0018A4_H$	—	— /(SCSFR28) [R/W] B,H,W -------- *3	— /(SCSFR18) [R/W] B,H,W -------- *3	— /(SCSFR08) [R/W] B,H,W -------- *3	
$0018A8_H$	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -------- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -------- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -------- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	
$0018AC_H$	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -------- *2	— /(ISBA8)[R/W] B,H,W -------- *2	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001928_H	FCR111[R/W] B,H,W ---00100	FCR011[R/W] B,H,W -0000000	FBYTE11[R/W] B,H,W 00000000 00000000		Multi-UART11
$00192C_H$	FTICR11[R/W] B,H,W 00000000 00000000		—	—	
001930_H to $0019D8_H$	—	—	—	—	Reserved
$0019DC_H$	—	GATEC0 [R/W] B,H,W ------00	—	GATEC2 [R/W] B,H,W ------00	PPG GATE control
$0019E0_H$	—	GATEC4 [R/W] B,H,W ------00	—	—	
$0019E4_H$	—	—	—	—	Reserved
$0019E8_H$	GTRS0 [R/W] B,H,W -0000000 -0000000		GTRS1 [R/W] B,H,W -0000000 -0000000		PPG controller
$0019EC_H$	GTRS2 [R/W] B,H,W -0000000 -0000000		GTRS3 [R/W] B,H,W -0000000 -0000000		
$0019F0_H$	GTRS4 [R/W] B,H,W -0000000 -0000000		GTRS5 [R/W] B,H,W -0000000 -0000000		
$0019F4_H$	GTRS6 [R/W] B,H,W -0000000 -0000000		GTRS7 [R/W] B,H,W -0000000 -0000000		
$0019F8_H$	GTRS8 [R/W] B,H,W -0000000 -0000000		GTRS9 [R/W] B,H,W -0000000 -0000000		PPG controller
$0019FC_H$	GTRS10 [R/W] B,H,W -0000000 -0000000		GTRS11 [R/W] B,H,W -0000000 -0000000		
$001A00_H$	GTRS12 [R/W] B,H,W -0000000 -0000000		GTRS13 [R/W] B,H,W -0000000 -0000000		
$001A04_H$	GTRS14 [R/W] B,H,W -0000000 -0000000		GTRS15 [R/W] B,H,W -0000000 -0000000		
$001A08_H$	GTRS16 [R/W] B,H,W -0000000 -0000000		GTRS17 [R/W] B,H,W -0000000 -0000000		
$001A0C_H$	GTRS18 [R/W] B,H,W -0000000 -0000000		GTRS19 [R/W] B,H,W -0000000 -0000000		
$001A10_H$	GTRS20 [R/W] B,H,W -0000000 -0000000		GTRS21 [R/W] B,H,W -0000000 -0000000		
$001A14_H$	GTRS22 [R/W] B,H,W -0000000 -0000000		GTRS23 [R/W] B,H,W -0000000 -0000000		
$001A18_H$ to $001A2C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001AD0_H$	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
$001AD4_H$	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
$001AD8_H$	PCN206 [R/W] B,H,W --000000 -----110		PSDR6 [R/W] H,W 00000000 00000000		
$001ADC_H$	PTPC6 [R/W] H,W 00000000 00000000		—	—	
$001AE0_H$	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
$001AE4_H$	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
$001AE8_H$	PCN207 [R/W] B,H,W --000000 -----110		PSDR7 [R/W] H,W 00000000 00000000		
$001AEC_H$	PTPC7 [R/W] H,W 00000000 00000000		—	—	
$001AF0_H$	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
$001AF4_H$	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
$001AF8_H$	PCN208 [R/W] B,H,W --000000 -----110		PSDR8 [R/W] H,W 00000000 00000000		
$001AFC_H$	PTPC8 [R/W] H,W 00000000 00000000		—	—	
$001B00_H$	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
$001B04_H$	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
$001B08_H$	PCN209 [R/W] B,H,W --000000 -----110		PSDR9 [R/W] H,W 00000000 00000000		
$001B0C_H$	PTPC9 [R/W] H,W 00000000 00000000		—	—	
$001B10_H$	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
$001B14_H$	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PTMR10 [R] H,W 11111111 11111111		
$001B18_H$	PCN210 [R/W] B,H,W --000000 -----110		PSDR10 [R/W] H,W 00000000 00000000		PPG10
$001B1C_H$	PTPC10 [R/W] H,W 00000000 00000000		—	—	
$001B20_H$	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11

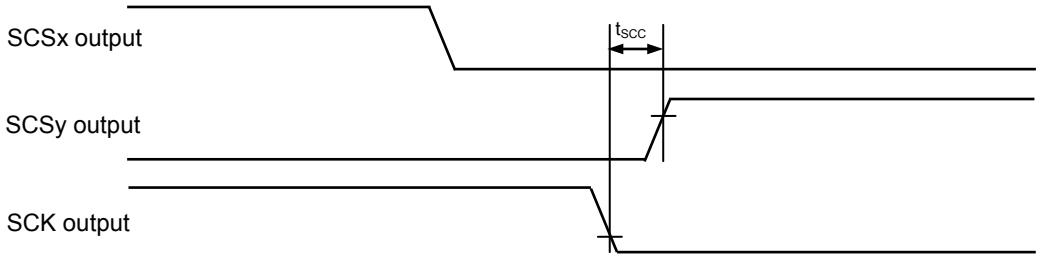
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001BCC$_H$	PTPC21 [R/W] H,W 00000000 00000000		—	—	PPG21
001BD0$_H$	PCN22 [R/W] B,H,W 00000000 000000-0		PCSR22 [W] H,W XXXXXXXX XXXXXXXX		PPG22
001BD4$_H$	PDUT22 [W] H,W XXXXXXXX XXXXXXXX		PTMR22 [R] H,W 11111111 11111111		
001BD8$_H$	PCN222 [R/W] B,H,W --000000 -----110		PSDR22 [R/W] H,W 00000000 00000000		
001BDC$_H$	PTPC22 [R/W] H,W 00000000 00000000		—	—	
001BE0$_H$	PCN23 [R/W] B,H,W 00000000 000000-0		PCSR23 [W] H,W XXXXXXXX XXXXXXXX		PPG23
001BE4$_H$	PDUT23 [W] H,W XXXXXXXX XXXXXXXX		PTMR23 [R] H,W 11111111 11111111		
001BE8$_H$	PCN223 [R/W] B,H,W --000000 -----110		PSDR23 [R/W] H,W 00000000 00000000		
001BEC$_H$	PTPC23 [R/W] H,W 00000000 00000000		—	—	
001BF0$_H$	PCN24 [R/W] B,H,W 00000000 000000-0		PCSR24 [W] H,W XXXXXXXX XXXXXXXX		PPG24
001BF4$_H$	PDUT24 [W] H,W XXXXXXXX XXXXXXXX		PTMR24 [R] H,W 11111111 11111111		
001BF8$_H$	PCN224 [R/W] B,H,W --000000 -----110		PSDR24 [R/W] H,W 00000000 00000000		
001BFC$_H$	PTPC24 [R/W] H,W 00000000 00000000		—	—	
001C00$_H$	PCN25 [R/W] B,H,W 00000000 000000-0		PCSR25 [W] H,W XXXXXXXX XXXXXXXX		PPG25
001C04$_H$	PDUT25 [W] H,W XXXXXXXX XXXXXXXX		PTMR25 [R] H,W 11111111 11111111		
001C08$_H$	PCN225 [R/W] B,H,W --000000 -----110		PSDR25 [R/W] H,W 00000000 00000000		
001C0C$_H$	PTPC25 [R/W] H,W 00000000 00000000		—	—	
001C10$_H$	PCN26 [R/W] B,H,W 00000000 000000-0		PCSR26 [W] H,W XXXXXXXX XXXXXXXX		PPG26
001C14$_H$	PDUT26 [W] H,W XXXXXXXX XXXXXXXX		PTMR26 [R] H,W 11111111 11111111		
001C18$_H$	PCN226 [R/W] B,H,W --000000 -----110		PSDR26 [R/W] H,W 00000000 00000000		
001C1C$_H$	PTPC26 [R/W] H,W 00000000 00000000		—	—	
001C20$_H$	PCN27 [R/W] B,H,W 00000000 000000-0		PCSR27 [W] H,W XXXXXXXX XXXXXXXX		PPG27

176 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

(4-1-5) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↑→SCS↑ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50~SCS53, SCS60~SCS63, SCS70~SCS73, SCS8~SCS11 SOT1 , SOT2, SOT5~SOT11		-	40	ns	
		SCS3 , SCS40~SCS43 SOT3 ,SOT4		-	300	ns	
SCS↓→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↑ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50		

*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock
*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock
*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3.

(4-4) I^2C timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Standard mode		Fast mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK3 to SCK11	C_L=50pF R = (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK3 to SCK11, (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK3 to SCK11, (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK3 to SCK11, (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		250	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT3 to SOT11, (SDA) SCK3 to SCK11, (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	$2t_{CPP}$ *4	–	$2t_{CPP}$ *4	–	ns	

Notes: Only ch.3 and ch.4 are standard mode/fast mode correspondence. In ch.5-ch.8, ch.10, and ch.11, only a standard mode is correspondences.

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.
Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A fast mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of

(11) External bus I/F (asynchronous mode) timing
(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	V_{CC}=5.0V±10% *1
			31.25			V_{CC}=3.3V±0.3V
Address setup → RDX↑time	t_{ASRH}	RDX A00 to A21	2×t_{CYC} - 12	2×t_{CYC} + 12	ns	RWT=1, set RWT to 1 or more. *2
RDX↑→ Address hold	t_{RHAH}		t_{CYC} - 12	t_{CYC} + 12	ns	Set RDCS to 1 or more.
Data setup→ RDX↑time	t_{DSRH}	RDX D16 to D31	18 + t_{CYC}	-	ns	RWT=1, set RWT to 1 or more.
RDX↑→ Data hold	t_{RHDH}		0	-	ns	
Address setup→ WRnX↑time	t_{ASWH}	WR0X to WR1X A00 to A21	t_{CYC} - 12	t_{CYC} + 12	ns	WWT=0 *2
WRnX↑→ Address hold	t_{WHAH}		t_{CYC} - 12	t_{CYC} + 12	ns	Set WRCS to 1 or more.
Data setup→ WRnX↑time	t_{DSWH}	WR0X to WR1X D16 to D31	t_{CYC} - 16	t_{CYC} + 16	ns	WWT=0 *2
WRnX↑→ Data hold	t_{WHDH}		t_{CYC} - 16	t_{CYC} + 16	ns	Set WRCS to 1 or more.
Address setup → ASX↑time	t_{MASASH}	ASX D16 to D31	t_{CYC}-16	t_{CYC}+ 16	ns	ASCY=0
ASX↑→Address hold	t_{MASHAH}		t_{CYC}-16	t_{CYC} + 16	ns	In multiplex mode, set as follows: ☐Set CSWR and CSRD to 2 or more. ☐ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

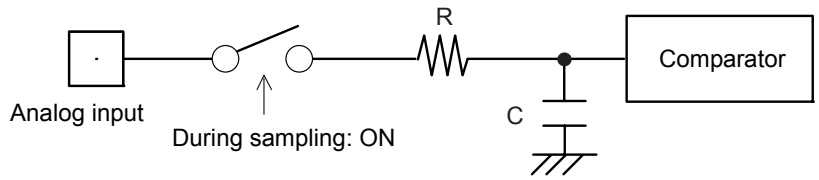
*1: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).
*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

- Analog input circuit model



	R	C	
12bit A/D	1.9kΩ (Max)	8.30pF (Max)	(4.5V ≤ AV_{CC} ≤ 5.5V)
	4.3kΩ (Max)	8.30pF (Max)	(3.0V ≤ AV_{CC} ≤ 3.6V)

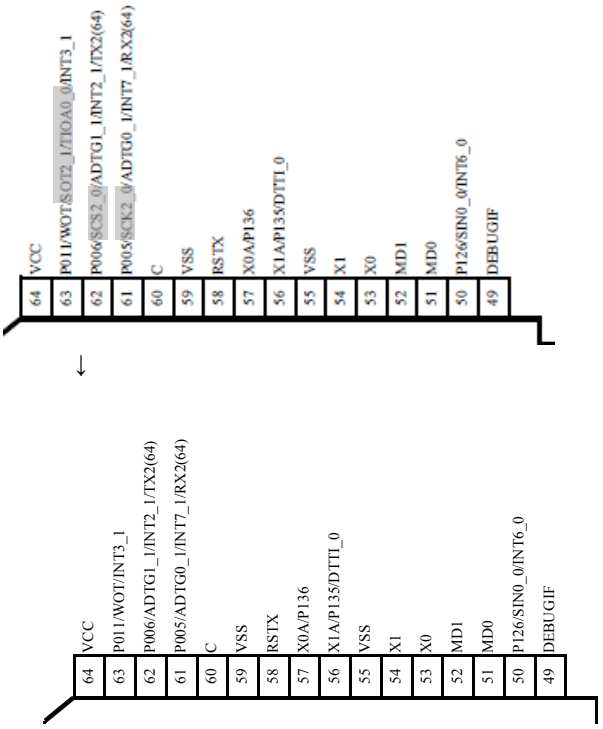
Note: Listed values must be considered as reference values.

13. Ordering Information MB91F52xxxB[*1]

Part number	Sub clock	CSV Initial value	LVD Initial value	Package[*2]
MB91F526LWBPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LYBPMC			OFF	
MB91F526LJBPMC		OFF	ON	
MB91F526LLBPMC			OFF	
MB91F525LWBPMC		ON	ON	
MB91F525LYBPMC			OFF	
MB91F525LJBPMC		OFF	ON	
MB91F525LLBPMC			OFF	
MB91F524LWBPMC		ON	ON	
MB91F524LYBPMC			OFF	
MB91F524LJBPMC		OFF	ON	
MB91F524LLBPMC			OFF	
MB91F523LWBPMC		ON	ON	
MB91F523LYBPMC			OFF	
MB91F523LJBPMC		OFF	ON	
MB91F523LLBPMC			OFF	
MB91F522LWBPMC		ON	ON	
MB91F522LYBPMC			OFF	
MB91F522LJBPMC		OFF	ON	
MB91F522LLBPMC			OFF	
MB91F526LSBPMC	None	ON	ON	
MB91F526LUBPMC			OFF	
MB91F526LHBPMC		OFF	ON	
MB91F526LKBPMC			OFF	
MB91F525LSBPMC		ON	ON	
MB91F525LUBPMC			OFF	
MB91F525LHBPMC		OFF	ON	
MB91F525LKBPMC			OFF	
MB91F524LSBPMC		ON	ON	
MB91F524LUBPMC			OFF	
MB91F524LHBPMC		OFF	ON	
MB91F524LKBPMC			OFF	
MB91F523LSBPMC		ON	ON	
MB91F523LUBPMC			OFF	
MB91F523LHBPMC		OFF	ON	
MB91F523LKBPMC			OFF	
MB91F522LSBPMC		ON	ON	
MB91F522LUBPMC			OFF	
MB91F522LHBPMC		OFF	ON	
MB91F522LKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526FWBPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FYBPMC			OFF	
MB91F526FJBPMC		OFF	ON	
MB91F526FLBPMC			OFF	
MB91F525FWBPMC		ON	ON	
MB91F525FYBPMC			OFF	
MB91F525FJBPMC		OFF	ON	
MB91F525FLBPMC			OFF	
MB91F524FWBPMC		ON	ON	
MB91F524FYBPMC			OFF	
MB91F524FJBPMC		OFF	ON	
MB91F524FLBPMC			OFF	
MB91F523FWBPMC		ON	ON	
MB91F523FYBPMC			OFF	
MB91F523FJBPMC		OFF	ON	
MB91F523FLBPMC			OFF	
MB91F522FWBPMC		ON	ON	
MB91F522FYBPMC			OFF	
MB91F522FJBPMC		OFF	ON	
MB91F522FLBPMC			OFF	
MB91F526FSBPMC	None	ON	ON	
MB91F526FUBPMC			OFF	
MB91F526FHBPMC		OFF	ON	
MB91F526FKBPMC			OFF	
MB91F525FSBPMC		ON	ON	
MB91F525FUBPMC			OFF	
MB91F525FHBPMC		OFF	ON	
MB91F525FKBPMC			OFF	
MB91F524FSBPMC		ON	ON	
MB91F524FUBPMC			OFF	
MB91F524FHBPMC		OFF	ON	
MB91F524FKBPMC			OFF	
MB91F523FSBPMC		ON	ON	
MB91F523FUBPMC			OFF	
MB91F523FHBPMC		OFF	ON	
MB91F523FKBPMC			OFF	
MB91F522FSBPMC		ON	ON	
MB91F522FUBPMC			OFF	
MB91F522FHBPMC		OFF	ON	
MB91F522FKBPMC			OFF	

Page	Section	Change Results
8	■Product Lineup	Corrected the following description for Product lineup comparison(100 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
8	■Product Lineup	Added the following sentences under Product lineup comparison(100 pin) *1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
9	■Product Lineup	Corrected the following description for Product lineup comparison(120 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
9	■Product Lineup	Added the following sentences under Product lineup comparison(120 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
10	■Product Lineup	Corrected the following description for Product lineup comparison(144 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
10	■Product Lineup	Added the following sentences under Product lineup comparison(144 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).
11	■Product Lineup	Corrected the following description for Product lineup comparison(176 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
11	■Product Lineup	Added the following sentences under Product lineup comparison(176 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

Page	Section	Change Results
13	■Pin Assignment MB91F52xB	- Top 
13	■Pin Assignment MB91F52xB	The following note added on the bottom left of Figure. * In a single clock product, pin 56 and pin 57 are the general-purpose ports.

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>131</td><td>■Interrupt Vector Table</td><td>"42" is deleted as shown below from the interrupt factor in Interrupt vector 120pin.

(Error)
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/42/43
16-bit free-run timer 2 (0 detection) / (compare clear)</td><td>41</td><td>29</td><td>ICR 25</td><td>358 H</td><td>000F FF58 H</td><td>25 *3</td></tr>
</table>

(Correct)
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/43
16-bit free-run timer 2 (0 detection) / (compare clear)</td><td>41</td><td>29</td><td>ICR 25</td><td>358 H</td><td>000F FF58 H</td><td>25 *3</td></tr>
</table>
</td></tr>
<tr><td>133</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 120pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0
Base timer 1 IRQ1
–
–</td><td>61</td><td>3D</td><td>ICR 45</td><td>308 H</td><td>000F FF08 H</td><td>45 *5</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0
Base timer 1 IRQ1
–
–</td><td>61</td><td>3D</td><td>ICR 45</td><td>308 H</td><td>000F FF08 H</td><td>45</td></tr>
</table>
</td></tr>
<tr><td>133</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 120pins.

(Error)
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>

Page	Section	Change Results
143	■Electrical Characteristics 1. Absolute Maximum Ratings	The following note added. (Correct) *9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.
155	■Electrical Characteristics AC Characteristics (2) Reset Input	Added the At power-on*2 condition to the remarks in Reset input time.
156	■Electrical Characteristics AC Characteristics (3) Power-on Conditions	Deleted the Slope detection undetected specification. Added the Power ramp rate and C pin voltage at Power-on. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on.
6 to 11, 203 to 216	■Product lineup ■Ordering information	Package description modified to JEDEC description.
47	■During Power-on	The following sentence modified as fdeleted from Interrupt (Error) To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.
49, 50	■Block Diagram	The following Block diagram modified as follows: ●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B ●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D (Error) CAN (2ch). (Correct) CAN (3ch)
217 to 220	■Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxD
221 to 227	■Package Dimensions	Package Dimensions modified to JEDEC description.