Infineon Technologies - MB91F524DSCPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f524dscpmc-gse2

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444_H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448_H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
$00044C_H$	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450_H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454_H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458_H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
$00045C_H$	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460_H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464_H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468_H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
$00046C_H$	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470_H to $00047C_H$	—	—	—	—	Reserved [S]
000480_H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484_H	—	—	—	—	Reserved [S]
000488_H	DIVR0 [R/W] B,H,W 000-----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
$00048C_H$	—	—	—	—	Reserved [S]
000490_H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494_H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498_H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CF0_H$	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000CF4_H$	DCSR15 [R/W] H 0------- -----000		DTCR15 [R/W] H 00000000 00000000		
$000CF8_H$	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CFC_H$	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000D00_H$ to $000DF0_H$	—	—	—	—	Reserved [S]
$000DF4_H$	—	—	DNMIR [R/W] B 0------0	DILVR [R/W] B ---11111	DMA Controller [S]
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	—	—	—	—	Reserved [S]
$000E00_H$	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
$000E04_H$	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
$000E08_H$	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register
$000E0C_H$	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -0000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000	
$000E10_H$	—	—	—	—	
$000E14_H$	—	—	—	—	
$000E18_H$	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
$000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
$000E24_H$	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
$000E28_H$	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
$000E2C_H$	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
$000E30_H$	—	—	—	—	
$000E34_H$	—	—	—	—	
$000E38_H$	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001434_H	ADRCCS24[R/W] B,H,W 00000000	ADRCCS25[R/W] B,H,W 00000000	ADRCCS26[R/W] B,H,W 00000000	ADRCCS27[R/W] B,H,W 00000000	12-bit A/D converter 1/2 unit
001438_H	ADRCCS28[R/W] B,H,W 00000000	ADRCCS29[R/W] B,H,W 00000000	ADRCCS30[R/W] B,H,W 00000000	ADRCCS31[R/W] B,H,W 00000000	
$00143C_H$	ADRCOT0[R] B,H,W 00000000 00000000 00000000 00000000				
001440_H	ADRCIF0[R,W] B,H,W 00000000 00000000 00000000 00000000				
001444_H	ADSCANS0[R/W] B,H,W 000-----	—	—	—	
001448_H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	
$00144C_H$	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00	
001450_H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00	
001454_H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00	
001458_H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000				
$00145C_H$	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111				
001460_H	ADCS0[R] B,H,W 0------- --------		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0---0000	
001464_H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000	
001468_H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000	
$00146C_H$	—				12-bit A/D converter 2/2 unit
001470_H	ADTSS1[R/W] B,H,W -------0	—	—	—	
001474_H	ADTSE1[R/W] B,H,W -------- -------- 00000000 00000000				
001478_H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001804_H	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001808_H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
$00180C_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810_H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814_H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818_H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00181C_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820_H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824_H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828_H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
$00182C_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830_H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834_H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838_H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
$00183C_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001A80_H$	PCN202 [R/W] B,H,W --000000 -----110		PSDR2 [R/W] H,W 00000000 00000000		PPG2 * for communication
$001A84_H$	PTPC2 [R/W] H,W 00000000 00000000		PCMDWD2 [R/W] B,H,W -------- ----0000		
$001A88_H$	PHCSR2 [W] H,W XXXXXXXX XXXXXXXX		PLCSR2 [W] H,W XXXXXXXX XXXXXXXX		
$001A8C_H$	PHDUT2 [W] H,W XXXXXXXX XXXXXXXX		PLDUT2 [W] H,W XXXXXXXX XXXXXXXX		
$001A90_H$	PCMDDT2 [R/W] H,W 00000000 00000000		—	—	
$001A94_H$	PCN3 [R/W] B,H,W 00000000 000000-0		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3 * for communication
$001A98_H$	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PTMR3 [R] H,W 11111111 11111111		
$001A9C_H$	PCN203 [R/W] B,H,W --000000 -----110		PSDR3 [R/W] H,W 00000000 00000000		
$001AA0_H$	PTPC3 [R/W] H,W 00000000 00000000		PCMDWD3 [R/W] B,H,W -------- ----0000		
$001AA4_H$	PHCSR3 [W] H,W XXXXXXXX XXXXXXXX		PLCSR3 [W] H,W XXXXXXXX XXXXXXXX		
$001AA8_H$	PHDUT3 [W] H,W XXXXXXXX XXXXXXXX		PLDUT3 [W] H,W XXXXXXXX XXXXXXXX		
$001AAC_H$	PCMDDT3 [R/W] H,W 00000000 00000000		—	—	
$001AB0_H$	PCN4 [R/W] B,H,W 00000000 000000-0		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
$001AB4_H$	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PTMR4 [R] H,W 11111111 11111111		
$001AB8_H$	PCN204 [R/W] B,H,W --000000 -----110		PSDR4 [R/W] H,W 00000000 00000000		
$001ABC_H$	PTPC4 [R/W] H,W 00000000 00000000		—	—	PPG4
$001AC0_H$	PCN5 [R/W] B,H,W 00000000 000000-0		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
$001AC4_H$	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PTMR5 [R] H,W 11111111 11111111		
$001AC8_H$	PCN205 [R/W] B,H,W --000000 -----110		PSDR5 [R/W] H,W 00000000 00000000		
$001ACC_H$	PTPC5 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001C24_H$	PDUT27 [W] H,W XXXXXXXX XXXXXXXX		PTMR27 [R] H,W 11111111 11111111		PPG27
$001C28_H$	PCN227 [R/W] B,H,W --000000 -----110		PSDR27 [R/W] H,W 00000000 00000000		
$001C2C_H$	PTPC27 [R/W] H,W 00000000 00000000		—	—	PPG27
$001C30_H$	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
$001C34_H$	PDUT28 [W] H,W XXXXXXXX XXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
$001C38_H$	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
$001C3C_H$	PTPC28 [R/W] H,W 00000000 00000000		—	—	
$001C40_H$	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
$001C44_H$	PDUT29 [W] H,W XXXXXXXX XXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
$001C48_H$	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
$001C4C_H$	PTPC29 [R/W] H,W 00000000 00000000		—	—	
$001C50_H$	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
$001C54_H$	PDUT30 [W] H,W XXXXXXXX XXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
$001C58_H$	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
$001C5C_H$	PTPC30 [R/W] H,W 00000000 00000000		—	—	
$001C60_H$	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
$001C64_H$	PDUT31 [W] H,W XXXXXXXX XXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
$001C68_H$	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
$001C6C_H$	PTPC31 [R/W] H,W 00000000 00000000		—	—	
$001C70_H$	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
$001C74_H$	PDUT32 [W] H,W XXXXXXXX XXXXXXXX		PTMR32 [R] H,W 11111111 11111111		

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
-	38	26	ICR22	364_H	$000FFF64_H$	-*6
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358_H	$000FFF58_H$	25*3
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/15/24/35	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/18/19/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29
Main timer	46	2E	ICR30	344_H	$000FFF44_H$	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0/1/2 WG dead timer reload 0/1/2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40

DC Characteristics

(T_A: -40°C to +105°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	80	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	90	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	90	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	71	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	81	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	81	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	62	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	72	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	72	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	61	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	51	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation, Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

(T_A: -40°C to +125°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	102	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	115	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	115	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	92	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	105	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	105	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	82	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	95	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	95	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	82	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	72	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation , Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

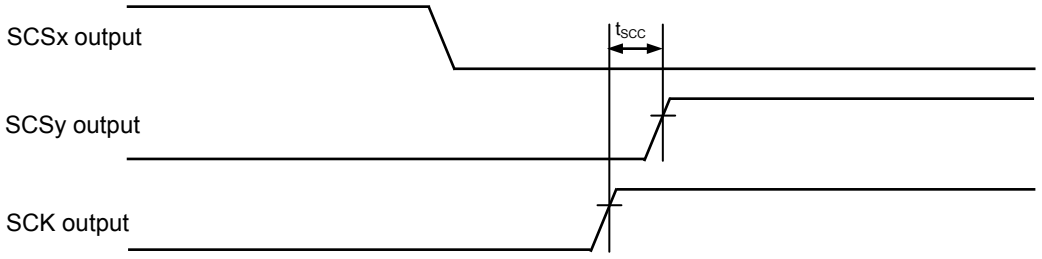
Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	-	ns	WWT=0 *2
SYSCLK↑→ data output time	t_{CHDV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t_{CHDX}		-	18	ns	Set WRCS to 1 or more.
SYSCLK↑→ address output time	t_{CHMAV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: □Set CSWR and CSRD to 2 or more. □ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

*1: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

Page	Section	Change Results
19	■PIN Description	(Continued) (Correct)

Pin no.						Pin Name
64	80	100	120	144	176	
-	-	-	-	2	2	P015 D29 TRG0_0
-	-	-	-	3	3	P016 D30 TRG1_0
-	-	-	-	-	4	P170 PPG36_1
-	-	-	-	4	5	P017 D31 TRG2_0
-	-	-	-	-	6	P171 PPG37_1
2 *1	2 *1	2 *1	2 *1	5	7	P020 ASX *2, *3, *4, *5 SIN3_1 TRG3_0 TIN0_2 RTO5_1
-	-	-	3 *1	6	8	P021 CS0X *5 SOT3_1 TRG6_1 TRG4_0
-	-	-	4 *1	7	9	P022 CS1X *5 SCK3_1 TRG7_1 TRG5_0
-	-	-	5 *1	8	10	P023 RDX *5 SCS3_1 PPG32_0 TIN0_0
3 *1	3 *1	3 *1	6 *1	9	11	P024 WR0X *2, *3, *4, *5 SIN4_1 PPG24_0 TIN1_0 RTO4_1 INT15_0

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>24</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table><tr><th>Function*2</th></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External Bus chip select 2 output pin(0)</td></tr><tr><td>Multi-function serial ch.10 serial data input pin(0)</td></tr><tr><td>ADC analog 43 input pin</td></tr><tr><td>PPG ch.37 output pin(0)</td></tr><tr><td>Reload timer ch.4 event input pin(1)</td></tr></table>
(Correct)
<table><tr><th>Function*9</th></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External Bus chip select 2 output pin</td></tr><tr><td>Multi-function serial ch.10 serial data input pin(0)</td></tr><tr><td>ADC analog 43 input pin</td></tr><tr><td>PPG ch.37 output pin(0)</td></tr><tr><td>Reload timer ch.4 event input pin(1)</td></tr></table></td></tr>
</table>

Page	Section	Change Results
24	■PIN Description	A List of "Pin Description" modified. (Error) Function*2 General-purpose I/O port External Bus chip select 3 output pin(0) Input capture ch.9 input pin(0) PPG ch.0 output pin(1) Input capture ch.0 input pin(1) Reload timer ch.5 event input pin(1) Waveform generator ch.0 to ch.5 input pin(2) (Correct) Function*9 General-purpose I/O port External Bus chip select 3 output pin Input capture ch.9 input pin(0) PPG ch.0 output pin(1) Input capture ch.0 input pin(1) Reload timer ch.5 event input pin(1) Waveform generator ch.0 to ch.5 input pin(2)

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>141</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 176pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45 *5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
<tr><td>141</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 176pins.

(Error)
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>142</td><td>■Electrical Characteristics
1. Absolute Maximum Ratings</td><td>The remarks of "L" level average output current" and "H" level average output current" modified as follows.

(Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td rowspan="2">"L" level average output current *4</td><td>I_{OLAV1}</td><td>-</td><td>4</td><td>mA</td><td rowspan="2"></td></tr>
<tr><td>I_{OLAV2}</td><td>-</td><td>12</td><td>mA</td></tr>
<tr><td rowspan="2">"H" level average output current *4</td><td>I_{OHAV1}</td><td>-</td><td>-4</td><td>mA</td><td></td></tr>
<tr><td>I_{OHAV2}</td><td>-</td><td>-12</td><td>mA</td><td></td></tr>
</table>

(Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td rowspan="2">"L" level average output current *4</td><td>I_{OLAV1}</td><td>-</td><td>4</td><td>mA</td><td>*9</td></tr>
<tr><td>I_{OLAV2}</td><td>-</td><td>12</td><td>mA</td><td>*10</td></tr>
<tr><td rowspan="2">"H" level average output current *4</td><td>I_{OHAV1}</td><td>-</td><td>-4</td><td>mA</td><td>*9</td></tr>
<tr><td>I_{OHAV2}</td><td>-</td><td>-12</td><td>mA</td><td>*10</td></tr>
</table>
</td></tr>
</table>

Page	Section	Change Results
46	■During Power-on	The following sentence modified as following: (Error) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.
142,143	11. Electrical Characteristics Recommended operating conditions	The following sentence modified as following: (Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset. (Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
156, 157	11. Electrical Characteristics AC Characteristics	Added (3-2) Power-on Conditions for MB91F52xxxE

Page	Section	Change Results
220 to 223	16. Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxE
Rev *D		
1	Features	The following sentence should be modified as follows: (Error) Conversion time : 1µs (Correct) Conversion time : 1.4µs
5,6,7,8,9,10	1. Product Lineup	The following sentence should be modified as follows: (Error) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. (Correct) *2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Page	Section	Change Results
188	11. Electrical Characteristics (9) Low voltage detection (Internal low-voltage detection)	The following sentence modified as following: (Error) (9) Low voltage detection (RAM retention low-voltage detection) (Correct) (9) Low voltage detection (Internal low-voltage detection)
		The following symbol should be modified as follows: (Error) * (Correct) *1
		Note of Detection voltage should be added as follows: (Correct) Detection voltage *2 *2: The detection voltage of the internal low voltage detection is 0.9V±0.1V. This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
233 to 235	18. Errata	Limitation for Watch mode (power off) should be added in Errata.

Document History

Document Title: MB91520 Series 32-bit FR81S Microcontroller
Document Number: 002-04662

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	–	–	Initial release
	–	–	2/20/2014	Features: Corrected the following description. 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input ↓ 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input I/O CIRCUIT TYPE: Corrected the following description to "Type F, G, I, J, K, M". Schmitt input → CMOS hysteresis input