Infineon Technologies - MB91F524FHCPMC-GS-F4E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f524fhcpmc-gs-f4e1

Product lineup comparison 80 pins

	MB91F522D	MB91F523D	MB91F524D	MB91F525D	MB91F526D
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch, 32bit×2ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×27ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×16ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	9ch*1				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	56 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V *2				
Package	LQH080				

*1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 100 pins

	MB91F522F	MB91F523F	MB91F524F	MB91F525F	MB91F526F
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×34ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×21ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch[*1]				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	76 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V [*2]				
Package	LQI100				

*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 144 pins

	MB91F522K	MB91F523K	MB91F524K	MB91F525K	MB91F526K
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	Yes				
DMA Transfer	16ch				
16-bit Base Timer	2ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×44ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×32ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch*1				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	120 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V *2				
Package	LQS144, LQN144				

*1: Only channel 3 and channel 4 support the I^2C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

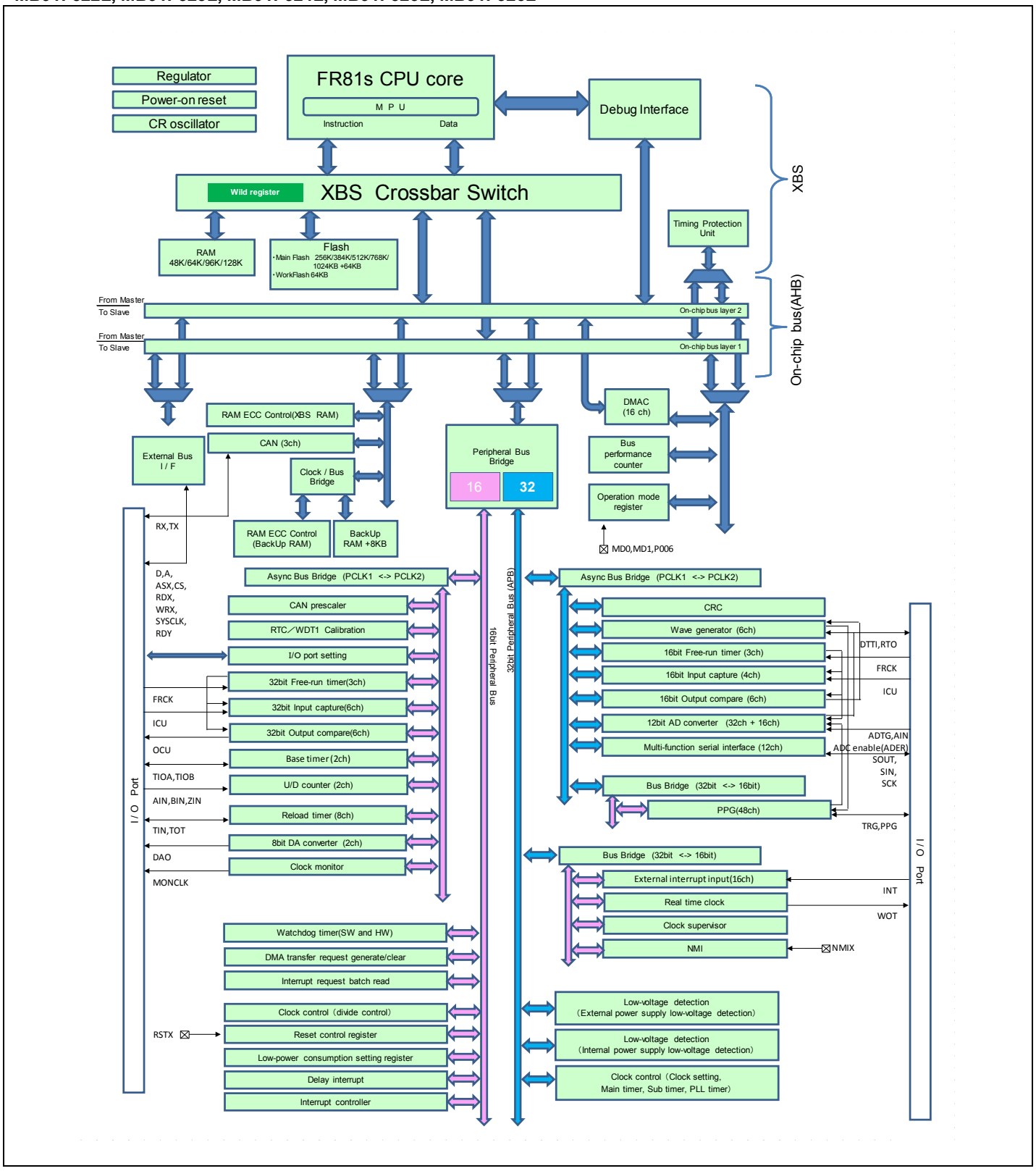
Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	40	46	54	68	P070	-	A	General-purpose I/O port
						ICU0_2	-		Input capture ch.0 input (2)
26	33	41	47	55	69	P071	-	G	General-purpose I/O port
						SCK4_2	-		Multi-function serial ch.4 clock I/O (2)
						AN35	-		ADC analog 35 input
						ICU1_2	-		Input capture ch.1 input (2)
						MONCLK	-		Clock monitor output pin
27	34	42	48	56	70	P072	-	G	General-purpose I/O port
						SIN4_0	-		Multi-function serial ch.4 serial data input (0)
						AN34	-		ADC analog 34 input
						ICU2_2	-		Input capture ch.2 input (2)
						INT5_0	-		INT5 External interrupt input (0)
-	35 *3	43 *4	49	57	71	P073	-	D	General-purpose I/O port
						SOT4_0/ SDA4 *3, *4	-		Multi-function serial ch.4 serial data output (0)/I^{2}C bus serial data I/O
						AN33	-		ADC analog 33 input
						ICU3_2	-		Input capture ch.3 input (2)
-	-	-	-	-	72	P186	-	A	General-purpose I/O port
						PPG46_0	-		PPG ch.46 output (0)
-	-	-	-	-	73	P187	-	A	General-purpose I/O port
						PPG47_0	-		PPG ch.47 output (0)
-	-	-	50	58	74	P074	-	E	General-purpose I/O port
						SCK4_0/ SCL4	-		Multi-function serial ch.4 clock I/O (0)/ I^{2}C bus serial clock I/O
-	-	-	51	59	75	P075	-	F	General-purpose I/O port
						SIN3_0	-		Multi-function serial ch.3 serial data input (0)
						INT4_0	-		INT4 External interrupt input (0)
-	-	-	52	60	76	P076	-	E	General-purpose I/O port
						SOT3_0/ SDA3	-		Multi-function serial ch.3 serial data output (0)/I^{2}C bus serial data I/O
-	-	-	53	61	77	P077	-	E	General-purpose I/O port
						SCK3_0/ SCL3	-		Multi-function serial ch.3 clock I/O (0)/ I^{2}C bus serial clock I/O
-	-	44	54	62	78	P152	-	A	General-purpose I/O port
						SCS53_0	-		Serial chip select 53 output (0)
28	36	45	55	63	79	P153	-	G	General-purpose I/O port
						SCK5_0/ SCL5	-		Multi-function serial ch.5 clock I/O (0)/ I^{2}C bus serial clock I/O
						AN32	-		ADC analog 32 input
						FRCK1_1	-		Free-run timer 1 clock input (1)
						INT4_1	-		INT4 External interrupt input (1)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	48 *1	59	69	85	104	P100	-	G	General-purpose I/O port
						SCK7_0/ SCL7 *3	-		Multi-function serial ch.7 clock I/O (0)/ I^2C bus serial clock I/O
						AN12	-		ADC analog 12 input
						PPG8_0	-		PPG ch.8 output (0)
-	-	60	70	86	105	P101	-	G	General-purpose I/O port
						SOT7_0/ SDA7	-		Multi-function serial ch.7 serial data output (0)/I^2C bus serial data I/O
						AN13	-		ADC analog 13 input
						PPG9_0	-		PPG ch.9 output (0)
40 *1	49 *1	61	71	87	106	P102	-	G	General-purpose I/O port
						SIN7_0 *2, *3	-		Multi-function serial ch.7 serial data input (0)
						AN14	-		ADC analog 14 input
						PPG10_0	-		PPG ch.10 output (0)
						INT10_0	-		INT10 External interrupt input (0)
41 *1	50 *1	62	72	88	107	P103	-	H	General-purpose I/O port
						SCS73_0 *2, *3	-		Serial chip select 73 output (0)
						AN15	-		ADC analog 15 input
						PPG11_0	-		PPG ch.11 output (0)
42 *1	51 *1	63	73	89	108	P104	-	H	General-purpose I/O port
						SCS72_0 *2, *3	-		Serial chip select 72 output (0)
						AN16	-		ADC analog 16 input
						PPG12_0	-		PPG ch.12 output (0)
43 *1	52 *1	64	74	90	109	P105	-	H	General-purpose I/O port
						SCS71_0 *2, *3	-		Serial chip select 71 output (0)
						AN17	-		ADC analog 17 input
						PPG13_0	-		PPG ch.13 output (0)
-	-	65	75	91	110	P106	-	H	General-purpose I/O port
						SCS70_0	-		Serial chip select 70 I/O (0)
						AN18	-		ADC analog 18 input
						PPG14_0	-		PPG ch.14 output (0)
-	53	66	76	92	111	P107	-	B	General-purpose I/O port
						AN19	-		ADC analog 19 input
						PPG15_0	-		PPG ch.15 output (0)
-	-	-	-	-	112	P193	-	A	General-purpose I/O port
						PPG25_1	-		PPG ch.25 output (1)
-	-	-	77	93	113	P154	-	B	General-purpose I/O port
						AN20	-		ADC analog 20 input
-	-	-	78	94	114	P155	-	B	General-purpose I/O port
						AN21	-		ADC analog 21 input

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	113 *1	133	161	P002	-	F	General-purpose I/O port
						D18 *5	-		External bus data bit18 I/O
						SCK1_0	-		Multi-function serial ch.1 clock I/O (0)
						TIOB0_1	-		TIOB input of Base timer ch.0 (1)
-	76 *1	96 *1	114 *1	134	162	P003	-	F	General-purpose I/O port
						D19 *3, *4, *5	-		External bus data bit19 I/O
						SIN2_0	-		Multi-function serial ch.2 serial data input (0)
						TIOB1_1	-		TIOB input of Base timer ch.1 (1)
						INT3_0	-		INT3 External interrupt input (0)
-	-	-	-	135	163	P004	-	A	General-purpose I/O port
						D20	-		External bus data bit20 I/O (0)
						SOT2_0	-		Multi-function serial ch.2 serial data output (0)
-	-	-	-	-	164	P164	-	A	General-purpose I/O port
						PPG32_1	-		PPG ch.32 output (1)
61 *1	77 *1	97 *1	115 *1	136 *1	165 *1	P005	-	F	General-purpose I/O port
						D21 *2, *3, *4, *5	-		External bus data bit21 I/O (0)
						SCK2_0 *2	-		Multi-function serial ch.2 clock I/O (0)
						ADTG0_1	-		A/D converter external trigger input 0 (1)
						INT7_1	-		INT7 External interrupt input (1)
						RX2(64) *4, *5, *6, *7	-		CAN reception data 2 input
-	-	-	-	-	166	P165	-	A	General-purpose I/O port
						PPG33_1	-		PPG ch.33 output (1)
62 *1	78 *1	98 *1	116 *1	137 *1	167 *1	P006	-	A	General-purpose I/O port
						D22 *2, *3, *4, *5	-		External bus data bit22 I/O (0)
						SCS2_0 *2	-		Serial chip select 2 I/O (0)
						ADTG1_1	-		A/D converter external trigger input 1 (1)
						INT2_1	-		INT2 External interrupt input (1)
						TX2(64) *4, *5, *6, *7	-		CAN transmission data 2 output
-	-	-	117 *1	138	168	P007	-	A	General-purpose I/O port
						D23 *5	-		External bus data bit23 I/O
-	-	-	-	-	169	P166	-	A	General-purpose I/O port
						PPG34_1	-		PPG ch.34 output (1)
-	-	-	118 *1	139	170	P010	-	A	General-purpose I/O port
						D24 *5	-		External bus data bit24 I/O

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
63 *1	79 *1	99 *1	119 *1	140	171	P011	-	A	General-purpose I/O port
						WOT	-		RTC output signal
						D25 *2, *3, *4, *5	-		External bus data bit25 I/O
						SOT2_1 *2	-		Multi-function serial ch.2 serial data output (1)
						TIOA0_0 *2, *3, *4	-		TIOA output of Base timer ch.0 (0)
						INT3_1	-		INT3 External interrupt input (1)
-	-	-	-	141	172	P012	-	A	General-purpose I/O port
						D26	-		External bus data bit26 I/O
						TIOB0_0	-		TIOB input of Base timer ch.0 (0)
-	-	-	-	-	173	P167	-	A	General-purpose I/O port
						PPG35_1	-		PPG ch.35 output (1)
-	-	-	-	142	174	P013	-	A	General-purpose I/O port
						D27	-		External bus data bit27 I/O
						TIOA1_0	-		TIOA I/O of Base timer ch.1 (0)
-	-	-	-	143	175	P014	-	A	General-purpose I/O port
						D28	-		External bus data bit28 I/O
						TIOB1_0	-		TIOB input of Base timer ch.1 (0)
18	23	28	34	40	50	AVCC1	-	-	Analog power supply for AD/DA convertor unit1
39	47	58	68	84	103	AVCC0	-	-	Analog power supply for AD/DA convertor unit0
20	25	30	36	42	52	AVRH1	-	-	Upper limit reference voltage for AD convertor unit1
38	46	57	67	83	102	AVRH0	-	-	Upper limit reference voltage for AD convertor unit0
21	26	31	37	43	53	AVSS1/ AVRL1	-	-	GND for AD/DA convertor unit1 Lower limit reference voltage for AD convertor unit1
37	45	56	66	82	101	AVSS0/ AVRL0	-	-	GND for AD/DA convertor unit0 Lower limit reference voltage for AD convertor unit0
60	74	93	110	130	158	C	-	-	External capacity connection output
-	20	25	30	36	44	VCC	-	-	+5.0V power supply
32	40	50	60	72	88				
-	61	76	91	109	133				
64	80	100	120	144	176				
1	1	1	1	1	1	VSS	-	-	GND
-	21	26	31	37	45				
33	41	51	61	73	89				
-	60	75	90	108	132				
55	69	85	101	120	148				
59	73	92	109	129	157				

MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001588_H	ADRCCS32[R/W] B,H,W 00000000	ADRCCS33[R/W] B,H,W 00000000	ADRCCS34[R/W] B,H,W 00000000	ADRCCS35[R/W] B,H,W 00000000	12-bit A/D converter 2/2 unit
$00158C_H$	ADRCCS36[R/W] B,H,W 00000000	ADRCCS37[R/W] B,H,W 00000000	ADRCCS38[R/W] B,H,W 00000000	ADRCCS39[R/W] B,H,W 00000000	
001590_H	ADRCCS40[R/W] B,H,W 00000000	ADRCCS41[R/W] B,H,W 00000000	ADRCCS42[R/W] B,H,W 00000000	ADRCCS43[R/W] B,H,W 00000000	
001594_H	ADRCCS44[R/W] B,H,W 00000000	ADRCCS45[R/W] B,H,W 00000000	ADRCCS46[R/W] B,H,W 00000000	ADRCCS47[R/W] B,H,W 00000000	
001598_H to $0015A4_H$	—	—	—	—	Reserved
$0015A8_H$	ADRCOT1 [R] B,H,W -------- -------- 00000000 00000000				12-bit A/D converter 2/2 unit
$0015AC_H$	ADRCIF1 [R,W] B,H,W -------- -------- 00000000 00000000				
$0015B0_H$	ADSCANS1 [R/W] B,H,W 000-----	—	—	—	
$0015B4_H$	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	
$0015B8_H$	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00	
$0015BC_H$	—	—	—	—	
$0015C0_H$	—	—	—	—	
$0015C4_H$	ADPRTF1 [R] B,H,W -------- -------- 00000000 00000000				12-bit A/D converter 2/2 unit
$0015C8_H$	ADEOCF1 [R] B,H,W -------- -------- 11111111 11111111				
$0015CC_H$	ADCS1 [R] B,H,W 0------- --------		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000	
$0015D0_H$	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000	
$0015D4_H$ to $00174C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017C8H	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000-00-0	SSR3[R/W] B,H,W 0-000011	ESCR3/(IBSR3)[R/W] B,H,W 00000000	Multi-UART3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017CCH	— /(RDR13/(TDR13))[R/W] B,H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
0017D0H	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
0017D4H	STMCR3[R/W] B,H,W 00000000 00000000		— /(SCSCR3/SFUR3)[R/W] B,H,W -------- -------- *3 *4		
0017D8H	— /(SCSTR33)/ (LAMSR3) [R/W] B,H,W -------- *3	— /(SCSTR23)/ (LAMCR3) [R/W] B,H,W -------- *3	— /(SCSTR13)/ (SFLR13) [R/W] B,H,W -------- *3	— /(SCSTR03)/ (SFLR03) [R/W] B,H,W -------- *3	
0017DCH	—	— /(SCSFR23) [R/W] B,H,W -------- *3	— /(SCSFR13) [R/W] B,H,W -------- *3	— /(SCSFR03) [R/W] B,H,W -------- *3	
0017E0H	—/(TBYTE33)/ (LAMESR3) [R/W] B,H,W -------- *3	—/(TBYTE23)/ (LAMERT3) [R/W] B,H,W -------- *3	—/(TBYTE13)/ (LAMIER3) [R/W] B,H,W -------- *3	TBYTE03/(LAMRID3) / (LAMTID3) [R/W] B,H,W 00000000	
0017E4H	BGR3[R/W] H, W 00000000 00000000		— /(ISMK3)[R/W] B,H,W -------- *2	— /(ISBA3)[R/W] B,H,W -------- *2	
0017E8H	FCR13[R/W] B,H,W ---00100	FCR03[R/W] B,H,W -0000000	FBYTE3[R/W] B,H,W 00000000 00000000		
0017ECH	FTICR3[R/W] B,H,W 00000000 00000000		—	—	
0017F0H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000-00-0	SSR4[R/W] B,H,W 0-000011	ESCR4/(IBSR4)[R/W] B,H,W 00000000	Multi-UART4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset.
0017F4H	— /(RDR14/(TDR14))[R/W] B,H,W -------- -------- *3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1		
0017F8H	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		
0017FCH	STMCR4[R/W] B,H,W 00000000 00000000		— /(SCSCR4/SFUR4)[R/W] B,H,W -------- -------- *3 *4		
001800H	— /(SCSTR34)/ (LAMSR4) [R/W] B,H,W -------- *3	— /(SCSTR24)/ (LAMCR4) [R/W] B,H,W -------- *3	— /(SCSTR14)/ (SFLR14) [R/W] B,H,W -------- *3	— /(SCSTR04)/ (SFLR04) [R/W] B,H,W -------- *3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001AD0_H$	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
$001AD4_H$	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
$001AD8_H$	PCN206 [R/W] B,H,W --000000 -----110		PSDR6 [R/W] H,W 00000000 00000000		
$001ADC_H$	PTPC6 [R/W] H,W 00000000 00000000		—	—	
$001AE0_H$	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
$001AE4_H$	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
$001AE8_H$	PCN207 [R/W] B,H,W --000000 -----110		PSDR7 [R/W] H,W 00000000 00000000		
$001AEC_H$	PTPC7 [R/W] H,W 00000000 00000000		—	—	
$001AF0_H$	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
$001AF4_H$	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
$001AF8_H$	PCN208 [R/W] B,H,W --000000 -----110		PSDR8 [R/W] H,W 00000000 00000000		
$001AFC_H$	PTPC8 [R/W] H,W 00000000 00000000		—	—	
$001B00_H$	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
$001B04_H$	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
$001B08_H$	PCN209 [R/W] B,H,W --000000 -----110		PSDR9 [R/W] H,W 00000000 00000000		
$001B0C_H$	PTPC9 [R/W] H,W 00000000 00000000		—	—	
$001B10_H$	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
$001B14_H$	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PTMR10 [R] H,W 11111111 11111111		
$001B18_H$	PCN210 [R/W] B,H,W --000000 -----110		PSDR10 [R/W] H,W 00000000 00000000		PPG10
$001B1C_H$	PTPC10 [R/W] H,W 00000000 00000000		—	—	
$001B20_H$	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001C24_H$	PDUT27 [W] H,W XXXXXXXX XXXXXXXX		PTMR27 [R] H,W 11111111 11111111		PPG27
$001C28_H$	PCN227 [R/W] B,H,W --000000 -----110		PSDR27 [R/W] H,W 00000000 00000000		
$001C2C_H$	PTPC27 [R/W] H,W 00000000 00000000		—	—	PPG27
$001C30_H$	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
$001C34_H$	PDUT28 [W] H,W XXXXXXXX XXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
$001C38_H$	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
$001C3C_H$	PTPC28 [R/W] H,W 00000000 00000000		—	—	
$001C40_H$	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
$001C44_H$	PDUT29 [W] H,W XXXXXXXX XXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
$001C48_H$	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
$001C4C_H$	PTPC29 [R/W] H,W 00000000 00000000		—	—	
$001C50_H$	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
$001C54_H$	PDUT30 [W] H,W XXXXXXXX XXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
$001C58_H$	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
$001C5C_H$	PTPC30 [R/W] H,W 00000000 00000000		—	—	
$001C60_H$	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
$001C64_H$	PDUT31 [W] H,W XXXXXXXX XXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
$001C68_H$	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
$001C6C_H$	PTPC31 [R/W] H,W 00000000 00000000		—	—	
$001C70_H$	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
$001C74_H$	PDUT32 [W] H,W XXXXXXXX XXXXXXXX		PTMR32 [R] H,W 11111111 11111111		

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed) / Multi-function serial interface ch.4 (status)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed) / Multi-function serial interface ch.5 (status)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed) / Multi-function serial interface ch.6 (status)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1 / RAM diagnosis end / RAM initialization completion / Error generation during RAM diagnosis / Backup RAM diagnosis end / Backup RAM initialization completion / Error generation during Backup RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-
CAN2 / Up/down counter 0 / Up/down counter 1	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed) / Multi-function serial interface ch.7 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*1
16-bit Free-running timer 0 (0 detection) / (compare clear) / Multi-function serial interface ch.7 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/21/30/31 / 16-bit Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
PPG 2/3/12/13/23/32/43 / 16-bit Free-run timer 2 (0 detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*3
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*1
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358_H	$000FFF58_H$	25*3
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	0.7× V_{CC}	-	V_{CC}	V	
	V_{IH3}	Port other than V_{IH1}	Automotive input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IH5}	RSTX,NMIX,MD0,MD1	CMOS hysteresis input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IHT}	DEBUGIF	TTL input level	2	-	V_{CC}	V	
"L" level input voltage	V_{IL1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	Vss	-	0.3× V_{CC}	V	
	V_{IL3}	Port other than V_{IH1}	Automotive input level	Vss	-	0.5× V_{CC}	V	
	V_{IL5}	RSTX,NMIX,MD0,MD1	CMOS hysteresis input level	Vss	-	0.2× V_{CC}	V	
	V_{ILT}	DEBUGIF	TTL input level	Vss	-	0.8	V	

*: It is a standard in BRAMSC (Backup RAM sleep control bit)=1(Enter the state of the sleep at the standby mode) condition.

(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.

(9) Low voltage detection (Internal low-voltage detection)
(T_A: -40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage*2	V_{RDL}		*1	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	-	-		-	-	30	µs	

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.
*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V.
This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(10) External bus I/F (synchronous mode) timing
(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	V_{CC}=5.0V±10%*1
			31.25			V_{CC}=3.3V±0.3V
ASX delay time	t_{CHASL}, t_{CHASH}	SYSCLK ASX	0.5	18	ns	
CS0X to CS3X delay time	t_{CHCSL}, t_{CHCSH}	SYSCLK CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t_{CHAV}, t_{CHAX}	SYSCLK A00 to A21	0.5	18	ns	
RDX delay time	t_{CHRL}, t_{CHRH}	SYSCLK RDX	0.5	18	ns	
RDX minimum pulse	t_{RLRH}	RDX	t_{CYC}× 2 - 20	-	ns	RWT=1, set RWT to 1 or more.*2
Data setup → RDX↑time	t_{DSRH}	RDX D16 to D31	18+t_{CYC}	-	ns	Same as above
RDX↑→ data hold	t_{RHDH}		0	-	ns	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWCPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KYCPMC			OFF	
MB91F526KJCPMC		OFF	ON	
MB91F526KLCPMC			OFF	
MB91F525KWCPMC		ON	ON	
MB91F525KYCPMC			OFF	
MB91F525KJCPMC		OFF	ON	
MB91F525KLCPMC			OFF	
MB91F524KWCPMC		ON	ON	
MB91F524KYCPMC			OFF	
MB91F524KJCPMC		OFF	ON	
MB91F524KLCPMC			OFF	
MB91F523KWCPMC		ON	ON	
MB91F523KYCPMC			OFF	
MB91F523KJCPMC		OFF	ON	
MB91F523KLCPMC			OFF	
MB91F522KWCPMC		ON	ON	
MB91F522KYCPMC			OFF	
MB91F522KJCPMC		OFF	ON	
MB91F522KLCPMC			OFF	
MB91F526KSCPMC	None	ON	ON	
MB91F526KUCPMC			OFF	
MB91F526KHCPMC		OFF	ON	
MB91F526KKCPMC			OFF	
MB91F525KSCPMC		ON	ON	
MB91F525KUCPMC			OFF	
MB91F525KHCPMC		OFF	ON	
MB91F525KKCPMC			OFF	
MB91F524KSCPMC		ON	ON	
MB91F524KUCPMC			OFF	
MB91F524KHCPMC		OFF	ON	
MB91F524KKCPMC			OFF	
MB91F523KSCPMC		ON	ON	
MB91F523KUCPMC			OFF	
MB91F523KHCPMC		OFF	ON	
MB91F523KKCPMC			OFF	
MB91F522KSCPMC		ON	ON	
MB91F522KUCPMC			OFF	
MB91F522KHCPMC		OFF	ON	
MB91F522KKCPMC			OFF	

■ **Scope of Impact**

For the affected parts, when the Power-On Reset and Internal Low Voltage Detection are not generated, the MCU may set invalid package and sub clock option information. Therefore, the MCU may operate with an invalid pin configuration.

■ **Workaround**

For the affected parts, it is necessary to satisfy at least one of the Power-On Reset requirements for any Power-On event as given below:

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate is less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

If the customer system does not satisfy the condition above-mentioned, Cypress will releases new version D, so Cypress recommends the version D for MB91F52x. The new version prevents the limitation when an external reset signal is asserted at pin RSTX anytime the supply voltage (VCC) is turned on.

■ **Fix Status**

Will be fixed in production silicon version D, E

2. Limitation for Watch mode (power off)

■ **Problem Definition**

If the below all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

■ **Trigger Conditions**

(1) Using the watch mode (power off)

(2) Interrupt levels that are used as sources for recovering from the watch mode (power off) are ‘16’ to ‘30’, or using NMIX pin as source for recovering from the watch mode (power off)

(3) The sources for recovering from the watch mode (power off) are generated between PCLK 1 cycle and PMUCLK 3 cycles (*), after CPU state changes to the watch mode (power off)
(*): In case of PCLK = 0.5 MHz and PMUCLK = 32 kHz, it is approx. 2 µs to 100 µs

■ **Scope of Impact**

If the all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

WTCRH, WTCRM, WTCRL

CSELR.SCEN

CMONR.SCRDY

CCRTSELR.CST

CCRTSELR.CSC

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(Error)
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<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">2</td><td rowspan="3">2</td><td>P015</td></tr>
<tr><td>D29</td></tr>
<tr><td>TRG0_0</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">3</td><td rowspan="3">3</td><td>P016</td></tr>
<tr><td>D30</td></tr>
<tr><td>TRG1_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">4</td><td>P170</td></tr>
<tr><td>PPG36_1</td></tr>
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<tr><td>D31</td></tr>
<tr><td>TRG2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">6</td><td>P171</td></tr>
<tr><td>PPG37_1</td></tr>
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<tr><td>TIN0_2</td></tr>
<tr><td>RTO5_1</td></tr>
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