Infineon Technologies - MB91F524FWBPMC-GSE1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f524fwbpmc-gse1

1. Product Lineup

Product lineup comparison 64 pins

	MB91F522B	MB91F523B	MB91F524B	MB91F525B	MB91F526B
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	None				
Free-run Timer	16bit×3ch, 32bit×1ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×21ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×13ch (1unit), 12bit×13ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	8ch[*1]				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	44 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
NMI request function	Yes				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V [*2]				
Package	LQD064				

*1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Table for clock supervisor and external low voltage detection reset initial value ON/OFF

Clock	CSV Initial value	LVD Initial value	Function
single	ON	ON	S
		OFF	U
	OFF	ON	H
		OFF	K
Dual	ON	ON	W
		OFF	Y
	OFF	ON	J
		OFF	L

MB９１F５２X□△○

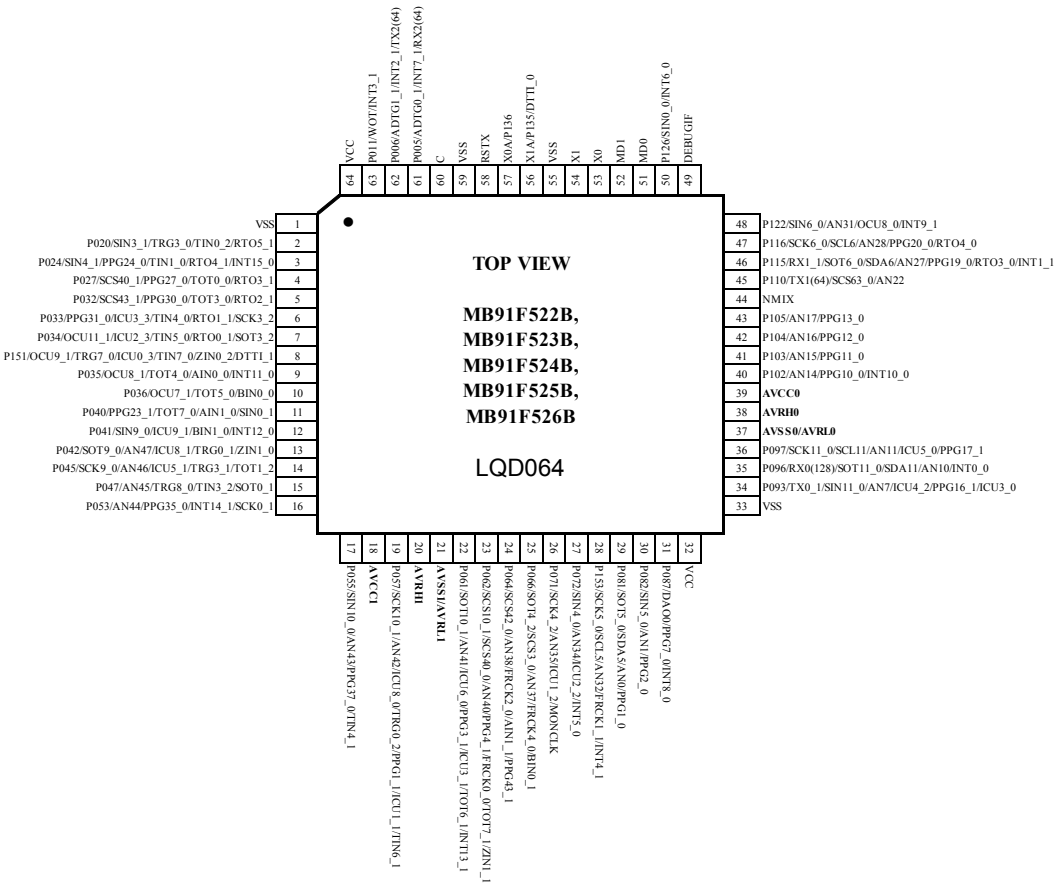
```
          |||└→Ｒｅｖｉｓｉｏｎ：B, C, D, E
          ||└──→Ｆｕｎｃｔｉｏｎ：See the table for clock supervisor and external
          ||                      low voltage detection reset initial value ON/OFF.
          |└────→ＰＫＧ Ｔｙｐｅ：Ｂ ６４ｐｉｎ
          |                      Ｄ ８０ ｐｉｎ
          |                      Ｆ １００ ｐｉｎ
          |                      Ｊ １２０ ｐｉｎ
          |                      Ｋ １４４ ｐｉｎ
          |                      Ｌ １７６ ｐｉｎ
          └────────→Ｍｅｍｏｒｙ Ｓｉｚｅ：２ ２５６ＫＢ
                                 ３ ３８４ＫＢ
                                 ４ ５１２ＫＢ
                                 ５ ７６８ＫＢ
                                 ６ １ＭＢ
```

2. Pin Assignment

MB91F52xB

MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B

(TOP VIEW)



* In a single clock product, pin 56 and pin 57 are the general-purpose ports.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001200_H	TCGS [R/W] B,H,W ------00	—	—	TCGSE [R/W] B,H,W -----000	16-bit Free-run timer synchronous activation
001204_H	CPCLRB0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 0
001208_H	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00120C_H$	CPCLRB1/CPCLR1 [W] H,W 11111111 11111111		TCDT1 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 1
001210_H	TCCS1 [R/W] B,H,W 00000000 01000000 ----0000 --------				
001214_H	CPCLRB2/CPCLR2 [W] H,W 11111111 11111111		TCDT2 [R/W] H,W 00000000 00000000		16-bit Free-run Timer 2
001218_H	TCCS2 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00121C_H$ to 001230_H	—	—	—	—	Reserved
001234_H	FRS0 [R/W] B,H,W -------- --00--00 --00--00 --00--00				16-bit Free-run timer selection
001238_H	—		FRS1 [R/W] B,H,W --00--00 --00--00		
$00123C_H$	FRS2 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001240_H	FRS3 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001244_H	FRS4 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001248_H	—	—	—	—	Reserved
$00124C_H$	OCCPB0/OCCP0 [R/W] H,W 00000000 00000000		OCCPB1/OCCP1 [R/W] H,W 00000000 00000000		16-bit Output compare 0/1
001250_H	OCS01 [R/W] B,H,W -110--00 00001100		—	OCMOD01 [R/W] B,H,W ------00	
001254_H	OCCPB2/OCCP2 [R/W] H,W 00000000 00000000		OCCPB3/OCCP3 [R/W] H,W 00000000 00000000		16-bit Output compare 2/3
001258_H	OCS23 [R/W] B,H,W -110--00 00001100		—	OCMOD23 [R/W] B,H,W ------00	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001804_H	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001808_H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
$00180C_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810_H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814_H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818_H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00181C_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820_H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824_H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828_H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
$00182C_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830_H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834_H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838_H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
$00183C_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001878_H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W -------- *3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W -------- *3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W -------- *3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W -------- *3	Multi-UART7 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00187C_H$	—	— /(SCSFR27) [R/W] B,H,W -------- *3	— /(SCSFR17) [R/W] B,H,W -------- *3	— /(SCSFR07) [R/W] B,H,W -------- *3	
001880_H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W -------- *3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W -------- *3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W -------- *3	TBYTE07/(LAMRID7) / (LAMTID7) [R/W] B,H,W 00000000	
001884_H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -------- *2	— /(ISBA7)[R/W] B,H,W -------- *2	Multi-UART7
001888_H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
$00188C_H$	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890_H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894_H	— /(RDR18/(TDR18))[R/W] B,H,W -------- -------- *3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000 *1		
001898_H	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
$00189C_H$	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- -------- *3 *4		
$0018A0_H$	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -------- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -------- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -------- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -------- *3	
$0018A4_H$	—	— /(SCSFR28) [R/W] B,H,W -------- *3	— /(SCSFR18) [R/W] B,H,W -------- *3	— /(SCSFR08) [R/W] B,H,W -------- *3	
$0018A8_H$	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -------- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -------- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -------- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	
$0018AC_H$	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -------- *2	— /(ISBA8)[R/W] B,H,W -------- *2	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002150_H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		CAN1 (64msb)
002154_H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158_H	—	—	—	—	
$00215C_H$	—	—	—	—	
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H to $00217C_H$	—				
002180_H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184_H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188_H	—	—	—	—	
$00218C_H$	—	—	—	—	
002190_H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194_H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198_H	—	—	—	—	
$00219C_H$	—	—	—	—	
$0021A0_H$	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
$0021A8_H$	—	—	—	—	
$0021AC_H$	—	—	—	—	
$0021B0_H$	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		
$0021B8_H$	—	—	—	—	
$0021BC_H$	—	—	—	—	

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU 6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40

DC Characteristics

(T_A: -40°C to +105°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

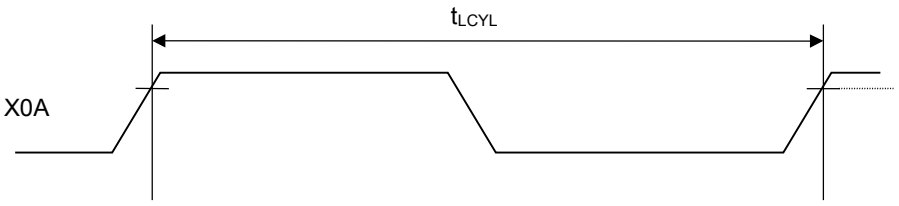
Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	80	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	90	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	90	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	71	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	81	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	81	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	62	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	72	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	72	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	61	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	51	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation, Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

(1-2) Sub clock timing

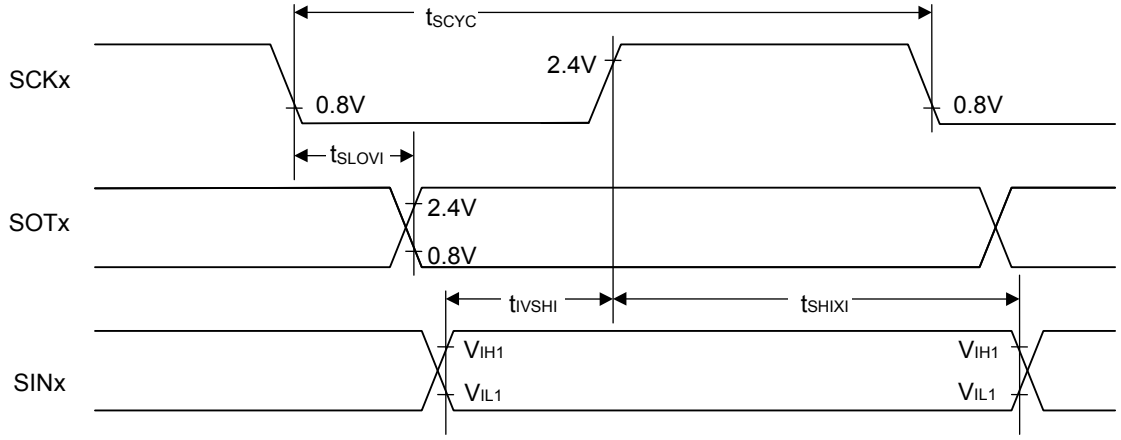
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A		-	30.52	-	µs	

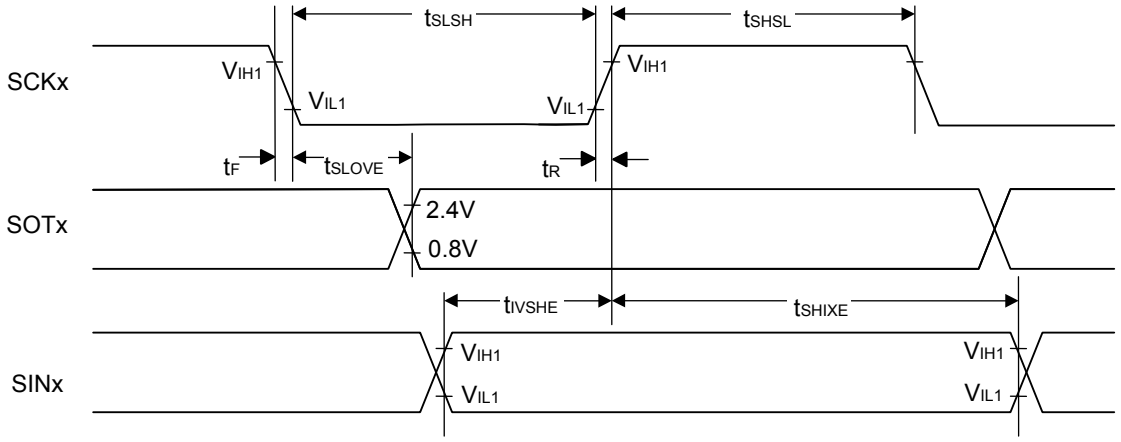
・X0A,X1A clock timing



- Internal shift clock mode

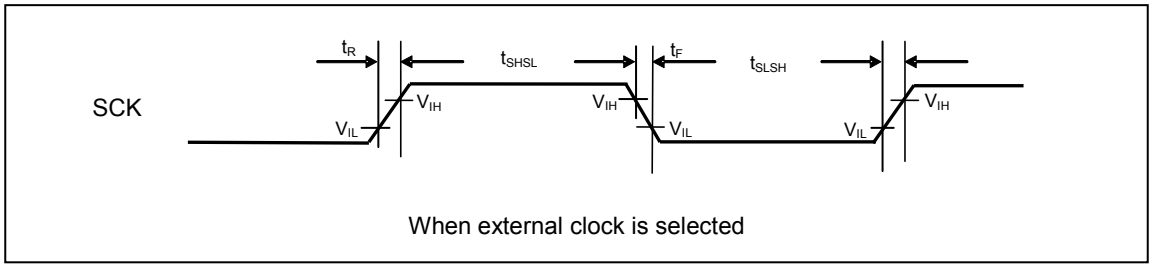


- External shift clock mode



(4-2) UART (Asynchronous serial interface) timing
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=0
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=1
When external clock is selected (BGR:EXT=1)
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



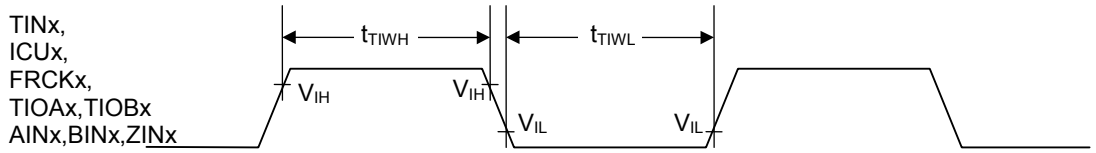
When external clock is selected

(5) Timer input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN7 ICU0 to ICU9 FRCK0 to FRCK5 TIOA0, TIOA1, TIOB0, TIOB1, AIN0, AIN1, BIN0, BIN1, ZIN0, ZIN1	–	$4t_{CPP}$	–	ns	

• Timer input timing

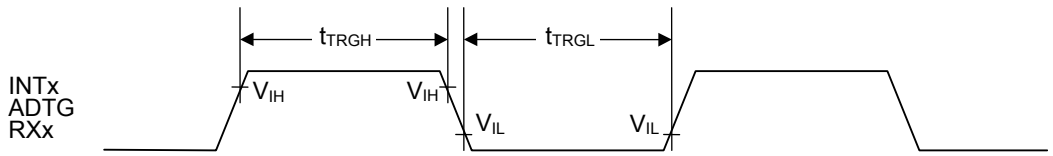


(6) Trigger input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

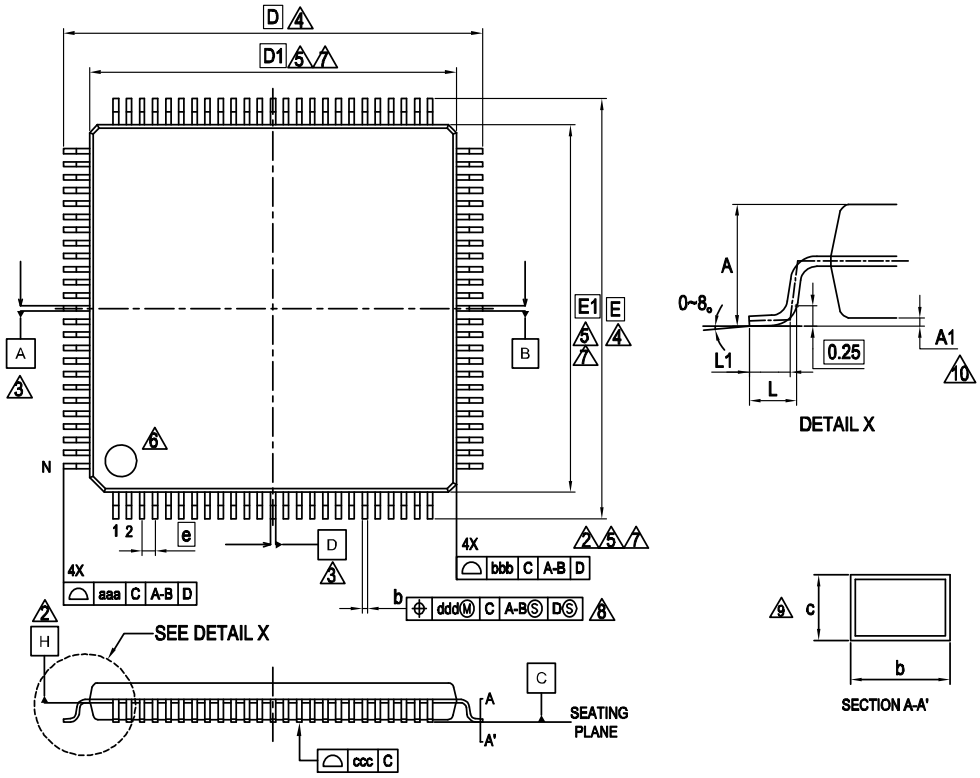
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT15, ADTG, RX0, RX1, RX2	–	$5t_{CPP}$	–	ns	
				1	–	µs	At stop mode

• Trigger input timing



Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWCPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KYCPMC			OFF	
MB91F526KJCPMC		OFF	ON	
MB91F526KLCPMC			OFF	
MB91F525KWCPMC		ON	ON	
MB91F525KYCPMC			OFF	
MB91F525KJCPMC		OFF	ON	
MB91F525KLCPMC			OFF	
MB91F524KWCPMC		ON	ON	
MB91F524KYCPMC			OFF	
MB91F524KJCPMC		OFF	ON	
MB91F524KLCPMC			OFF	
MB91F523KWCPMC		ON	ON	
MB91F523KYCPMC			OFF	
MB91F523KJCPMC		OFF	ON	
MB91F523KLCPMC			OFF	
MB91F522KWCPMC		ON	ON	
MB91F522KYCPMC			OFF	
MB91F522KJCPMC		OFF	ON	
MB91F522KLCPMC			OFF	
MB91F526KSCPMC	None	ON	ON	
MB91F526KUCPMC			OFF	
MB91F526KHCPMC		OFF	ON	
MB91F526KKCPMC			OFF	
MB91F525KSCPMC		ON	ON	
MB91F525KUCPMC			OFF	
MB91F525KHCPMC		OFF	ON	
MB91F525KKCPMC			OFF	
MB91F524KSCPMC		ON	ON	
MB91F524KUCPMC			OFF	
MB91F524KHCPMC		OFF	ON	
MB91F524KKCPMC			OFF	
MB91F523KSCPMC		ON	ON	
MB91F523KUCPMC			OFF	
MB91F523KHCPMC		OFF	ON	
MB91F523KKCPMC			OFF	
MB91F522KSCPMC		ON	ON	
MB91F522KUCPMC			OFF	
MB91F522KHCPMC		OFF	ON	
MB91F522KKCPMC			OFF	

LQI100 , 100 Lead Plastic Low Profile Quad Flat Package



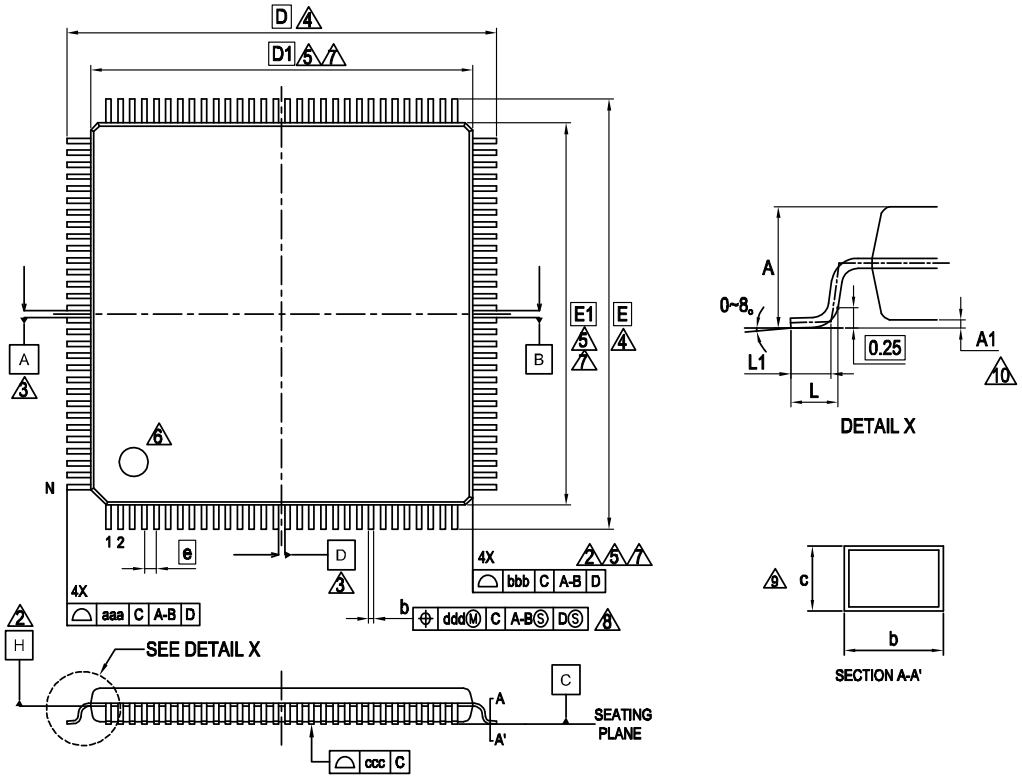
PACKAGE	LQI100		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.15	0.20	0.25
c	0.09	——	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
e	0.50 BSC		
E	16.00 BSC.		
E1	14.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	100		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQM120 , 120 Lead Plastic Low Profile Quad Flat Package

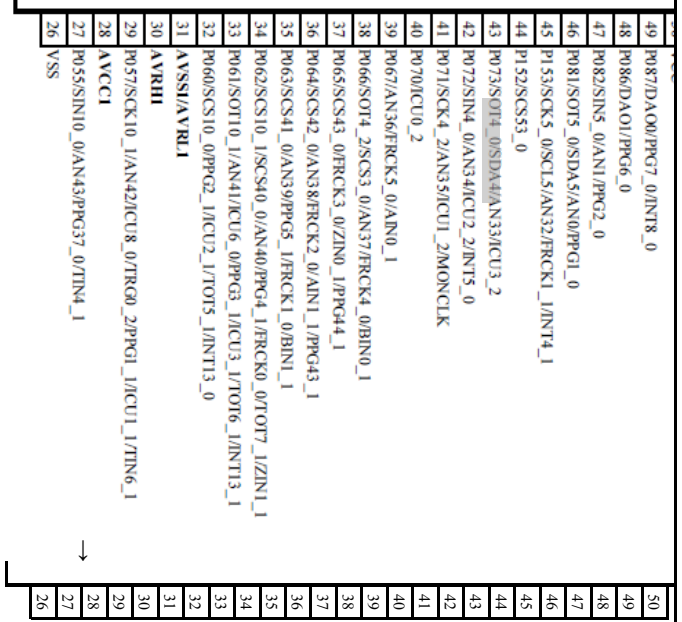


PACKAGE	LQM120		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.17	0.22	0.27
c	0.115	——	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.50 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	120		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Page	Section	Change Results
15	■Pin Assignment MB91F52xF	Signals indicated by the shading below deleted in Figure. (Error) - Bottom 

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>20</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">4</td><td rowspan="5">7</td><td rowspan="5">10</td><td rowspan="5">12</td><td>P025</td></tr>
<tr><td>WR1X</td></tr>
<tr><td>SOT4_1</td></tr>
<tr><td>PPG25_0</td></tr>
<tr><td>TIN2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">13</td><td>P172</td></tr>
<tr><td>PPG38_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">4</td><td rowspan="5">5</td><td rowspan="5">8</td><td rowspan="5">11</td><td rowspan="5">14</td><td>P026</td></tr>
<tr><td>A00</td></tr>
<tr><td>SCK4_1</td></tr>
<tr><td>PPG26_0</td></tr>
<tr><td>TIN3_0</td></tr>
<tr><td rowspan="6">4</td><td rowspan="6">5</td><td rowspan="6">6</td><td rowspan="6">9</td><td rowspan="6">12</td><td rowspan="6">15</td><td>P027</td></tr>
<tr><td>A01</td></tr>
<tr><td>SCS40_1</td></tr>
<tr><td>PPG27_0</td></tr>
<tr><td>TOT0_0</td></tr>
<tr><td>RTO3_1</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">16</td><td>P173</td></tr>
<tr><td>PPG39_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">7</td><td rowspan="5">10</td><td rowspan="5">13</td><td rowspan="5">17</td><td>P030</td></tr>
<tr><td>A02</td></tr>
<tr><td>SCS41_1</td></tr>
<tr><td>PPG28_0</td></tr>
<tr><td>TOT1_0</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">6</td><td rowspan="5">8</td><td rowspan="5">11</td><td rowspan="5">14</td><td rowspan="5">18</td><td>P031</td></tr>
<tr><td>A03</td></tr>
<tr><td>SCS42_1</td></tr>
<tr><td>PPG29_0</td></tr>
<tr><td>TOT2_0</td></tr>
<tr><td rowspan="5">5</td><td rowspan="5">7</td><td rowspan="5">9</td><td rowspan="5">12</td><td rowspan="5">15</td><td rowspan="5">19</td><td>P032</td></tr>
<tr><td>A04</td></tr>
<tr><td>SCS43_1</td></tr>
<tr><td>PPG30_0</td></tr>
<tr><td>TOT3_0</td></tr>
<tr><td>RTO2_1</td></tr>
<tr><td rowspan="7">6</td><td rowspan="7">8</td><td rowspan="7">10</td><td rowspan="7">13</td><td rowspan="7">16</td><td rowspan="7">20</td><td>P033</td></tr>
<tr><td>A05</td></tr>
<tr><td>PPG31_0</td></tr>
<tr><td>ICU3_3</td></tr>
<tr><td>TIN4_0</td></tr>
<tr><td>RTO1_1</td></tr>
<tr><td>SCK3_2</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>21, 22</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="7">7</td><td rowspan="7">9</td><td rowspan="7">11</td><td rowspan="7">14</td><td rowspan="7">17</td><td rowspan="7">21</td><td>P034</td></tr>
<tr><td>A06</td></tr>
<tr><td>OCU11_1</td></tr>
<tr><td>ICU2_3</td></tr>
<tr><td>TIN5_0</td></tr>
<tr><td>RTO0_1</td></tr>
<tr><td>SOT3_2</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="8">8</td><td rowspan="8">10</td><td rowspan="8">13</td><td rowspan="8">16</td><td rowspan="8">19</td><td rowspan="8">23</td><td>P151</td></tr>
<tr><td>SCK8_0/ SCL8</td></tr>
<tr><td>OCU9_1</td></tr>
<tr><td>TRG7_0</td></tr>
<tr><td>ICU0_3</td></tr>
<tr><td>TIN7_0</td></tr>
<tr><td>ZIN0_2</td></tr>
<tr><td>DTTI_1</td></tr>
<tr><td rowspan="7">9</td><td rowspan="7">11</td><td rowspan="7">14</td><td rowspan="7">17</td><td rowspan="7">20</td><td rowspan="7">24</td><td>P035</td></tr>
<tr><td>A07</td></tr>
<tr><td>SIN8_0</td></tr>
<tr><td>OCU8_1</td></tr>
<tr><td>TOT4_0</td></tr>
<tr><td>AIN0_0</td></tr>
<tr><td>INT11_0</td></tr>
<tr><td rowspan="7">10</td><td rowspan="7">12</td><td rowspan="7">15</td><td rowspan="7">18</td><td rowspan="7">21</td><td rowspan="7">25</td><td>P036</td></tr>
<tr><td>A08</td></tr>
<tr><td>SCS8_0</td></tr>
<tr><td>OCU7_1</td></tr>
<tr><td>TOT5_0</td></tr>
<tr><td>BIN0_0</td></tr>
<tr><td rowspan="6">-</td><td rowspan="6">-</td><td rowspan="6">16</td><td rowspan="6">19</td><td rowspan="6">22</td><td rowspan="6">26</td><td>P037</td></tr>
<tr><td>A09</td></tr>
<tr><td>OCU6_1</td></tr>
<tr><td>TOT6_0</td></tr>
<tr><td>ZIN0_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">27</td><td>P174</td></tr>
<tr><td>TRG8_1</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>21, 22</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="7">7 *1</td><td rowspan="7">9 *1</td><td rowspan="7">11 *1</td><td rowspan="7">14 *1</td><td rowspan="7">17</td><td rowspan="7">21</td><td>P034</td></tr>
<tr><td>A06 *2, *3, *4, *5</td></tr>
<tr><td>OCU11_1</td></tr>
<tr><td>ICU2_3</td></tr>
<tr><td>TIN5_0</td></tr>
<tr><td>RTO0_1</td></tr>
<tr><td>SOT3_2</td></tr>
<tr><td colspan="7"></td></tr>
<tr><td rowspan="8">8 *1</td><td rowspan="8">10 *1</td><td rowspan="8">13</td><td rowspan="8">16</td><td rowspan="8">19</td><td rowspan="8">23</td><td>P151</td></tr>
<tr><td>SCK8_0/ SCL8 *2, *3</td></tr>
<tr><td>OCU9_1</td></tr>
<tr><td>TRG7_0</td></tr>
<tr><td>ICU0_3</td></tr>
<tr><td>TIN7_0</td></tr>
<tr><td>ZIN0_2</td></tr>
<tr><td>DTTI_1</td></tr>
<tr><td rowspan="8">9 *1</td><td rowspan="8">11 *1</td><td rowspan="8">14 *1</td><td rowspan="8">17 *1</td><td rowspan="8">20</td><td rowspan="8">24</td><td>P035</td></tr>
<tr><td>A07 *2, *3, *4, *5</td></tr>
<tr><td>SIN8_0 *2, *3</td></tr>
<tr><td>OCU8_1</td></tr>
<tr><td>TOT4_0</td></tr>
<tr><td>AIN0_0</td></tr>
<tr><td>INT11_0</td></tr>
<tr><td rowspan="8">10 *1</td><td rowspan="8">12 *1</td><td rowspan="8">15 *1</td><td rowspan="8">18 *1</td><td rowspan="8">21</td><td rowspan="8">25</td><td>P036</td></tr>
<tr><td>A08 *2, *3, *4, *5</td></tr>
<tr><td>SCS8_0 *2, *3</td></tr>
<tr><td>OCU7_1</td></tr>
<tr><td>TOT5_0</td></tr>
<tr><td>BIN0_0</td></tr>
<tr><td colspan="7"></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">16 *1</td><td rowspan="5">19 *1</td><td rowspan="5">22</td><td rowspan="5">26</td><td>P037</td></tr>
<tr><td>A09 *4, *5</td></tr>
<tr><td>OCU6_1</td></tr>
<tr><td>TOT6_0</td></tr>
<tr><td>ZIN0_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">27</td><td>P174</td></tr>
<tr><td>TRG8_1</td></tr>
</table></td></tr>
</table>