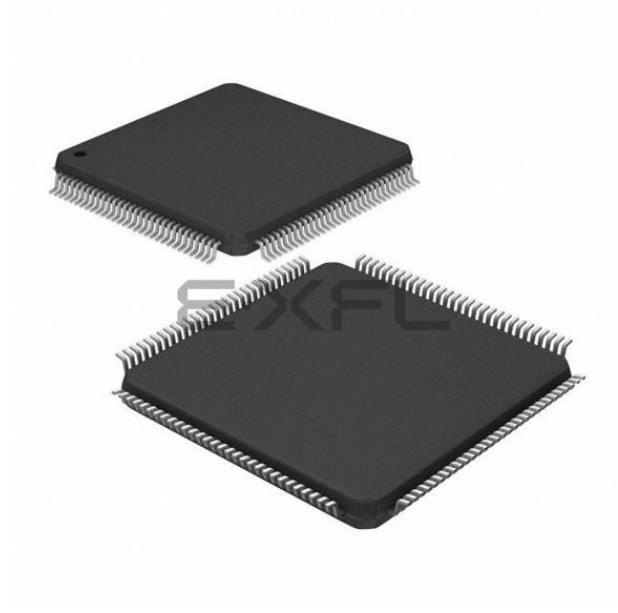


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

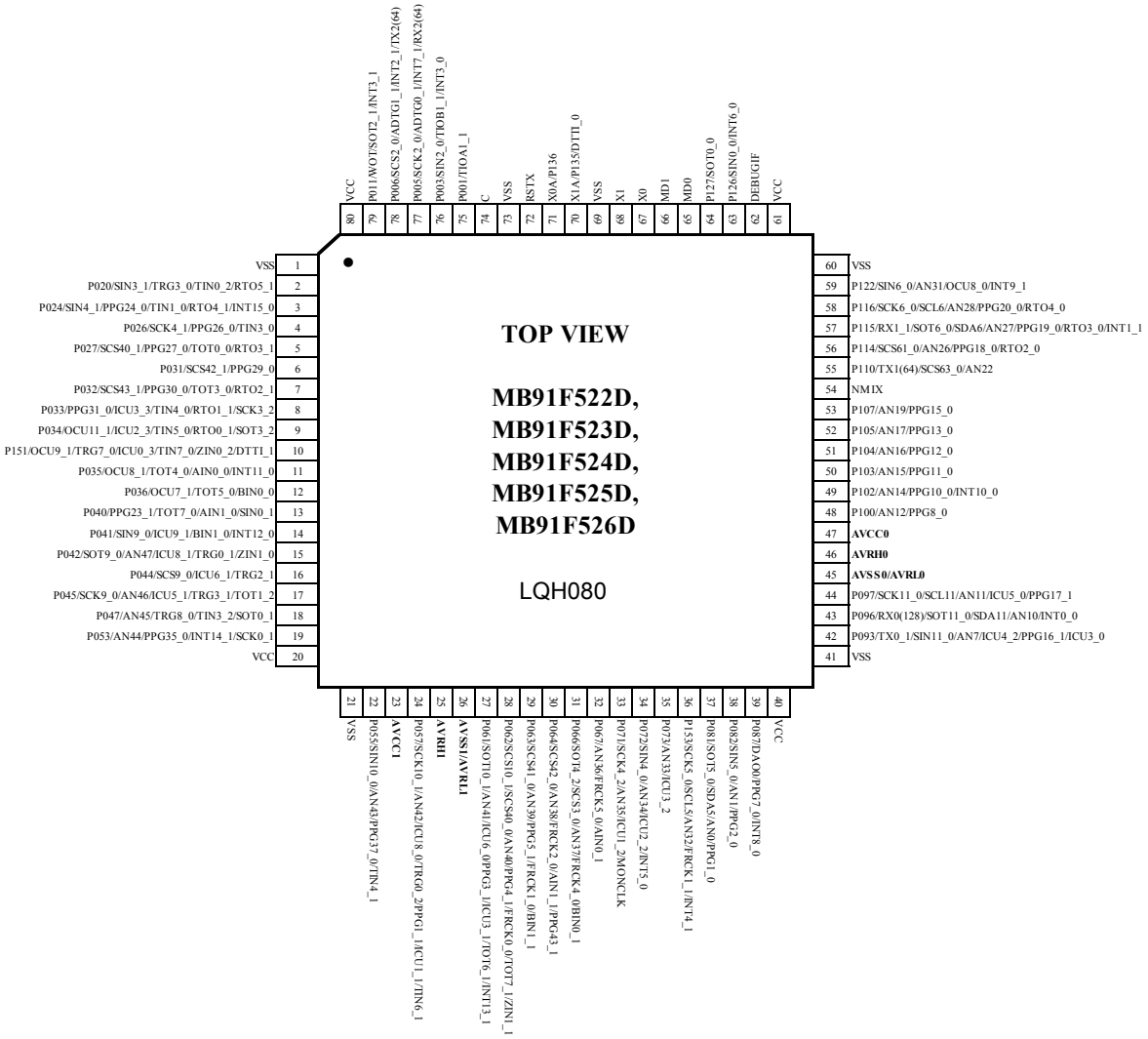
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 42x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f524jhbpmc-gte1

MB91F52xD

MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D

(TOP VIEW)



* In a single clock product, pin 70 and pin 71 are the general-purpose ports.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

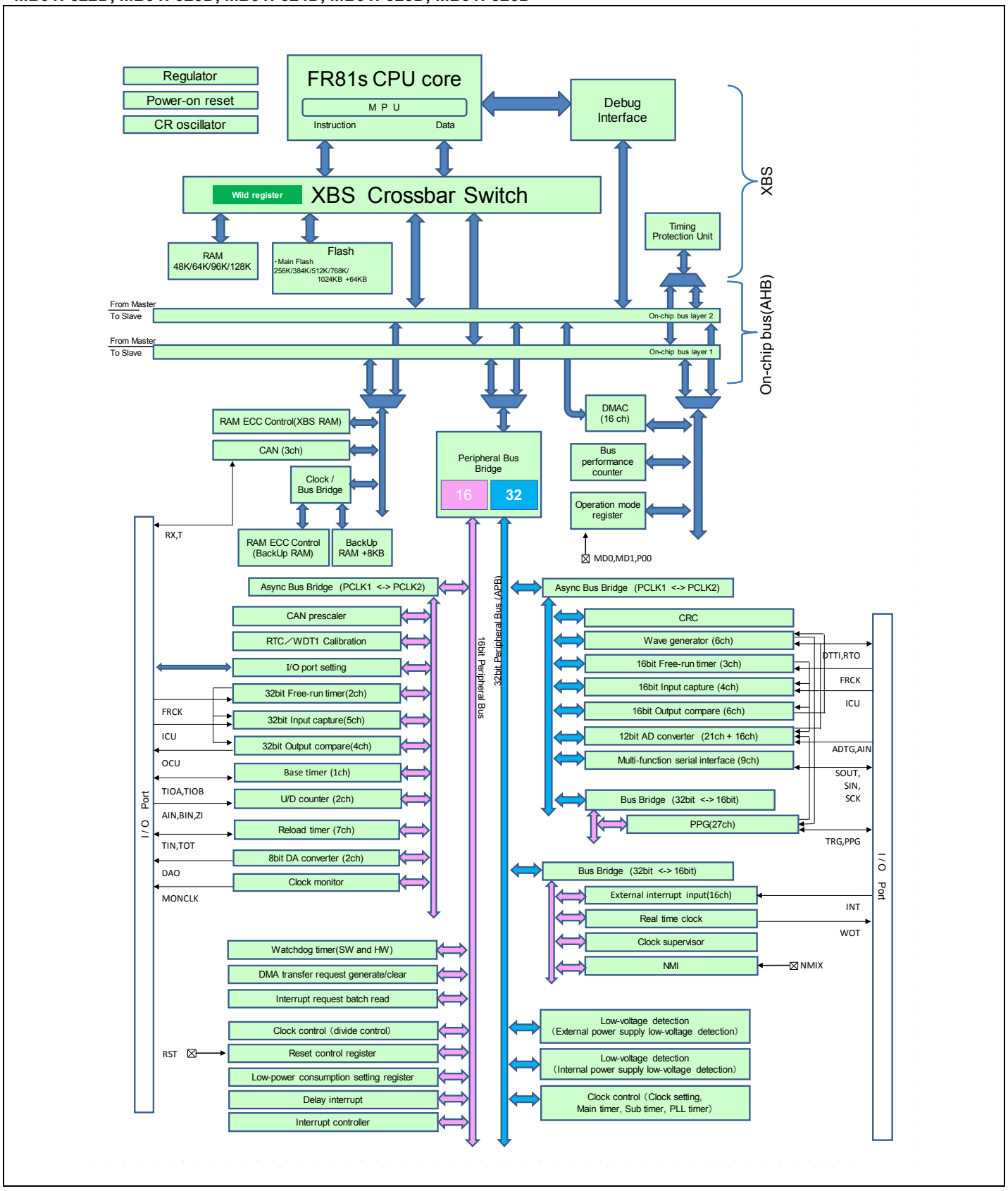
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

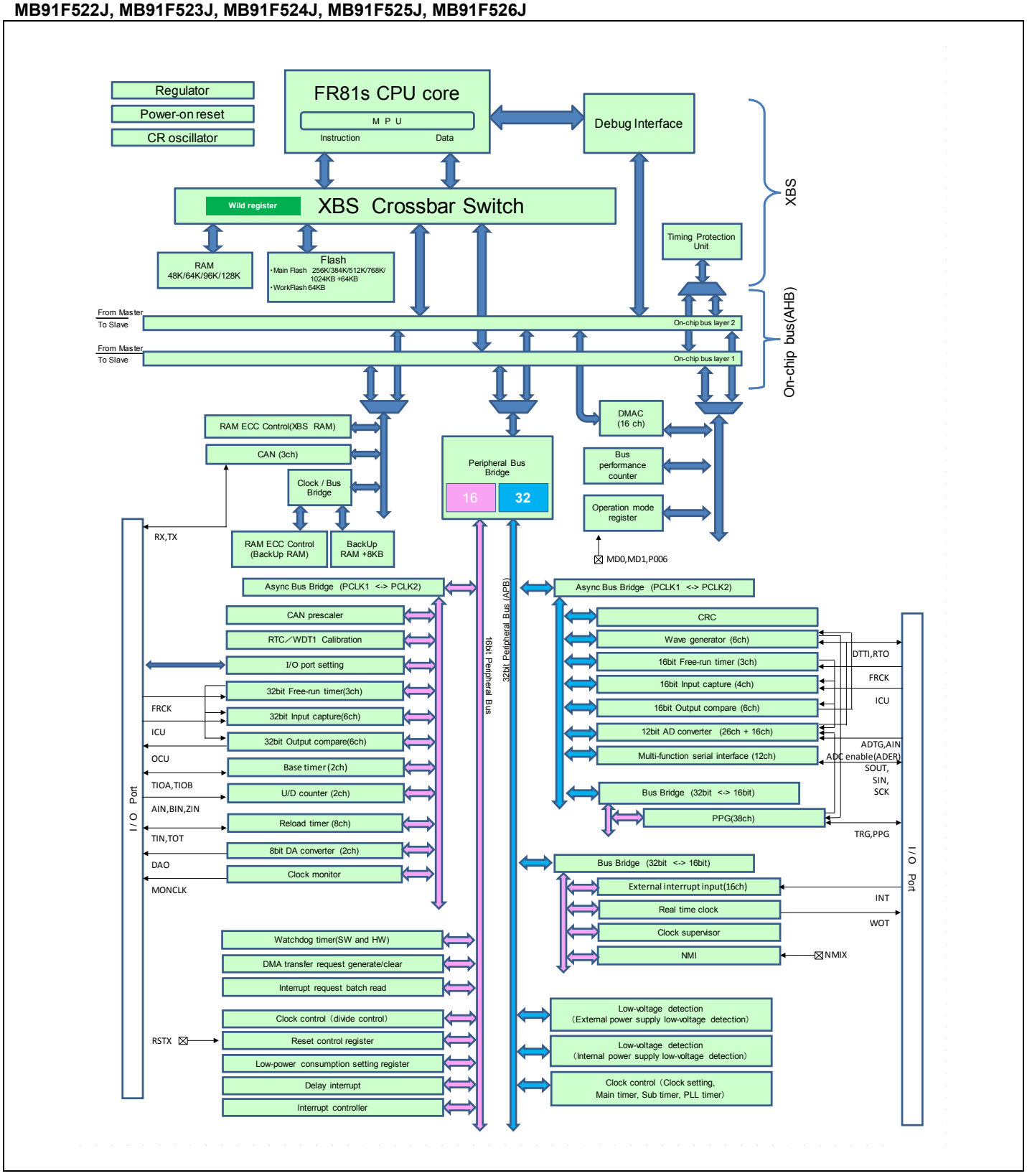
■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D



MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000400_H	ICSEL0 [R/W] B,H,W -----000	ICSEL1 [R/W] B,H,W -----000	ICSEL2 [R/W] B,H,W -------0	ICSEL3 [R/W] B,H,W -------0	DMA request generation and clear
000404_H	—	ICSEL5 [R/W] B,H,W -----000	ICSEL6 [R/W] B,H,W ----0000	ICSEL7 [R/W] B,H,W ----0000	
000408_H	ICSEL8 [R/W] B,H,W ------00	ICSEL9 [R/W] B,H,W ------00	ICSEL10 [R/W] B,H,W ------00	ICSEL11 [R/W] B,H,W -----000	
$00040C_H$	—	ICSEL13 [R/W] B,H,W ------00	ICSEL14 [R/W] B,H,W ------00	ICSEL15 [R/W] B,H,W ------00	
000410_H	ICSEL16 [R/W] B,H,W ----0000	ICSEL17 [R/W] B,H,W ------00	ICSEL18 [R/W] B,H,W ---00000	ICSEL19 [R/W] B,H,W -----000	
000414_H	ICSEL20 [R/W] B,H,W -----000	ICSEL21 [R/W] B,H,W ------00	ICSEL22 [R/W] B,H,W ------00	ICSEL23 [R/W] B,H,W ------00	
000418_H	IRPR0H [R] B,H,W 00------	IRPR0L [R] B,H,W 00------	IRPR1H [R] B,H,W 00------	IRPR1L [R] B,H,W 00------	Interrupt Request Batch Reading Register
$00041C_H$	—	—	IRPR3H [R] B,H,W 000000--	IRPR3L [R] B,H,W 000000--	
000420_H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 000-----	
000424_H	IRPR6H [R] B,H,W --00----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W -0-00---	IRPR7L [R] B,H,W ------00	
000428_H	IRPR8H [R] B,H,W --0-----	IRPR8L [R] B,H,W -00-----	IRPR9H [R] B,H,W -0------	IRPR9L [R] B,H,W -0------	
$00042C_H$	IRPR10H [R] B,H,W -0------	IRPR10L [R] B,H,W -0------	IRPR11H [R] B,H,W 0-------	IRPR11L [R] B,H,W 0-------	
000430_H	IRPR12H [R] B,H,W --0000--	IRPR12L [R] B,H,W ----00--	IRPR13H [R] B,H,W 00------	IRPR13L [R] B,H,W 00------	
000434_H	IRPR14H [R] B,H,W 00000000	IRPR14L [R] B,H,W 00000000	IRPR15H [R] B,H,W 000-----	IRPR15L [R] B,H,W 0000000-	
000438_H	ICSEL24 [R/W] B,H,W ------00	ICSEL25 [R/W] B,H,W ---00000	ICSEL26 [R/W] B,H,W -------0	ICSEL27 [R/W] B,H,W -------0	DMA request generation and clear
$00043C_H$	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444_H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448_H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
$00044C_H$	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450_H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454_H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458_H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
$00045C_H$	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460_H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464_H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468_H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
$00046C_H$	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470_H to $00047C_H$	—	—	—	—	Reserved [S]
000480_H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484_H	—	—	—	—	Reserved [S]
000488_H	DIVR0 [R/W] B,H,W 000-----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
$00048C_H$	—	—	—	—	Reserved [S]
000490_H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494_H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498_H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0008F4$_H$	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild Register [S]
0008F8$_H$	WRAR15 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008FC$_H$	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900$_H$	TPUUNLOCK [R/W] W 00000000 00000000 00000000 00000000				Time Protection Unit [S]
000904$_H$	TPULST [R] B,H,W -------0	—	TPUVST [R/W] B,H,W -----000	—	
000908$_H$	TPUCFG [R/W] B,H,W -------0 0-000000 -------- -------0				
00090C$_H$	TPUTIR [R] B,H,W 00000000	—	—	—	
000910$_H$	TPUTST [R] B,H,W 00000000	—	—	—	
000914$_H$	TPUTIE [R/W] B,H,W 00000000	—	—	—	
000918$_H$	TPUTMID [R] B,H,W 00000000 00000000 00000000 00000000				
00091C$_H$ to 00092C$_H$	—	—	—	—	
000930$_H$	TPUTCN00 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000934$_H$	TPUTCN01 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000938$_H$	TPUTCN02 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
00093C$_H$	TPUTCN03 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000940$_H$	TPUTCN04 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000944$_H$	TPUTCN05 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000948$_H$	TPUTCN06 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
00094C$_H$	TPUTCN07 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000950$_H$	TPUTCN10 [R/W] B,H,W ---00000	—	—	—	

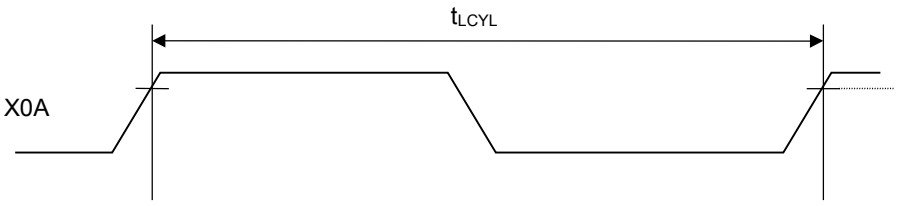
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001840$_H$	SCR6/(IBCR6) [R/W] B,H,W 0--00000	SMR6[R/W] B,H,W 000-00-0	SSR6[R/W] B,H,W 0-000011	ESCR6/(IBSR6)[R/W] B,H,W 00000000	Multi-UART6
001844$_H$	— /(RDR16/(TDR16))[R/W] B,H,W -------- -------- *3		RDR06/(TDR06)[R/W] B,H,W -------0 00000000 *1		Multi-UART6 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001848$_H$	SACSR6[R/W] B,H,W 0----000 00000000		STMR6[R] B,H,W 00000000 00000000		
00184C$_H$	STMCR6[R/W] B,H,W 00000000 00000000		— /(SCSCR6/SFUR6)[R/W] B,H,W -------- -------- *3 *4		
001850$_H$	— /(SCSTR36)/ (LAMSR6) [R/W] B,H,W -------- *3	— /(SCSTR26)/ (LAMCR6) [R/W] B,H,W -------- *3	— /(SCSTR16)/ (SFLR16) [R/W] B,H,W -------- *3	— /(SCSTR06)/ (SFLR06) [R/W] B,H,W -------- *3	
001854$_H$	—	— /(SCSFR26) [R/W] B,H,W -------- *3	— /(SCSFR16) [R/W] B,H,W -------- *3	— /(SCSFR06) [R/W] B,H,W -------- *3	
001858$_H$	—/(TBYTE36)/ (LAMESR6) [R/W] B,H,W -------- *3	—/(TBYTE26)/ (LAMERT6) [R/W] B,H,W -------- *3	—/(TBYTE16)/ (LAMIER6) [R/W] B,H,W -------- *3	TBYTE06/(LAMRID6) / (LAMTID6) [R/W] B,H,W 00000000	
00185C$_H$	BGR6[R/W] H, W 00000000 00000000		— /(ISMK6)[R/W] B,H,W -------- *2	— /(ISBA6)[R/W] B,H,W -------- *2	
001860$_H$	FCR16[R/W] B,H,W ---00100	FCR06[R/W] B,H,W -0000000	FBYTE6[R/W] B,H,W 00000000 00000000		
001864$_H$	FTICR6[R/W] B,H,W 00000000 00000000		—	—	
001868$_H$	SCR7/(IBCR7) [R/W] B,H,W 0--00000	SMR7[R/W] B,H,W 000-00-0	SSR7[R/W] B,H,W 0-000011	ESCR7/(IBSR7)[R/W] B,H,W 00000000	Multi-UART7 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset.
00186C$_H$	— /(RDR17/(TDR17))[R/W] B,H,W -------- -------- *3		RDR07/(TDR07)[R/W] B,H,W -------0 00000000 *1		
001870$_H$	SACSR7[R/W] B,H,W 0----000 00000000		STMR7[R] B,H,W 00000000 00000000		
001874$_H$	STMCR7[R/W] B,H,W 00000000 00000000		— /(SCSCR7/SFUR7)[R/W] B,H,W -------- -------- *3 *4		

(1-2) Sub clock timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

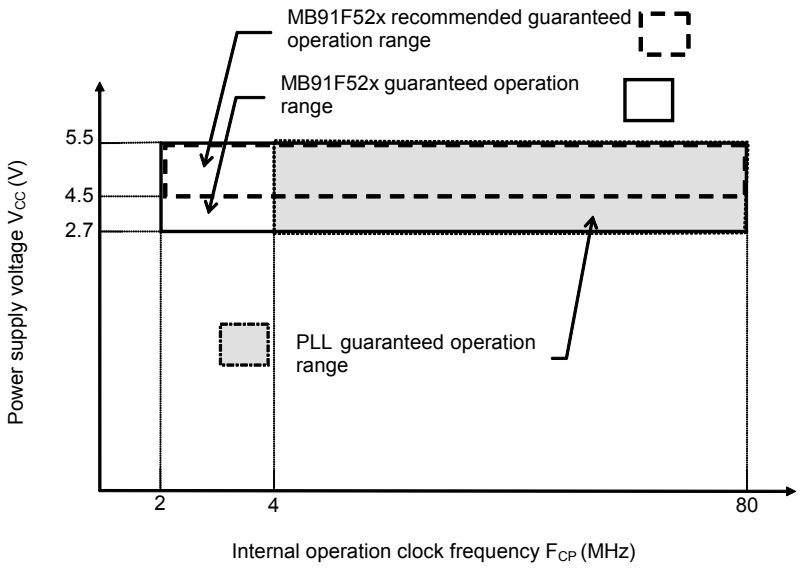
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A		-	30.52	-	µs	

・X0A,X1A clock timing



- Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage



Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

(4-1-2) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=1, SCR:SPI=0

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3, SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

(4-1-3) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=0, SCR:SPI=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
SOT→SCK↓ delay time	t_{SOVLI}	SCK0 to SCK11 SOT0 to SOT11		$2t_{CPP}$ -30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+ 10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$ -10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

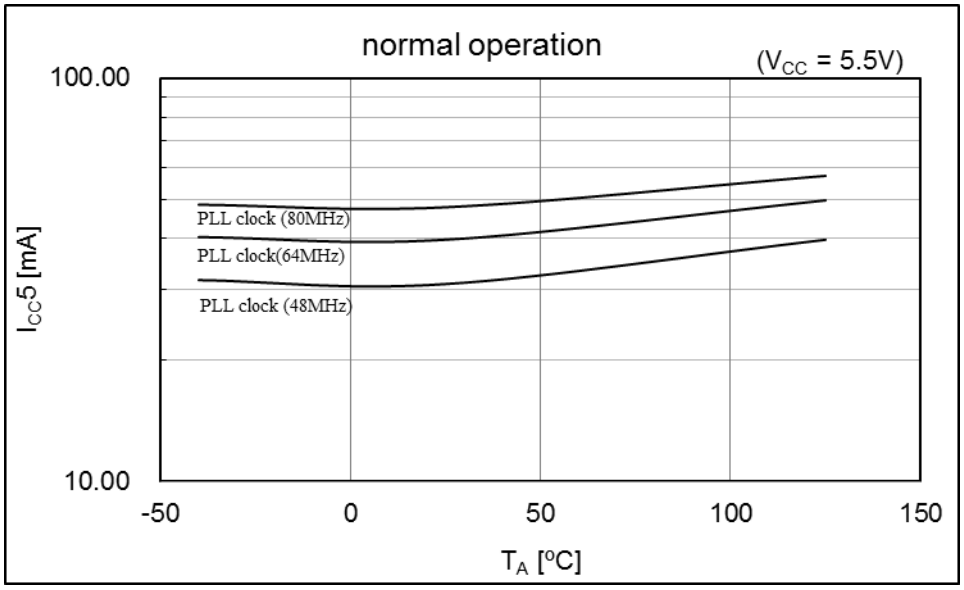
(4-1-8) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used: SCSCR:CSEN=1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

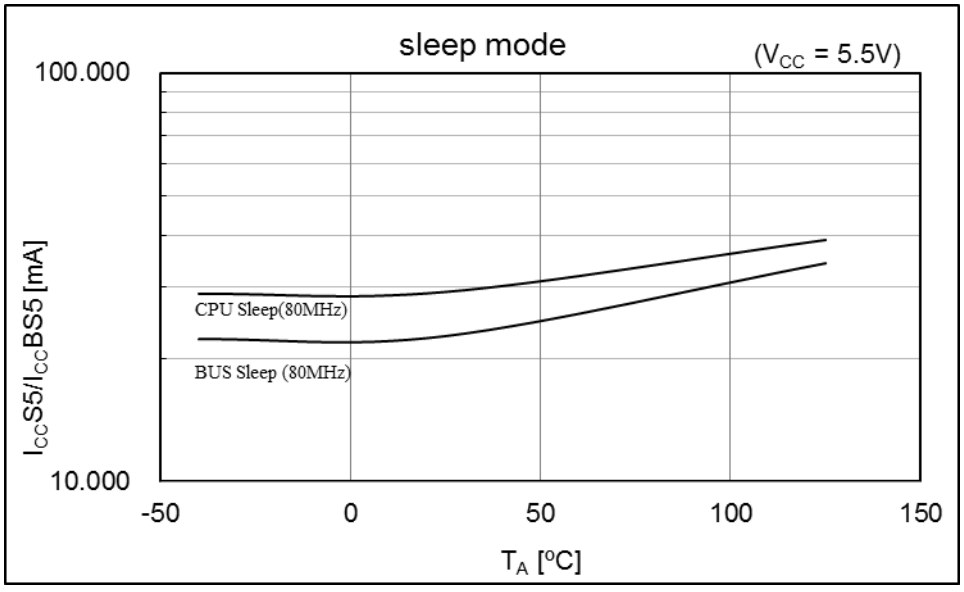
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↓→SCS↓ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	

12. EXAMPLE CHARACTERISTICS

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

MB91F526





Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526DWBPMC	Yes	ON	ON	LQH・80 pin, Plastic
MB91F526DYBPMC			OFF	
MB91F526DJBPMC		OFF	ON	
MB91F526DLBPMC			OFF	
MB91F525DWBPMC		ON	ON	
MB91F525DYBPMC			OFF	
MB91F525DJBPMC		OFF	ON	
MB91F525DLBPMC			OFF	
MB91F524DWBPMC		ON	ON	
MB91F524DYBPMC			OFF	
MB91F524DJBPMC		OFF	ON	
MB91F524DLBPMC			OFF	
MB91F523DWBPMC		ON	ON	
MB91F523DYBPMC			OFF	
MB91F523DJBPMC		OFF	ON	
MB91F523DLBPMC			OFF	
MB91F522DWBPMC		ON	ON	
MB91F522DYBPMC			OFF	
MB91F522DJBPMC		OFF	ON	
MB91F522DLBPMC			OFF	
MB91F526DSBPMC	None	ON	ON	
MB91F526DUBPMC			OFF	
MB91F526DHBPMC		OFF	ON	
MB91F526DKBPMC			OFF	
MB91F525DSBPMC		ON	ON	
MB91F525DUBPMC			OFF	
MB91F525DHBPMC		OFF	ON	
MB91F525DKBPMC			OFF	
MB91F524DSBPMC		ON	ON	
MB91F524DUBPMC			OFF	
MB91F524DHBPMC		OFF	ON	
MB91F524DKBPMC			OFF	
MB91F523DSBPMC		ON	ON	
MB91F523DUBPMC			OFF	
MB91F523DHBPMC		OFF	ON	
MB91F523DKBPMC			OFF	
MB91F522DSBPMC		ON	ON	
MB91F522DUBPMC			OFF	
MB91F522DHBPMC		OFF	ON	
MB91F522DKBPMC			OFF	

18. Errata

This section describes the errata for the MB91520 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
MB91F522B/D/F/J/K/L MB91F523B/D/F/J/K/L MB91F524B/D/F/J/K/L MB91F525B/D/F/J/K/L MB91F526B/D/F/J/K/L

MB91F522/3/4/5/6 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available MB91520 Series devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Power-on Conditions is not enough in the Datasheet Specification	MB91F522B/D/F/J/K/L MB91F523B/D/F/J/K/L MB91F524B/D/F/J/K/L MB91F525B/D/F/J/K/L MB91F526B/D/F/J/K/L	B, C	Will be fixed in production silicon version D, E
[2]. Limitation for Watch mode (power off)		B, C, D, E	-

1. Power-on Conditions is not enough in the Datasheet Specification

■ **Problem Definition**

If the Power-On-Reset and Internal Low Voltage Detection are not generated, some port functions will not be available.

■ **Parameters Affected**

t_{OFF} for Power off time on Power-on Conditions

VCC Power ramp rate on Power-on Conditions

■ **Trigger Condition**

When the power supply voltage to the MCU has been turned off but has not reached 0 V when the power supply voltage is turned on again, MCU does not generate an internal power-on-reset signal (Power-On reset or Internal LVD reset). Then, some port functions will not be available.

If below condition (1) or (2) or (3) is satisfied, Power-On Reset (Initialization-Reset signal) is generated and no problem occurs.

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>20</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">4 *1</td><td rowspan="5">7 *1</td><td rowspan="5">10</td><td rowspan="5">12</td><td>P025</td></tr>
<tr><td>WR1X *4, *5</td></tr>
<tr><td>SOT4_1</td></tr>
<tr><td>PPG25_0</td></tr>
<tr><td>TIN2_0</td></tr>
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<tr><td>PPG38_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">4 *1</td><td rowspan="5">5 *1</td><td rowspan="5">8 *1</td><td rowspan="5">11</td><td rowspan="5">14</td><td>P026</td></tr>
<tr><td>A00 *3, *4, *5</td></tr>
<tr><td>SCK4_1</td></tr>
<tr><td>PPG26_0</td></tr>
<tr><td>TIN3_0</td></tr>
<tr><td rowspan="6">4 *1</td><td rowspan="6">5 *1</td><td rowspan="6">6 *1</td><td rowspan="6">9 *1</td><td rowspan="6">12</td><td rowspan="6">15</td><td>P027</td></tr>
<tr><td>A01 *2, *3, *4, *5</td></tr>
<tr><td>SCS40_1</td></tr>
<tr><td>PPG27_0</td></tr>
<tr><td>TOT0_0</td></tr>
<tr><td>RTO3_1</td></tr>
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<tr><td>PPG39_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">7 *1</td><td rowspan="5">10 *1</td><td rowspan="5">13</td><td rowspan="5">17</td><td>P030</td></tr>
<tr><td>A02 *4, *5</td></tr>
<tr><td>SCS41_1</td></tr>
<tr><td>PPG28_0</td></tr>
<tr><td>TOT1_0</td></tr>
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<tr><td>A03 *3, *4, *5</td></tr>
<tr><td>SCS42_1</td></tr>
<tr><td>PPG29_0</td></tr>
<tr><td>TOT2_0 *3</td></tr>
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<tr><td>A04 *2, *3, *4, *5</td></tr>
<tr><td>SCS43_1</td></tr>
<tr><td>PPG30_0</td></tr>
<tr><td>TOT3_0</td></tr>
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<tr><td>A05 *2, *3, *4, *5</td></tr>
<tr><td>PPG31_0</td></tr>
<tr><td>ICU3_3</td></tr>
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(Error)
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<tr><td>A06</td></tr>
<tr><td>OCU11_1</td></tr>
<tr><td>ICU2_3</td></tr>
<tr><td>TIN5_0</td></tr>
<tr><td>RTO0_1</td></tr>
<tr><td>SOT3_2</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
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<tr><td>SCK8_0/ SCL8</td></tr>
<tr><td>OCU9_1</td></tr>
<tr><td>TRG7_0</td></tr>
<tr><td>ICU0_3</td></tr>
<tr><td>TIN7_0</td></tr>
<tr><td>ZIN0_2</td></tr>
<tr><td>DTTI_1</td></tr>
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<tr><td>SIN8_0</td></tr>
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<tr><td>AIN0_0</td></tr>
<tr><td>INT11_0</td></tr>
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<table><tr><th>Function*2</th></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit21 I/O (0)</td></tr><tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr><tr><td>A/D converter external trigger input 0 (1)</td></tr><tr><td>INT7 External interrupt input (1)</td></tr><tr><td>(CAN reception data 2 input
MB91F52xB ,MB91F52xD only)</td></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit22 I/O (0)</td></tr><tr><td>Serial chip select 2 I/O (0)</td></tr><tr><td>A/D converter external trigger input 1 (1)</td></tr><tr><td>INT2 External interrupt input (1)</td></tr><tr><td>(CAN transmission data 2 output
MB91F52xB ,MB91F52xD only)</td></tr></table>
(Correct)
<table><tr><th>Function*9</th></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit21 I/O (0)</td></tr><tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr><tr><td>A/D converter external trigger input 0 (1)</td></tr><tr><td>INT7 External interrupt input (1)</td></tr><tr><td>CAN reception data 2 input</td></tr><tr><td></td></tr><tr><td>General-purpose I/O port</td></tr><tr><td>External bus data bit22 I/O (0)</td></tr><tr><td>Serial chip select 2 I/O (0)</td></tr><tr><td>A/D converter external trigger input 1 (1)</td></tr><tr><td>INT2 External interrupt input (1)</td></tr><tr><td>CAN transmission data 2 output</td></tr></table></td></tr>
</table>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Package ↓ Package*2 Added the following description. *1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products. Corrected the following description. For details of the package, see "■ PACKAGE DIMENSIONS ". ↓ *2: For details of the package, see "■ PACKAGE DIMENSIONS ". Added the following description. • ORDERING INFORMATION MB91F52xxxC Company name and layout design change
*A	4999456	JHMU	11/13/2015	Updated to Cypress template. Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in “Absolute Maximum Ratings” of “ELECTRICAL CHARACTERISTICS”. *9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106. Added Errata section.
*B	5112138	KUME	01/28/2016	Fixed some clerical errors. For details, please see the chapter 18. Major Changes.
*C	5196285	KUME	04/28/2016	For details, please see the chapter 19. Major Changes.
*D	5318862	KUME	06/23/2016	For details, please see the chapter 19. Major Changes.