# Infineon Technologies - MB91F524KHBPMC-GS-F4K5E1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | FR81S |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, CSIO, I²C, LINbus, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 576KB (576K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 72K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 48x12b; D/A 2x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb91f524khbpmc-gs-f4k5e1 |

- Power-on reset
- Low-voltage detection reset (independently monitor the external power supply and the internal power supply)
  - The external power supply can select initial value ON/OFF by the part number.
- Device Package : 176/144/120/100/80/64
- CMOS 90nm Technology
- Power supplies
  - 5V Power supply
  - The internal 1.2V is generated from 5V with the voltage step-down circuit

**Product lineup comparison 100 pins**

| | MB91F522F | MB91F523F | MB91F524F | MB91F525F | MB91F526F |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5ns (80MHz) | | | | |
| Flash Capacity (Program) | (256+64)KB | (384+64)KB | (512+64)KB | (768+64)KB | (1024+64)KB |
| Flash Capacity (Data) | 64KB | | | | |
| RAM Capacity | (48+8)KB | | (64+8)KB | (96+8)KB | (128+8)KB |
| External BUS I/F (22address/16data/4cs) | None | | | | |
| DMA Transfer | 16ch | | | | |
| 16-bit Base Timer | 1ch | | | | |
| Free-run Timer | 16bit×3ch, 32bit×3ch | | | | |
| Input capture | 16bit×4ch, 32bit×6ch | | | | |
| Output Compare | 16bit×6ch, 32bit×6ch | | | | |
| 16-bit Reload Timer | 8ch | | | | |
| PPG | 16bit×34ch | | | | |
| Up/down Counter | 2ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8ch×2units | | | | |
| A/D converter | 12bit×21ch (1unit), 12bit×16ch (1unit) | | | | |
| D/A converter (8bit) | 2ch | | | | |
| Multi-Function Serial Interface | 12ch[*1] | | | | |
| CAN | 64msg×2ch/128msg×1ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 76 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| NMI request function | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6ch | | | | |
| Operation guaranteed temperature ($T_A$) | -40°C to +125°C | | | | |
| Power supply | 2.7V to 5.5V [*2] | | | | |
| Package | LQI100 | | | | |

*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

- Crystal oscillation circuit
  An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

  The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

- Mode pins (MD1, MD0)
  Connect the MD1and MD0 mode pins to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

- During power-on
  To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

- Notes during PLL clock operation
  When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

- Treatment of A/D converter power supply pins
  Connect the pins to have AVCC=AVRH=VCC and AVSS/AVRL=VSS even if the A/D converter is not used.

- Notes on using external clock
  An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

- Power-on sequence of A/D converter analog inputs
  Be sure to turn on the digital power supply (Vcc) first, and then turn on the A/D converter power supplies (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN47). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc). When the AVRH pin voltage is turned on or off, it must not exceed AVCC. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

- Treatment of C pin
  This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

  **Note:** Please see the latest data sheet for a detailed specification of the operation voltage.

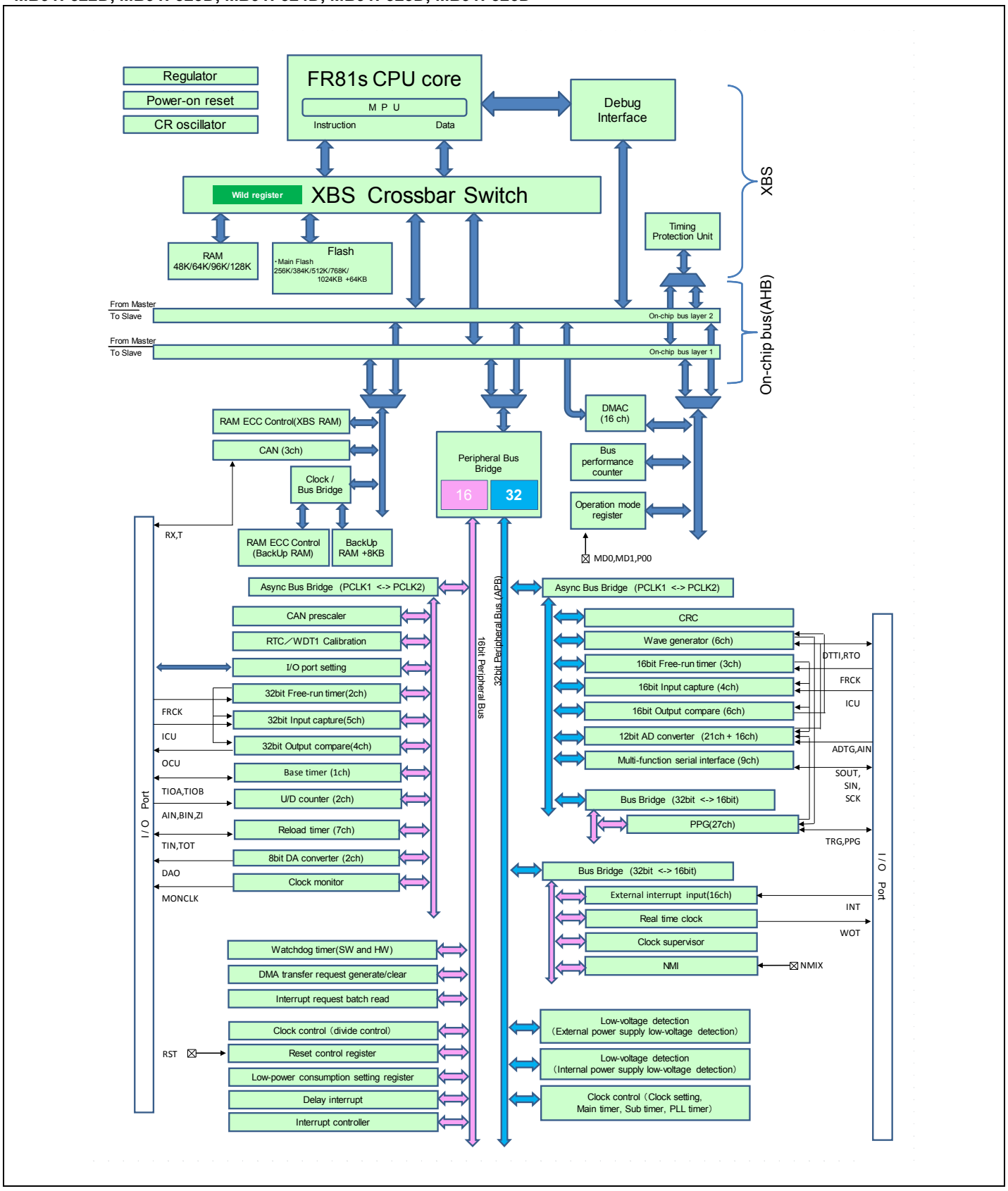
- Function switching of a multiplexed port
  To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see " I/O PORTS" in the hardware manual.

- Low-power consumption mode
  To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL" in the hardware manual.

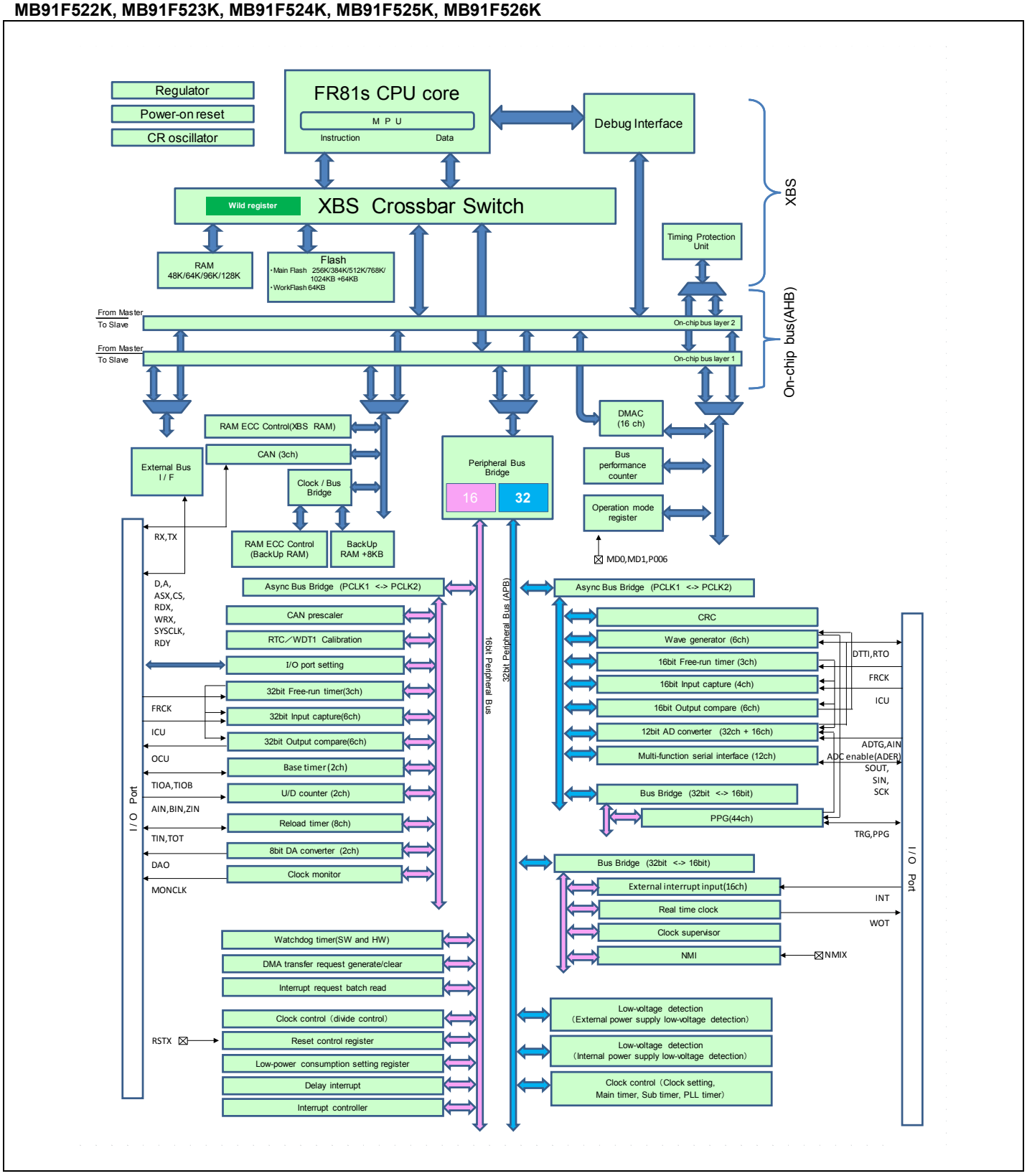
  Take the following notes when using a monitor debugger.

  - Do not set a break point for the low-power consumption transition program.
  - Do not execute an operation step for the low-power consumption transition program.

**MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D**



**MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K**



| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000000_H$ | PDR00 [R/W] B,H,W<br>XXXXXXXX | PDR01 [R/W] B,H,W<br>XXXXXXXX | PDR02 [R/W] B,H,W<br>XXXXXXXX | PDR03 [R/W] B,H,W<br>XXXXXXXX | Port Data Register |
| $000004_H$ | PDR04 [R/W] B,H,W<br>XXXXXXXX | PDR05 [R/W] B,H,W<br>XXXXXXXX | PDR06 [R/W] B,H,W<br>XXXXXXXX | PDR07 [R/W] B,H,W<br>XXXXXXXX | |
| $000008_H$ | PDR08 [R/W] B,H,W<br>XXXXXXXX | PDR09 [R/W] B,H,W<br>XXXXXXXX | PDR10 [R/W] B,H,W<br>XXXXXXXX | PDR11 [R/W] B,H,W<br>XXXXXXXX | |
| $00000C_H$ | PDR12 [R/W] B,H,W<br>XXXXXXXX | PDR13 [R/W] B,H,W<br>-XXXXXXX | PDR14 [R/W] B,H,W<br>---XXX-- | PDR15 [R/W] B,H,W<br>--XXXXXX | |
| $000010_H$ | — | — | — | — | |
| $000014_H$ | — | — | — | — | |
| $000018_H$ | PDR16 [R/W] B,H,W<br>XXXXXXXX | PDR17 [R/W] B,H,W<br>XXXXXXXX | PDR18 [R/W] B,H,W<br>XXXXXXXX | PDR19 [R/W] B,H,W<br>XXXXXXXX | |
| $00001C_H$ to $000034_H$ | — | — | — | — | Reserved |
| $000038_H$ | WDTECR0 [R/W] B,H,W<br>---00000 | — | — | — | Watchdog Timer [S] |
| $00003C_H$ | WDTCR0 [R/W] B,H,W<br>-0--0000 | WDTCPR0 [W] B,H,W<br>00000000 | WDTCR1 [R] B,H,W<br>----0110 | WDTCPR1 [W] B,H,W<br>00000000 | |
| $000040_H$ | — | — | — | — | Reserved |
| $000044_H$ | DICR [R/W] B,H,W<br>-------0 | — | — | — | Delayed Interrupt |
| $000048_H$ to $00005C_H$ | — | — | — | — | Reserved |
| $000060_H$ | TMRLRA0 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR0 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 0 |
| $000064_H$ | TMRLRB0 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR0 [R/W] B,H,W<br>00000000 0-000000 | | |
| $000068_H$ | TMRLRA7 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR7 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 7 |
| $00006C_H$ | TMRLRB7 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR7 [R/W] B,H,W<br>00000000 0-000000 | | |
| $000070_H$ | — | FRS8 [R/W] B,H,W<br>--00--00 --00--00 --00--00 | | | Free-run timer selection register 8 |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000BF8_H$ | — | — | MBR [R/W] B,H,W<br>00------ XXXXXXXX | | OCDU |
| $000BFC_H$ | — | — | UER [W] B,H,W<br>-------- -------X | | |
| $000C00_H$ | DCCR0 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | DMA Controller [S] |
| $000C04_H$ | DCSR0 [R/W] H<br>0------- -----000 | | DTCR0 [R/W] H<br>00000000 00000000 | | |
| $000C08_H$ | DSAR0 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C0C_H$ | DDAR0 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C10_H$ | DCCR1 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C14_H$ | DCSR1 [R/W] H<br>0------- -----000 | | DTCR1 [R/W] H<br>00000000 00000000 | | |
| $000C18_H$ | DSAR1 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C1C_H$ | DDAR1 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C20_H$ | DCCR2 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C24_H$ | DCSR2 [R/W] H<br>0------- -----000 | | DTCR2 [R/W] H<br>00000000 00000000 | | |
| $000C28_H$ | DSAR2 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C2C_H$ | DDAR2 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C30_H$ | DCCR3 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C34_H$ | DCSR3 [R/W] H<br>0------- -----000 | | DTCR3 [R/W] H<br>00000000 00000000 | | |
| $000C38_H$ | DSAR3 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C3C_H$ | DDAR3 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C40_H$ | DCCR4 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C44_H$ | DCSR4 [R/W] H<br>0------- -----000 | | DTCR4 [R/W] H<br>00000000 00000000 | | |
| $000C48_H$ | DSAR4 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0020BC$_H$ | MSGVAL80 [R] B,H,W<br>00000000 00000000 | | MSGVAL70 [R] B,H,W<br>00000000 00000000 | | CAN0<br>(128msb) |
| 0020C0$_H$<br>to<br>0020FC$_H$ | — | | | | |
| 002100$_H$ | CTRLR1 [R/W] B,H,W<br>-------- 000-0001 | | STATR1 [R/W] B,H,W<br>-------- 00000000 | | CAN1<br>(64msb) |
| 002104$_H$ | ERRCNT1 [R] B,H,W<br>00000000 00000000 | | BTR1 [R/W] B,H,W<br>-0100011 00000001 | | |
| 002108$_H$ | INTR1 [R] B,H,W<br>00000000 00000000 | | TESTR1 [R/W] B,H,W<br>-------- X00000-- | | |
| 00210C$_H$ | BRPER1 [R/W] B,H,W<br>-------- ----0000 | | — | — | |
| 002110$_H$ | IF1CREQ1 [R/W] B,H,W<br>0------- 00000001 | | IF1CMSK1 [R/W] B,H,W<br>-------- 00000000 | | |
| 002114$_H$ | IF1MSK21 [R/W] B,H,W<br>11-11111 11111111 | | IF1MSK11 [R/W] B,H,W<br>11111111 11111111 | | |
| 002118$_H$ | IF1ARB21 [R/W] B,H,W<br>00000000 00000000 | | IF1ARB11 [R/W] B,H,W<br>00000000 00000000 | | |
| 00211C$_H$ | IF1MCTR1 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002120$_H$ | IF1DTA11 [R/W] B,H,W<br>00000000 00000000 | | IF1DTA21 [R/W] B,H,W<br>00000000 00000000 | | |
| 002124$_H$ | IF1DTB11 [R/W] B,H,W<br>00000000 00000000 | | IF1DTB21 [R/W] B,H,W<br>00000000 00000000 | | |
| 002128$_H$ | — | — | — | — | |
| 00212C$_H$ | — | — | — | — | |
| 002130$_H$,<br>002134$_H$ | Reserved (IF1 data mirror) | | | | CAN1<br>(64msb) |
| 002138$_H$ | — | — | — | — | |
| 00213C$_H$ | — | — | — | — | |
| 002140$_H$ | IF2CREQ1 [R/W] B,H,W<br>0------- 00000001 | | IF2CMSK1 [R/W] B,H,W<br>-------- 00000000 | | |
| 002144$_H$ | IF2MSK21 [R/W] B,H,W<br>11-11111 11111111 | | IF2MSK11 [R/W] B,H,W<br>11111111 11111111 | | |
| 002148$_H$ | IF2ARB21 [R/W] B,H,W<br>00000000 00000000 | | IF2ARB11 [R/W] B,H,W<br>00000000 00000000 | | |
| 00214C$_H$ | IF2MCTR1 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |

| Interrupt factor | Interrupt number | | Interrupt level | Offset | Default address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexadecimal | | | | |
| Multi-function serial interface ch.8 (reception completed)<br>Multi-function serial interface ch.8 (status)<br>16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | 45 | 2D | ICR29 | $348_H$ | $000FFF48_H$ | 29*1 |
| Main timer<br>Sub timer<br>PLL timer<br>Multi-function serial interface ch.8 (transmission completed)<br>16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | 46 | 2E | ICR30 | $344_H$ | $000FFF44_H$ | 30 |
| Clock calibration unit (sub oscillation)<br>Multi-function serial interface ch.9 (reception completed)<br>Multi-function serial interface ch.9 (status) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1, *4 |
| A/D converter 0/1/7/9/10/11/12/13/14/15/16/ 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit ( CR oscillation)<br>Multi-function serial interface ch.9 (transmission completed)<br>16-bit OCU 0 (match) / 16-bit OCU 1 (match) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| 32-bit Free-run timer 4<br>16-bit OCU 2 (match) / 16-bit OCU 3 (match) | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 32-bit Free-run timer 3/5<br>16-bit OCU 4 (match) / 16-bit OCU 5 (match) | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35*5 |
| 32-bit ICU6 (fetching/measurement)<br>Multi-function serial interface ch.10 (reception completed)<br>Multi-function serial interface ch.10 (status) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| 32-bit ICU7 (fetching/measurement)<br>Multi-function serial interface ch.10 (transmission completed) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| 32-bit ICU8 (fetching/measurement)<br>Multi-function serial interface ch.11 (reception completed)<br>Multi-function serial interface ch.11 (status) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| 32-bit ICU9 (fetching/measurement)<br>WG dead timer underflow 0/1/2<br>WG dead timer reload 0/1/2<br>WG DTTI 0 | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| 32-bit ICU4 (fetching/measurement)<br>Multi-function serial interface ch.11 (transmission completed) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |

| Interrupt factor | Interrupt number | | Interrupt level | Offset | Default address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexadecimal | | | | |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter<br>32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU 6/7/10/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU 8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| -<br>- | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | 44 |
| Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>-<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | 45 |
| DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |
| System reserved<br>(Used for REALOS) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved<br>(Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |
| Used with the INT instruction | 66<br>\|<br>255 | 42<br>\|<br>FF | - | $2F4_H$<br>\|<br>$000_H$ | $000FFEF4_H$<br>\|<br>$000FFC00_H$ | - |

**Note:** It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and $I^2C$ reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

| Interrupt factor | Interrupt number | | Interrupt level | Offset | Default address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexadecimal | | | | |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter<br>32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU 6/7/10/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU 8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| Base timer 0 IRQ0<br>Base timer 0 IRQ1 | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | 44 |
| Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>-<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | 45 |
| DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |
| System reserved<br>(Used for REALOS) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved<br>(Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |
| Used with the INT instruction | 66<br>\|<br>255 | 42<br>\|<br>FF | - | $2F4_H$<br>\|<br>$000_H$ | $000FFEF4_H$<br>\|<br>$000FFC00_H$ | - |

**Note:** It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

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*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↑→SCK↓ setup time | $t_{CSSE}$ | SCK1 to SCK11<br>SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$+30 | - | ns | External shift clock mode output pin: $C_L$=50pF |
| SCK↑→SCS↓ hold time | $t_{CSHE}$ | | | +0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | | $3t_{CPP}$+30 | - | ns | |
| SCS↑→SOT delay time | $t_{DSE}$ | SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 , SOT2,<br>SOT5 to SOT11 | | - | 40 | ns | |
| | | SCS3 ,<br>SCS40 to SCS43<br>SOT3 , SOT4 | | - | 300 | ns | |
| SCS↓→SOT delay time | $t_{DEE}$ | SCS1 to ~SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 to SOT11 | - | +0 | - | ns | External shift clock mode output pin: $C_L$=50pF |
| SCK↓→SCS↑ clock switch time | $t_{SCC}$ | SCK1 , SCK2,<br>SCK5 to SCK11<br>SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$-10 | $3t_{CPP}$+50 | ns | Internal shift clock mode Round operation output pin: $C_L$=50pF |
| | | SCK3 , SCK4<br>SCS3 ,<br>SCS40 to SCS43 | | $3t_{CPP}$-300 | $3t_{CPP}$+50 | ns | |

*1: $t_{CSSU}$ =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: $t_{CSHD}$=SCSTR:CSHD7-0×Serial chip select timing operating clock

*3: $t_{CSDS}$=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3.

**Flash memory**

(1) Electrical Characteristics

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | – | 200 | 800 | ms | 8 Kbytes sector*1, excluding internal preprogramming time |
| | – | 300 | 1100 | ms | 8 Kbytes sector*1, including internal preprogramming time |
| | – | 400 | 2000 | ms | 64 Kbytes sector*1, excluding internal preprogramming time |
| | – | 700 | 3700 | ms | 64 Kbytes sector*1, including internal preprogramming time |
| 8-bit writing time | – | 9 | 288 | µs | Exclusive of overhead time at system level*1 |
| 16-bit writing time | – | 12 | 384 | µs | Exclusive of overhead time at system level*1 |
| ECC writing time | – | 9 | 288 | µs | Exclusive of overhead time at system level*1 |
| Erase cycle*2/ Data retain time | 1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years | – | – | – | Average $T_A$=+85°C*3 |

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.

In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage ($V_{DL}$*), hold Vcc at 2.7V or more within the duration calculated by the following expression:

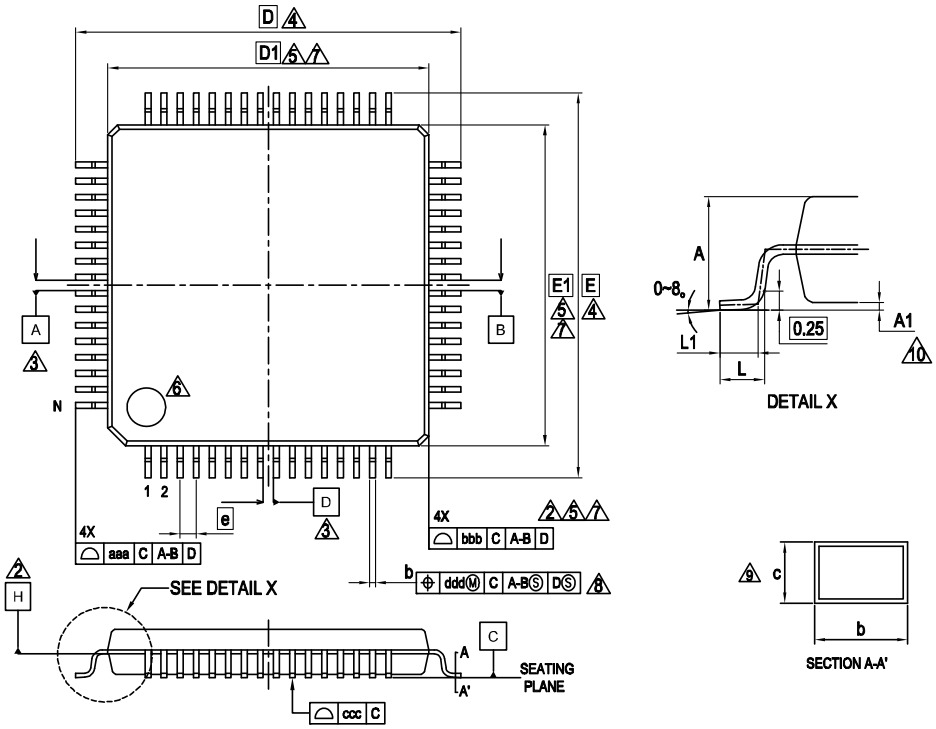
$$Td^{*}[\mu s] + (\text{period of PCLK } [\mu s] \times 257) + 50\ [\mu s]$$

*: See “4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) ”

| Part number | Sub clock | CSV Initial value | LVD Initial value | Package* |
|---|---|---|---|---|
| MB91F526KWEPMC1 | Yes | ON | ON | LQN・144 pin, (LeaE pitch 0.4mm) Plastic |
| MB91F526KJEPMC1 | | OFF | ON | |
| MB91F525KWEPMC1 | | ON | ON | |
| MB91F525KJEPMC1 | | OFF | ON | |
| MB91F524KWEPMC1 | | ON | ON | |
| MB91F524KJEPMC1 | | OFF | ON | |
| MB91F523KWEPMC1 | | ON | ON | |
| MB91F523KJEPMC1 | | OFF | ON | |
| MB91F522KWEPMC1 | | ON | ON | |
| MB91F522KJEPMC1 | | OFF | ON | |
| MB91F526KSEPMC1 | None | ON | ON | |
| MB91F526KHEPMC1 | | OFF | ON | |
| MB91F525KSEPMC1 | | ON | ON | |
| MB91F525KHEPMC1 | | OFF | ON | |
| MB91F524KSEPMC1 | | ON | ON | |
| MB91F524KHEPMC1 | | OFF | ON | |
| MB91F523KSEPMC1 | | ON | ON | |
| MB91F523KHEPMC1 | | OFF | ON | |
| MB91F522KSEPMC1 | | ON | ON | |
| MB91F522KHEPMC1 | | OFF | ON | |
| MB91F526JWEPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| MB91F526JJEPMC | | OFF | ON | |
| MB91F525JWEPMC | | ON | ON | |
| MB91F525JJEPMC | | OFF | ON | |
| MB91F524JWEPMC | | ON | ON | |
| MB91F524JJEPMC | | OFF | ON | |
| MB91F523JWEPMC | | ON | ON | |
| MB91F523JJEPMC | | OFF | ON | |
| MB91F522JWEPMC | | ON | ON | |
| MB91F522JJEPMC | | OFF | ON | |
| MB91F526JSEPMC | None | ON | ON | |
| MB91F526JHEPMC | | OFF | ON | |
| MB91F525JSEPMC | | ON | ON | |
| MB91F525JHEPMC | | OFF | ON | |
| MB91F524JSEPMC | | ON | ON | |
| MB91F524JHEPMC | | OFF | ON | |
| MB91F523JSEPMC | | ON | ON | |
| MB91F523JHEPMC | | OFF | ON | |
| MB91F522JSEPMC | | ON | ON | |
| MB91F522JHEPMC | | OFF | ON | |

## 17. Package Dimensions

### LQD064 , 64 Lead Plastic Low Profile Quad Flat Package



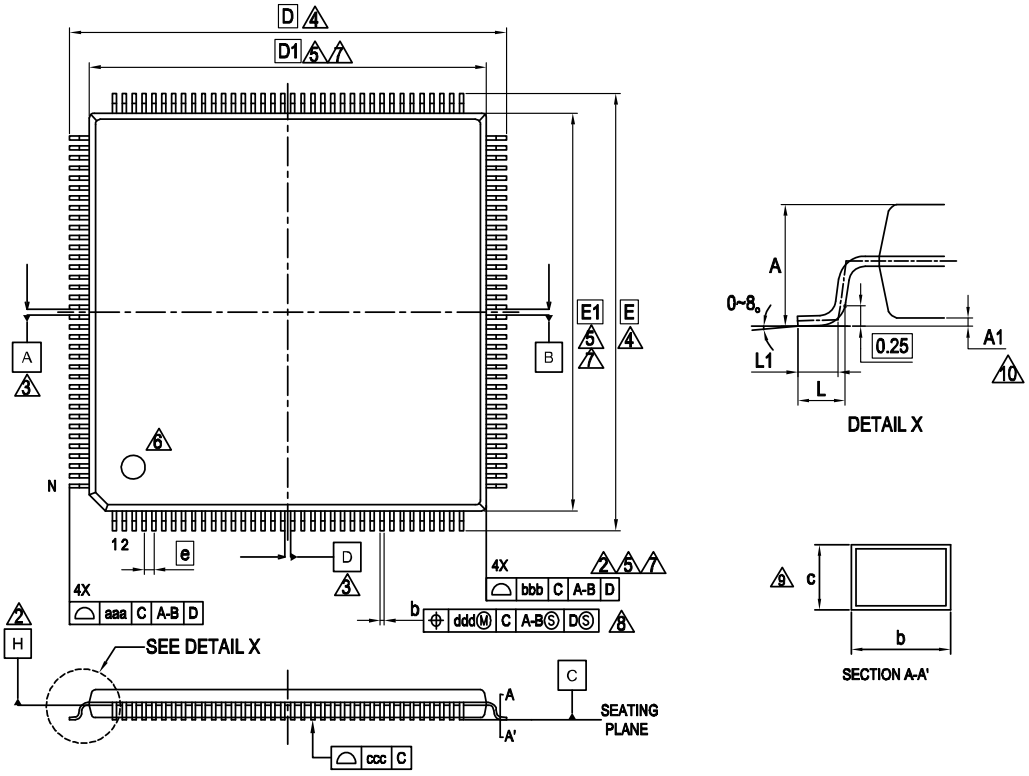

| PACKAGE | LQD64 | | |
|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.09 | — | 0.20 |
| D | 12.00 BSC. | | |
| D1 | 10.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 12.00 BSC. | | |
| E1 | 10.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| aaa | — | — | 0.20 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.08 |
| N | 64 | | |

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS ( mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION ( S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

## LQS144 , 144 Lead Plastic Low Profile Quad Flat Package




| PACKAGE | LQS144 | | |
|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.06 | — | 0.26 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 22.00 BSC. | | |
| D1 | 20.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 22.00 BSC. | | |
| E1 | 20.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| aaa | — | — | 0.20 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.08 |
| N | 144 | | |

**NOTES**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

■ **Workaround**

It is necessary to satisfy the below both conditions of (1) and (2).

(1) Interrupt levels that are used as sources for recovering from the watch mode (power off) are ‘31’, before CPU state changes to the watch mode (power off)

(2) Don’t use NMIX pin as source for recovering from the watch mode (power off)

■ **Fix Status**

Will not be planned

| Page | Section | Change Results |
|---|---|---|
| 141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the following description.<br>Pull-up resistance $R_{UP2}$<br>Port pin other than P035,041,093,122 → P073,074,076,077 |
| 141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the value of " Pull-up resistance $R_{UP2}$".<br>VCC=5.0V±10% Min 25 Max 100 →Min 25 Max 60<br>VCC=3.3V±0.3V Min 49 Max 140 →Min 33 Max 90 |
| 141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Added the value of " Pull-up resistance $R_{UP3}$".<br>Pin name : Port pin other than<br>P035,041,073,074,076,077,093,122<br>VCC=5.0V±10% Min 25 Max 100<br>VCC=3.3V±0.3V Min 45 Max 140 |
| 150,152,<br>154,156 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4) | (4-1-1),(4-1-4)SCK↓⇒SOT delay time $t_{SLOVI}$<br>(4-1-2),(4-1-3)SCK↑⇒SOT delay time $t_{SHOVI}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11<br>SOT0 to SOT11<br>Value: Min -30 Max 30<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>SOT0 to SOT2,SOT5 to SOT11<br>Value: Min -30 Max 30<br>Pin name: SCK3,SCK4<br>SOT3,SOT4<br>Value: Min -300 Max 300 |
| 150,152,<br>154,156 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4) | (4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time $t_{IVSHI}$<br>(4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time $t_{IVSLI}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11 SIN0 to SIN11<br>Value: Min 34 Max -<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to<br>SIN2,SIN5 to SIN11<br>Value: Min 34 Max -<br>Pin name: SCK3,SCK4,SIN3,SIN4<br>Value: Min 300 Max - |
| 150,152,<br>154,156 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4) | (4-1-1),(4-1-4)SCK↓⇒SOT delay time $t_{SLOVE}$<br>(4-1-2),(4-1-3)SCK↑⇒SOT delay time $t_{SHOVE}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11<br>SOT0 to SOT11<br>Value: Min - Max 33<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>SOT0 to SOT2,SOT5 to SOT11<br>Value: Min - Max 33<br>Pin name: SCK3,SCK4 SOT3,SOT4<br>Value: Min - Max 300 |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>29</td><td>■PIN Description</td><td>A List of "Pin Description" modified.<br><br>(Error)<br>
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="8">34</td><td rowspan="8">42</td><td rowspan="8">52</td><td rowspan="8">62</td><td rowspan="8">77</td><td rowspan="8">96</td><td>P093</td></tr>
<tr><td>TX0_1</td></tr>
<tr><td>SIN11_0</td></tr>
<tr><td>AN7</td></tr>
<tr><td>ICU4_2</td></tr>
<tr><td>PPG16_1</td></tr>
<tr><td>ICU3_0</td></tr>
<tr><td>TOT2_1</td></tr>
</table>
<br>(Correct)<br>
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<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
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<tr><td>TOT2_1*2, *3</td></tr>
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<tr><td>30</td><td>■PIN Description</td><td>
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(Error)
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<tr><td rowspan="4">-</td><td rowspan="4">48</td><td rowspan="4">59</td><td rowspan="4">69</td><td rowspan="4">85</td><td rowspan="4">104</td><td>P100</td></tr>
<tr><td>SCK7_0/ SCL7</td></tr>
<tr><td>AN12</td></tr>
<tr><td>PPG8_0</td></tr>
<tr><td colspan="6"></td><td></td></tr>
<tr><td rowspan="5">40</td><td rowspan="5">49</td><td rowspan="5">61</td><td rowspan="5">71</td><td rowspan="5">87</td><td rowspan="5">106</td><td>P102</td></tr>
<tr><td>SIN7_0</td></tr>
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