# Infineon Technologies - MB91F524KHBPMC-GTK5E1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

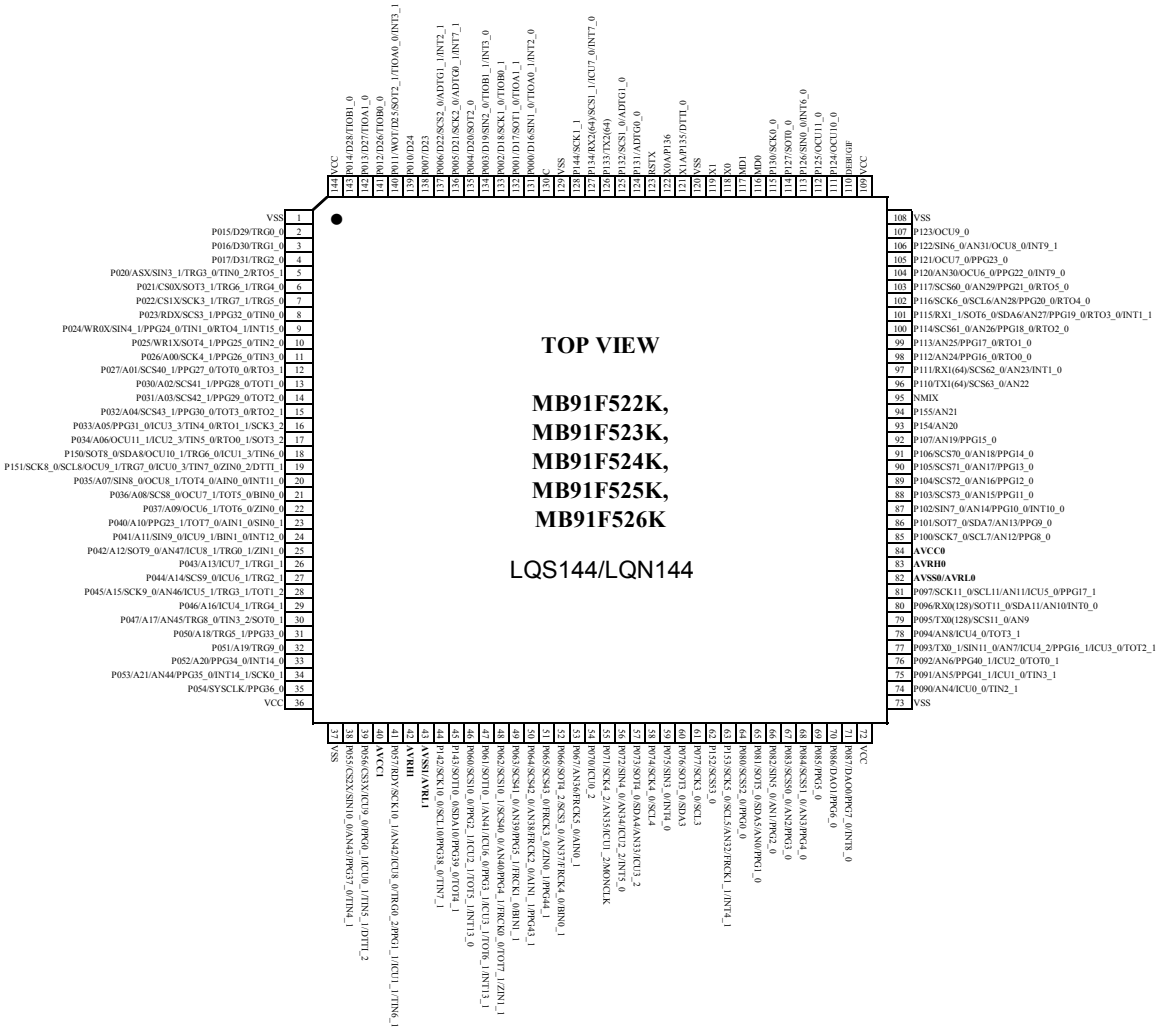
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | FR81S |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, CSIO, I²C, LINbus, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 576KB (576K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 72K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 48x12b; D/A 2x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb91f524khbpmc-gtk5e1 |

**MB91F52xK**

MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K

(TOP VIEW)




* In a single clock product, pin 121 and pin 122 are the general-purpose ports.

## 3. Pin Description

| Pin no. | | | | | | Pin Name | Polarity | I/O circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | - | - | 2 | 2 | P015 | - | A | General-purpose I/O port |
| | | | | | | D29 | - | | External bus data bit29 I/O (0) |
| | | | | | | TRG0_0 | - | | PPG trigger 0 input (0) |
| - | - | - | - | 3 | 3 | P016 | - | A | General-purpose I/O port |
| | | | | | | D30 | - | | External bus data bit30 I/O (0) |
| | | | | | | TRG1_0 | - | | PPG trigger 1 input (0) |
| - | - | - | - | - | 4 | P170 | - | A | General-purpose I/O port |
| | | | | | | PPG36_1 | - | | PPG ch.36 output (1) |
| - | - | - | - | 4 | 5 | P017 | - | A | General-purpose I/O port |
| | | | | | | D31 | - | | External bus data bit31 I/O (0) |
| | | | | | | TRG2_0 | - | | PPG trigger 2 input (0) |
| - | - | - | - | - | 6 | P171 | - | A | General-purpose I/O port |
| | | | | | | PPG37_1 | - | | PPG ch.37 output (1) |
| 2 *1 | 2 *1 | 2 *1 | 2 *1 | 5 | 7 | P020 | - | F | General-purpose I/O port |
| | | | | | | ASX *2, *3, *4, *5 | - | | External bus/Address strobe output |
| | | | | | | SIN3_1 | - | | Multi-function serial ch.3 serial data input (1) |
| | | | | | | TRG3_0 | - | | PPG trigger 3 input (0) |
| | | | | | | TIN0_2 | - | | Reload timer ch.0 event input (2) |
| | | | | | | RTO5_1 | - | | Waveform generator ch.5 output pin (1) |
| - | - | - | 3 *1 | 6 | 8 | P021 | - | A | General-purpose I/O port |
| | | | | | | CS0X *5 | - | | External bus chip select 0 output |
| | | | | | | SOT3_1 | - | | Multi-function serial ch.3 serial data output (1) |
| | | | | | | TRG6_1 | - | | PPG trigger 6 input (1) |
| | | | | | | TRG4_0 | - | | PPG trigger 4 input (0) |
| - | - | - | 4 *1 | 7 | 9 | P022 | - | F | General-purpose I/O port |
| | | | | | | CS1X *5 | - | | External bus chip select 1 output |
| | | | | | | SCK3_1 | - | | Multi-function serial ch.3 clock I/O (1) |
| | | | | | | TRG7_1 | - | | PPG trigger 7 input (1) |
| | | | | | | TRG5_0 | - | | PPG trigger 5 input (0) |
| - | - | - | 5 *1 | 8 | 10 | P023 | - | A | General-purpose I/O port |
| | | | | | | RDX *5 | - | | External bus/Read strobe output |
| | | | | | | SCS3_1 | - | | Serial chip select 3 output (1) |
| | | | | | | PPG32_0 | - | | PPG ch.32 output (0) |
| | | | | | | TIN0_0 | - | | Reload timer ch.0 event input (0) |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000000_H$ | PDR00 [R/W] B,H,W<br>XXXXXXXX | PDR01 [R/W] B,H,W<br>XXXXXXXX | PDR02 [R/W] B,H,W<br>XXXXXXXX | PDR03 [R/W] B,H,W<br>XXXXXXXX | Port Data Register |
| $000004_H$ | PDR04 [R/W] B,H,W<br>XXXXXXXX | PDR05 [R/W] B,H,W<br>XXXXXXXX | PDR06 [R/W] B,H,W<br>XXXXXXXX | PDR07 [R/W] B,H,W<br>XXXXXXXX | |
| $000008_H$ | PDR08 [R/W] B,H,W<br>XXXXXXXX | PDR09 [R/W] B,H,W<br>XXXXXXXX | PDR10 [R/W] B,H,W<br>XXXXXXXX | PDR11 [R/W] B,H,W<br>XXXXXXXX | |
| $00000C_H$ | PDR12 [R/W] B,H,W<br>XXXXXXXX | PDR13 [R/W] B,H,W<br>-XXXXXXX | PDR14 [R/W] B,H,W<br>---XXX-- | PDR15 [R/W] B,H,W<br>--XXXXXX | |
| $000010_H$ | — | — | — | — | |
| $000014_H$ | — | — | — | — | |
| $000018_H$ | PDR16 [R/W] B,H,W<br>XXXXXXXX | PDR17 [R/W] B,H,W<br>XXXXXXXX | PDR18 [R/W] B,H,W<br>XXXXXXXX | PDR19 [R/W] B,H,W<br>XXXXXXXX | |
| $00001C_H$ to $000034_H$ | — | — | — | — | Reserved |
| $000038_H$ | WDTECR0 [R/W] B,H,W<br>---00000 | — | — | — | Watchdog Timer [S] |
| $00003C_H$ | WDTCR0 [R/W] B,H,W<br>-0--0000 | WDTCPR0 [W] B,H,W<br>00000000 | WDTCR1 [R] B,H,W<br>----0110 | WDTCPR1 [W] B,H,W<br>00000000 | |
| $000040_H$ | — | — | — | — | Reserved |
| $000044_H$ | DICR [R/W] B,H,W<br>-------0 | — | — | — | Delayed Interrupt |
| $000048_H$ to $00005C_H$ | — | — | — | — | Reserved |
| $000060_H$ | TMRLRA0 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR0 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 0 |
| $000064_H$ | TMRLRB0 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR0 [R/W] B,H,W<br>00000000 0-000000 | | |
| $000068_H$ | TMRLRA7 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR7 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 7 |
| $00006C_H$ | TMRLRB7 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR7 [R/W] B,H,W<br>00000000 0-000000 | | |
| $000070_H$ | — | FRS8 [R/W] B,H,W<br>--00--00 --00--00 --00--00 | | | Free-run timer selection register 8 |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000CF0_H$ | DCCR15 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | DMA Controller [S] |
| $000CF4_H$ | DCSR15 [R/W] H<br>0------- -----000 | | DTCR15 [R/W] H<br>00000000 00000000 | | |
| $000CF8_H$ | DSAR15 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000CFC_H$ | DDAR15 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000D00_H$ to $000DF0_H$ | — | — | — | — | Reserved [S] |
| $000DF4_H$ | — | — | DNMIR [R/W] B<br>0------0 | DILVR [R/W] B<br>---11111 | DMA Controller [S] |
| $000DF8_H$ | DMACR[R/W] W<br>0------- -------- 0------- -------- | | | | |
| $000DFC_H$ | — | — | — | — | Reserved [S] |
| $000E00_H$ | DDR00 [R/W] B,H,W<br>00000000 | DDR01 [R/W] B,H,W<br>00000000 | DDR02 [R/W] B,H,W<br>00000000 | DDR03 [R/W] B,H,W<br>00000000 | Data Direction Register |
| $000E04_H$ | DDR04 [R/W] B,H,W<br>00000000 | DDR05 [R/W] B,H,W<br>00000000 | DDR06 [R/W] B,H,W<br>00000000 | DDR07 [R/W] B,H,W<br>00000000 | |
| $000E08_H$ | DDR08 [R/W] B,H,W<br>00000000 | DDR09 [R/W] B,H,W<br>00000000 | DDR10 [R/W] B,H,W<br>00000000 | DDR11 [R/W] B,H,W<br>00000000 | Data Direction Register |
| $000E0C_H$ | DDR12 [R/W] B,H,W<br>00000000 | DDR13 [R/W] B,H,W<br>-0000000 | DDR14 [R/W] B,H,W<br>---000-- | DDR15 [R/W] B,H,W<br>--000000 | |
| $000E10_H$ | — | — | — | — | |
| $000E14_H$ | — | — | — | — | |
| $000E18_H$ | DDR16 [R/W] B,H,W<br>00000000 | DDR17 [R/W] B,H,W<br>00000000 | DDR18 [R/W] B,H,W<br>00000000 | DDR19 [R/W] B,H,W<br>00000000 | |
| $000E1C_H$ | — | — | — | — | Reserved |
| $000E20_H$ | PFR00 [R/W] B,H,W<br>00000000 | PFR01 [R/W] B,H,W<br>00000000 | PFR02 [R/W] B,H,W<br>00000000 | PFR03 [R/W] B,H,W<br>00000000 | Port Function Register |
| $000E24_H$ | PFR04 [R/W] B,H,W<br>00000000 | PFR05 [R/W] B,H,W<br>00000000 | PFR06 [R/W] B,H,W<br>00000000 | PFR07 [R/W] B,H,W<br>00000000 | |
| $000E28_H$ | PFR08 [R/W] B,H,W<br>00000000 | PFR09 [R/W] B,H,W<br>00000000 | PFR10 [R/W] B,H,W<br>00000000 | PFR11 [R/W] B,H,W<br>00000000 | |
| $000E2C_H$ | PFR12 [R/W] B,H,W<br>00000000 | PFR13 [R/W] B,H,W<br>-0000000 | PFR14 [R/W] B,H,W<br>---000-- | PFR15 [R/W] B,H,W<br>--000000 | |
| $000E30_H$ | — | — | — | — | |
| $000E34_H$ | — | — | — | — | |
| $000E38_H$ | PFR16 [R/W] B,H,W<br>00000000 | PFR17 [R/W] B,H,W<br>00000000 | PFR18 [R/W] B,H,W<br>00000000 | PFR19 [R/W] B,H,W<br>00000000 | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000E3C$_H$ | — | — | — | — | Reserved |
| 000E40$_H$ | PDDR00 [R] B,H,W XXXXXXXX | PDDR01 [R] B,H,W XXXXXXXX | PDDR02 [R] B,H,W XXXXXXXX | PDDR03 [R] B,H,W XXXXXXXX | Port Direct Read Register |
| 000E44$_H$ | PDDR04 [R] B,H,W XXXXXXXX | PDDR05 [R] B,H,W XXXXXXXX | PDDR06 [R] B,H,W XXXXXXXX | PDDR07 [R] B,H,W XXXXXXXX | |
| 000E48$_H$ | PDDR08 [R] B,H,W XXXXXXXX | PDDR09 [R] B,H,W XXXXXXXX | PDDR10 [R] B,H,W XXXXXXXX | PDDR11 [R] B,H,W XXXXXXXX | |
| 000E4C$_H$ | PDDR12 [R] B,H,W XXXXXXXX | PDDR13 [R] B,H,W -XXXXXXX | PDDR14 [R] B,H,W ---XXX-- | PDDR15 [R] B,H,W --XXXXXX | |
| 000E50$_H$ | — | — | — | — | |
| 000E54$_H$ | — | — | — | — | |
| 000E58$_H$ | PDDR16 [R] B,H,W XXXXXXXX | PDDR17 [R] B,H,W XXXXXXXX | PDDR18 [R] B,H,W XXXXXXXX | PDDR19 [R] B,H,W XXXXXXXX | |
| 000E5C$_H$ | — | — | — | — | Reserved |
| 000E60$_H$ | EPFR00 [R/W] B,H,W 00000000 | EPFR01 [R/W] B,H,W -0-0-000 | EPFR02 [R/W] B,H,W ----0000 | EPFR03 [R/W] B,H,W ---000-0 | Extended Port Function Register |
| 000E64$_H$ | EPFR04 [R/W] B,H,W ----00-0 | EPFR05 [R/W] B,H,W ----0000 | EPFR06 [R/W] B,H,W ----000- | EPFR07 [R/W] B,H,W ---00000 | |
| 000E68$_H$ | EPFR08 [R/W] B,H,W ---00000 | EPFR09 [R/W] B,H,W -----00- | EPFR10 [R/W] B,H,W ----0000 | EPFR11 [R/W] B,H,W ----0000 | |
| 000E6C$_H$ | EPFR12 [R/W] B,H,W ----0000 | EPFR13 [R/W] B,H,W ------00 | EPFR14 [R/W] B,H,W ------00 | EPFR15 [R/W] B,H,W -----000 | |
| 000E70$_H$ | — | — | — | — | |
| 000E74$_H$ | — | — | — | — | |
| 000E78$_H$ | — | — | EPFR26 [R/W] B,H,W 00000000 | EPFR27 [R/W] B,H,W ---0---- | |
| 000E7C$_H$ | EPFR28 [R/W] B,H,W --000-0- | EPFR29 [R/W] B,H,W 00000000 | — | — | |
| 000E80$_H$ | — | EPFR33 [R/W] B,H,W -----00- | EPFR34 [R/W] B,H,W -----00- | EPFR35 [R/W] B,H,W ---00000 | |
| 000E84$_H$ | EPFR36 [R/W] B,H,W ----000- | — | — | — | |
| 000E88$_H$ | — | — | EPFR42 [R/W] B,H,W ------00 | EPFR43 [R/W] B,H,W 0--0000- | |
| 000E8C$_H$ | EPFR44 [R/W] B,H,W -00---0- | EPFR45 [R/W] B,H,W -0000000 | — | — | |
| 000E90$_H$ | — | — | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $001500_H$ | ADTCD36[R] B,H,W<br>10--0000 00000000 | | ADTCD37[R] B,H,W<br>10--0000 00000000 | | 12-bit A/D converter 2/2 unit |
| $001504_H$ | ADTCD38[R] B,H,W<br>10--0000 00000000 | | ADTCD39[R] B,H,W<br>10--0000 00000000 | | |
| $001508_H$ | ADTCD40[R] B,H,W<br>10--0000 00000000 | | ADTCD41[R] B,H,W<br>10--0000 00000000 | | |
| $00150C_H$ | ADTCD42[R] B,H,W<br>10--0000 00000000 | | ADTCD43[R] B,H,W<br>10--0000 00000000 | | |
| $001510_H$ | ADTCD44[R] B,H,W<br>10--0000 00000000 | | ADTCD45[R] B,H,W<br>10--0000 00000000 | | |
| $001514_H$ | ADTCD46[R] B,H,W<br>10--0000 00000000 | | ADTCD47[R] B,H,W<br>10--0000 00000000 | | |
| $001518_H$ to $001534_H$ | — | — | — | — | Reserved |
| $001538_H$ | ADTECS32[R/W] B,H,W<br>-------0 ----0000 | | ADTECS33[R/W] B,H,W<br>-------0 ----0000 | | 12-bit A/D converter 2/2 unit |
| $00153C_H$ | ADTECS34[R/W] B,H,W<br>-------0 ----0000 | | ADTECS35[R/W] B,H,W<br>-------0 ----0000 | | |
| $001540_H$ | ADTECS36[R/W] B,H,W<br>-------0 ----0000 | | ADTECS37[R/W] B,H,W<br>-------0 ----0000 | | |
| $001544_H$ | ADTECS38[R/W] B,H,W<br>-------0 ----0000 | | ADTECS39[R/W] B,H,W<br>-------0 ----0000 | | |
| $001548_H$ | ADTECS40[R/W] B,H,W<br>-------0 ----0000 | | ADTECS41[R/W] B,H,W<br>-------0 ----0000 | | |
| $00154C_H$ | ADTECS42[R/W] B,H,W<br>-------0 ----0000 | | ADTECS43[R/W] B,H,W<br>-------0 ----0000 | | |
| $001550_H$ | ADTECS44[R/W] B,H,W<br>-------0 ----0000 | | ADTECS45[R/W] B,H,W<br>-------0 ----0000 | | |
| $001554_H$ | ADTECS46[R/W] B,H,W<br>-------0 ----0000 | | ADTECS47[R/W] B,H,W<br>-------0 ----0000 | | |
| $001558_H$ to $001574_H$ | — | — | — | — | Reserved |
| $001578_H$ | ADRCUT4[R/W] B,H,W<br>----0000 00000000 | | ADRCLT4[R/W] B,H,W<br>----0000 00000000 | | 12-bit A/D converter 2/2 unit |
| $00157C_H$ | ADRCUT5[R/W] B,H,W<br>----0000 00000000 | | ADRCLT5[R/W] B,H,W<br>----0000 00000000 | | |
| $001580_H$ | ADRCUT6[R/W] B,H,W<br>----0000 00000000 | | ADRCLT6[R/W] B,H,W<br>----0000 00000000 | | |
| $001584_H$ | ADRCUT7[R/W] B,H,W<br>----0000 00000000 | | ADRCLT7[R/W] B,H,W<br>----0000 00000000 | | |

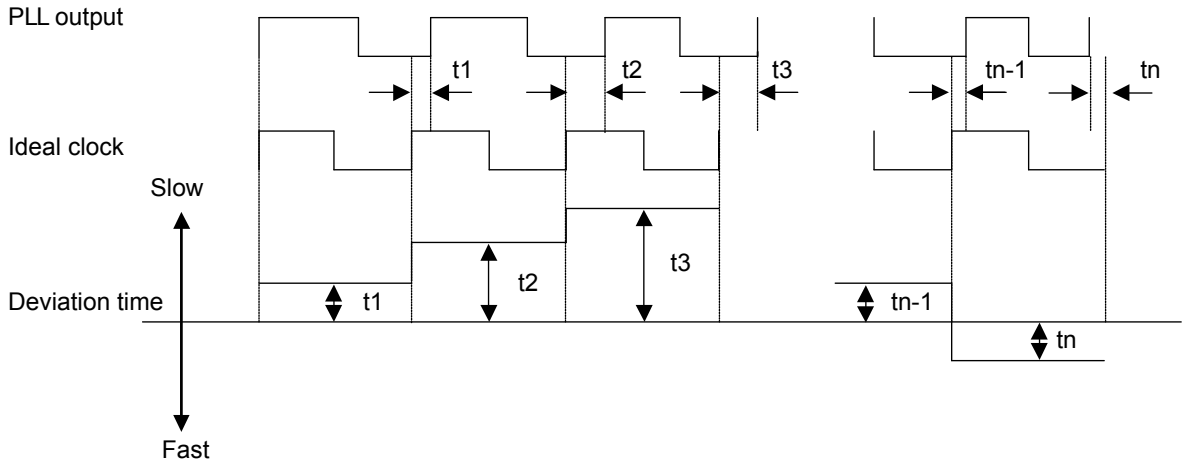
| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0018B0H | FCR18[R/W] B,H,W ---00100 | FCR08[R/W] B,H,W -0000000 | FBYTE8[R/W] B,H,W 00000000 00000000 | | Multi-UART8 |
| 0018B4H | FTICR8[R/W] B,H,W 00000000 00000000 | | — | — | |
| 0018B8H | SCR9/(IBCR9) [R/W] B,H,W 0--00000 | SMR9[R/W] B,H,W 000-00-0 | SSR9[R/W] B,H,W 0-000011 | ESCR9/(IBSR9)[R/W] B,H,W 00000000 | Multi-UART9<br>*1: Byte access is possible only for access to lower 8 bits.<br>*2: Reserved because I2C mode is not set immediately after reset.<br>*3: Reserved because CSIO mode is not set immediately after reset.<br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 0018BCH | — /(RDR19/(TDR19))[R/W] B,H,W -------- -------- *3 | | RDR09/(TDR09)[R/W] B,H,W -------0 00000000 *1 | | |
| 0018C0H | SACSR9[R/W] B,H,W 0----000 00000000 | | STMR9[R] B,H,W 00000000 00000000 | | |
| 0018C4H | STMCR9[R/W] B,H,W 00000000 00000000 | | — /(SCSCR9/SFUR9)[R/W] B,H,W -------- -------- *3 *4 | | |
| 0018C8H | — /(SCSTR39)/ (LAMSR9) [R/W] B,H,W -------- *3 | — /(SCSTR29)/ (LAMCR9) [R/W] B,H,W -------- *3 | — /(SCSTR19)/ (SFLR19) [R/W] B,H,W -------- *3 | — /(SCSTR09)/ (SFLR09) [R/W] B,H,W -------- *3 | |
| 0018CCH | — | — /(SCSFR29) [R/W] B,H,W -------- *3 | — /(SCSFR19) [R/W] B,H,W -------- *3 | — /(SCSFR09) [R/W] B,H,W -------- *3 | |
| 0018D0H | —/(TBYTE39)/ (LAMESR9) [R/W] B,H,W -------- *3 | —/(TBYTE29)/ (LAMERT9) [R/W] B,H,W -------- *3 | —/(TBYTE19)/ (LAMIER9) [R/W] B,H,W -------- *3 | TBYTE09/(LAMRID9) / (LAMTID9) [R/W] B,H,W 00000000 | |
| 0018D4H | BGR9[R/W] H, W 00000000 00000000 | | — /(ISMK9)[R/W] B,H,W -------- *2 | — /(ISBA9)[R/W] B,H,W -------- *2 | |
| 0018D8H | FCR19[R/W] B,H,W ---00100 | FCR09[R/W] B,H,W -0000000 | FBYTE9[R/W] B,H,W 00000000 00000000 | | |
| 0018DCH | FTICR9[R/W] B,H,W 00000000 00000000 | | — | — | |
| 0018E0H | SCR10/(IBCR10) [R/W] B,H,W 0--00000 | SMR10[R/W] B,H,W 000-00-0 | SSR10[R/W] B,H,W 0-000011 | ESCR10/(IBSR10) [R/W] B,H,W 00000000 | Multi-UART10<br>*1: Byte access is possible only for access to lower 8 bits.<br>*2: Reserved because I2C mode is not set immediately after reset. |
| 0018E4H | — /(RDR110/(TDR110))[R/W] B,H,W -------- -------- *3 | | RDR010/(TDR010)[R/W] B,H,W -------0 00000000 *1 | | |
| 0018E8H | SACSR10[R/W] B,H,W 0----000 00000000 | | STMR10[R] B,H,W 00000000 00000000 | | |
| 0018ECH | STMCR10[R/W] B,H,W 00000000 00000000 | | — /(SCSCR10/SFUR10)[R/W] B,H,W -------- -------- *3 *4 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $001928_H$ | FCR111[R/W] B,H,W ---00100 | FCR011[R/W] B,H,W -0000000 | FBYTE11[R/W] B,H,W 00000000 00000000 | | Multi-UART11 |
| $00192C_H$ | FTICR11[R/W] B,H,W 00000000 00000000 | | — | — | |
| $001930_H$ to $0019D8_H$ | — | — | — | — | Reserved |
| $0019DC_H$ | — | GATEC0 [R/W] B,H,W ------00 | — | GATEC2 [R/W] B,H,W ------00 | PPG GATE control |
| $0019E0_H$ | — | GATEC4 [R/W] B,H,W ------00 | — | — | |
| $0019E4_H$ | — | — | — | — | Reserved |
| $0019E8_H$ | GTRS0 [R/W] B,H,W -0000000 -0000000 | | GTRS1 [R/W] B,H,W -0000000 -0000000 | | PPG controller |
| $0019EC_H$ | GTRS2 [R/W] B,H,W -0000000 -0000000 | | GTRS3 [R/W] B,H,W -0000000 -0000000 | | |
| $0019F0_H$ | GTRS4 [R/W] B,H,W -0000000 -0000000 | | GTRS5 [R/W] B,H,W -0000000 -0000000 | | |
| $0019F4_H$ | GTRS6 [R/W] B,H,W -0000000 -0000000 | | GTRS7 [R/W] B,H,W -0000000 -0000000 | | |
| $0019F8_H$ | GTRS8 [R/W] B,H,W -0000000 -0000000 | | GTRS9 [R/W] B,H,W -0000000 -0000000 | | PPG controller |
| $0019FC_H$ | GTRS10 [R/W] B,H,W -0000000 -0000000 | | GTRS11 [R/W] B,H,W -0000000 -0000000 | | |
| $001A00_H$ | GTRS12 [R/W] B,H,W -0000000 -0000000 | | GTRS13 [R/W] B,H,W -0000000 -0000000 | | |
| $001A04_H$ | GTRS14 [R/W] B,H,W -0000000 -0000000 | | GTRS15 [R/W] B,H,W -0000000 -0000000 | | |
| $001A08_H$ | GTRS16 [R/W] B,H,W -0000000 -0000000 | | GTRS17 [R/W] B,H,W -0000000 -0000000 | | |
| $001A0C_H$ | GTRS18 [R/W] B,H,W -0000000 -0000000 | | GTRS19 [R/W] B,H,W -0000000 -0000000 | | |
| $001A10_H$ | GTRS20 [R/W] B,H,W -0000000 -0000000 | | GTRS21 [R/W] B,H,W -0000000 -0000000 | | |
| $001A14_H$ | GTRS22 [R/W] B,H,W -0000000 -0000000 | | GTRS23 [R/W] B,H,W -0000000 -0000000 | | |
| $001A18_H$ to $001A2C_H$ | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001D70$_H$ to 001FFC$_H$ | — | — | — | — | Reserved |
| 002000$_H$ | CTRLR0 [R/W] B,H,W<br>-------- 000-0001 | | STATR0 [R/W] B,H,W<br>-------- 00000000 | | CAN0 (128msb) |
| 002004$_H$ | ERRCNT0 [R] B,H,W<br>00000000 00000000 | | BTR0 [R/W] B,H,W<br>-0100011 00000001 | | |
| 002008$_H$ | INTR0 [R] B,H,W<br>00000000 00000000 | | TESTR0 [R/W] B,H,W<br>-------- X00000-- | | |
| 00200C$_H$ | BRPER0 [R/W] B,H,W<br>-------- ----0000 | | — | — | |
| 002010$_H$ | IF1CREQ0 [R/W] B,H,W<br>0------- 00000001 | | IF1CMSK0 [R/W] B,H,W<br>-------- 00000000 | | |
| 002014$_H$ | IF1MSK20 [R/W] B,H,W<br>11-11111 11111111 | | IF1MSK10 [R/W] B,H,W<br>11111111 11111111 | | |
| 002018$_H$ | IF1ARB20 [R/W] B,H,W<br>00000000 00000000 | | IF1ARB10 [R/W] B,H,W<br>00000000 00000000 | | |
| 00201C$_H$ | IF1MCTR0 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002020$_H$ | IF1DTA10 [R/W] B,H,W<br>00000000 00000000 | | IF1DTA20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002024$_H$ | IF1DTB10 [R/W] B,H,W<br>00000000 00000000 | | IF1DTB20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002028$_H$ | — | — | — | — | |
| 00202C$_H$ | — | — | — | — | |
| 002030$_H$, 002034$_H$ | Reserved(IF1 data mirror) | | | | |
| 002038$_H$ | — | — | — | — | |
| 00203C$_H$ | — | — | — | — | |
| 002040$_H$ | IF2CREQ0 [R/W] B,H,W<br>0------- 00000001 | | IF2CMSK0 [R/W] B,H,W<br>-------- 00000000 | | |
| 002044$_H$ | IF2MSK20 [R/W] B,H,W<br>11-11111 11111111 | | IF2MSK10 [R/W] B,H,W<br>11111111 11111111 | | |
| 002048$_H$ | IF2ARB20 [R/W] B,H,W<br>00000000 00000000 | | IF2ARB10 [R/W] B,H,W<br>00000000 00000000 | | |
| 00204C$_H$ | IF2MCTR0 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002050$_H$ | IF2DTA10 [R/W] B,H,W<br>00000000 00000000 | | IF2DTA20 [R/W] B,H,W<br>00000000 00000000 | | |

• CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



(4-1-4) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=1, SCR:SPI=1
($T_A$:-40°C to +125°C, $V_{CC}$=$AV_{CC}$=5.0V±10%/$V_{CC}$=$AV_{CC}$=3.3V±0.3V, $V_{SS}$=$AV_{SS}$=0.0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK11 | - | $4t_{CPP}$ | - | ns | Internal shift clock mode output pin : $C_L$=50pF |
| SCK↓→ SOT delay time | $t_{SLOVI}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | -30 | 30 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | -300 | 300 | ns | |
| Valid SIN → SCK↑setup time | $t_{IVSHI}$ | SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11 | | 34 | - | ns | |
| | | SCK3 , SCK4 SIN3 , SIN4 | | 300 | - | ns | |
| SCK↑→ Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK11 SIN0 to SIN11 | | 0 | - | ns | |
| SOT→SCK↑ delay time | $t_{SOVHI}$ | SCK0 to SCK11 SOT0 to SOT11 | | $2t_{CPP}$-30 | - | ns | |
| Serial clock "H"pulse width | $t_{SHSL}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | External shift clock mode output pin: $C_L$=50pF |
| Serial clock "L" pulse width | $t_{SLSH}$ | | | $2t_{CPP}$-10 | - | ns | |
| SCK↓→ SOT delay time | $t_{SLOVE}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | - | 33 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | - | 300 | ns | |
| Valid SIN → SCK↑setup time | $t_{IVSHE}$ | SCK0 to SCK11 SIN0 to SIN11 | | 10 | - | ns | |
| SCK↑→ Valid SIN hold time | $t_{SHIXE}$ | | | 20 | - | ns | |
| SCK fall time | $t_F$ | SCK0 to SCK11 | | - | 5 | ns | |
| SCK rise time | $t_R$ | SCK0 to SCK11 | | - | 5 | ns | |

**Notes:**
AC characteristic in CLK synchronized mode.
$C_L$ is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

(9) Low voltage detection (Internal low-voltage detection)
($T_A$: -40°C to +125°C, $V_{SS}$=$AV_{SS}$=0.0V)

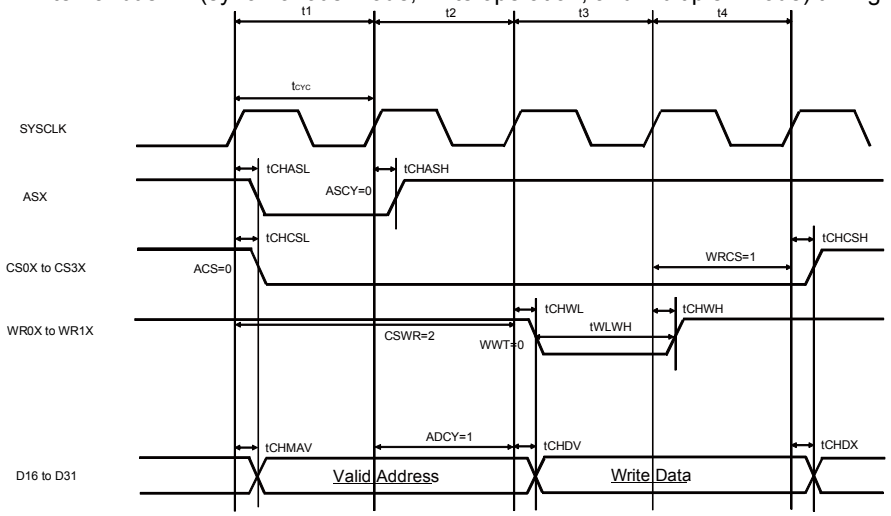
| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply voltage range | $V_{RDP5}$ | - | - | 0.6 | - | 1.4 | V | |
| Detection voltage*2 | $V_{RDL}$ | | *1 | 0.8 | 0.9 | 1.0 | V | When power-supply voltage falls |
| Hysteresis width | $V_{RHYS}$ | | - | - | 0.1 | - | V | When power-supply voltage rises |
| Low voltage detection time | - | - | | - | - | 30 | µs | |

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.
*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V.
This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

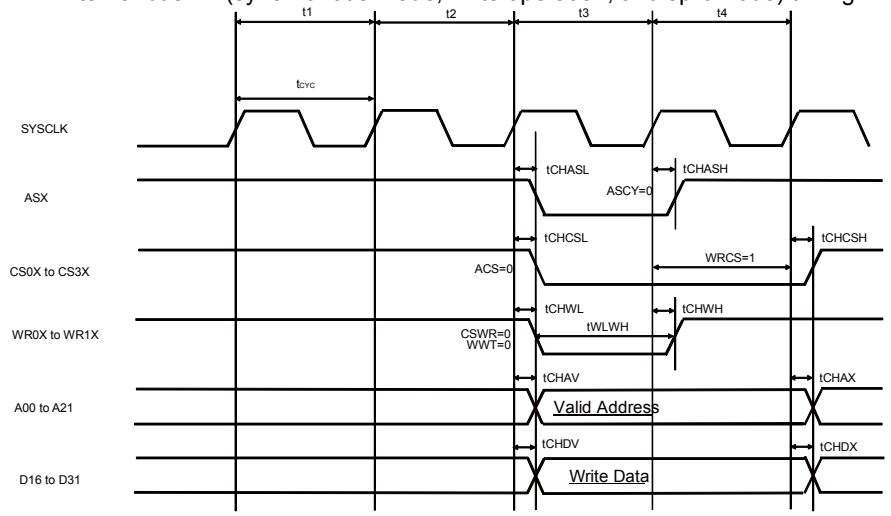
(10) External bus I/F (synchronous mode) timing
($T_A$: -40°C to +105°C, $V_{CC}$=$AV_{CC}$=5.0V±10%/$V_{CC}$= $AV_{CC}$=3.3V±0.3V, $V_{SS}$=$AV_{SS}$=0.0V)
(external load capacitance 50pF)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | SYSCLK | 25 | - | ns | $V_{CC}$=5.0V±10%*1 |
| | | | 31.25 | | | $V_{CC}$=3.3V±0.3V |
| ASX delay time | $t_{CHASL}$, $t_{CHASH}$ | SYSCLK ASX | 0.5 | 18 | ns | |
| CS0X to CS3X delay time | $t_{CHCSL}$, $t_{CHCSH}$ | SYSCLK CS0X to CS3X | 0.5 | 18 | ns | |
| A00 to A21 delay time | $t_{CHAV}$, $t_{CHAX}$ | SYSCLK A00 to A21 | 0.5 | 18 | ns | |
| RDX delay time | $t_{CHRL}$, $t_{CHRH}$ | SYSCLK RDX | 0.5 | 18 | ns | |
| RDX minimum pulse | $t_{RLRH}$ | RDX | $t_{CYC}$× 2 - 20 | - | ns | RWT=1, set RWT to 1 or more.*2 |
| Data setup → RDX↑time | $t_{DSRH}$ | RDX D16 to D31 | 18+$t_{CYC}$ | - | ns | Same as above |
| RDX↑→ data hold | $t_{RHDH}$ | | 0 | - | ns | |

External bus I/F (synchronous mode, write operation, and multiplex mode) timing




External bus I/F (synchronous mode, write operation, and split mode) timing

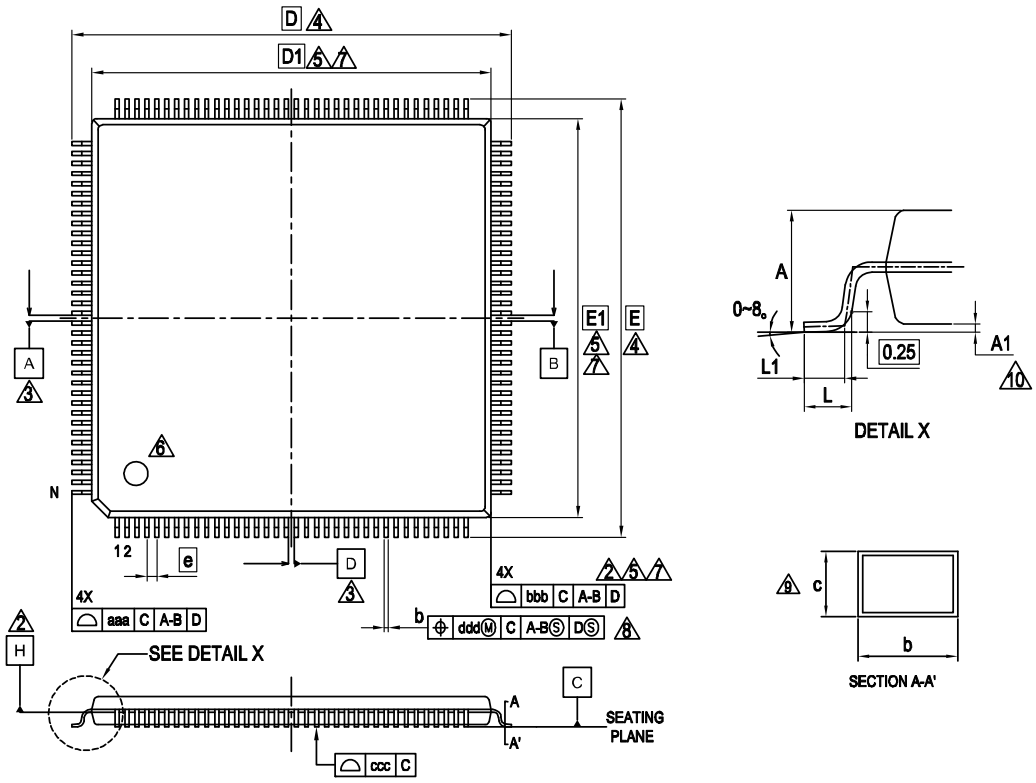


| Part number | Sub clock | CSV Initial value | LVD Initial value | Package*2 |
|---|---|---|---|---|
| MB91F526JWBPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| MB91F526JYBPMC | | | OFF | |
| MB91F526JJBPMC | | OFF | ON | |
| MB91F526JLBPMC | | | OFF | |
| MB91F525JWBPMC | | ON | ON | |
| MB91F525JYBPMC | | | OFF | |
| MB91F525JJBPMC | | OFF | ON | |
| MB91F525JLBPMC | | | OFF | |
| MB91F524JWBPMC | | ON | ON | |
| MB91F524JYBPMC | | | OFF | |
| MB91F524JJBPMC | | OFF | ON | |
| MB91F524JLBPMC | | | OFF | |
| MB91F523JWBPMC | | ON | ON | |
| MB91F523JYBPMC | | | OFF | |
| MB91F523JJBPMC | | OFF | ON | |
| MB91F523JLBPMC | | | OFF | |
| MB91F522JWBPMC | | ON | ON | |
| MB91F522JYBPMC | | | OFF | |
| MB91F522JJBPMC | | OFF | ON | |
| MB91F522JLBPMC | | | OFF | |
| MB91F526JSBPMC | None | ON | ON | |
| MB91F526JUBPMC | | | OFF | |
| MB91F526JHBPMC | | OFF | ON | |
| MB91F526JKBPMC | | | OFF | |
| MB91F525JSBPMC | | ON | ON | |
| MB91F525JUBPMC | | | OFF | |
| MB91F525JHBPMC | | OFF | ON | |
| MB91F525JKBPMC | | | OFF | |
| MB91F524JSBPMC | | ON | ON | |
| MB91F524JUBPMC | | | OFF | |
| MB91F524JHBPMC | | OFF | ON | |
| MB91F524JKBPMC | | | OFF | |
| MB91F523JSBPMC | | ON | ON | |
| MB91F523JUBPMC | | | OFF | |
| MB91F523JHBPMC | | OFF | ON | |
| MB91F523JKBPMC | | | OFF | |
| MB91F522JSBPMC | | ON | ON | |
| MB91F522JUBPMC | | | OFF | |
| MB91F522JHBPMC | | OFF | ON | |
| MB91F522JKBPMC | | | OFF | |

| Part number | Sub clock | CSV Initial value | LVD Initial value | Package*2 |
|---|---|---|---|---|
| MB91F526FWBPMC | Yes | ON | ON | LQI・100 pin, Plastic |
| MB91F526FYBPMC | | | OFF | |
| MB91F526FJBPMC | | OFF | ON | |
| MB91F526FLBPMC | | | OFF | |
| MB91F525FWBPMC | | ON | ON | |
| MB91F525FYBPMC | | | OFF | |
| MB91F525FJBPMC | | OFF | ON | |
| MB91F525FLBPMC | | | OFF | |
| MB91F524FWBPMC | | ON | ON | |
| MB91F524FYBPMC | | | OFF | |
| MB91F524FJBPMC | | OFF | ON | |
| MB91F524FLBPMC | | | OFF | |
| MB91F523FWBPMC | | ON | ON | |
| MB91F523FYBPMC | | | OFF | |
| MB91F523FJBPMC | | OFF | ON | |
| MB91F523FLBPMC | | | OFF | |
| MB91F522FWBPMC | | ON | ON | |
| MB91F522FYBPMC | | | OFF | |
| MB91F522FJBPMC | | OFF | ON | |
| MB91F522FLBPMC | | | OFF | |
| MB91F526FSBPMC | None | ON | ON | |
| MB91F526FUBPMC | | | OFF | |
| MB91F526FHBPMC | | OFF | ON | |
| MB91F526FKBPMC | | | OFF | |
| MB91F525FSBPMC | | ON | ON | |
| MB91F525FUBPMC | | | OFF | |
| MB91F525FHBPMC | | OFF | ON | |
| MB91F525FKBPMC | | | OFF | |
| MB91F524FSBPMC | | ON | ON | |
| MB91F524FUBPMC | | | OFF | |
| MB91F524FHBPMC | | OFF | ON | |
| MB91F524FKBPMC | | | OFF | |
| MB91F523FSBPMC | | ON | ON | |
| MB91F523FUBPMC | | | OFF | |
| MB91F523FHBPMC | | OFF | ON | |
| MB91F523FKBPMC | | | OFF | |
| MB91F522FSBPMC | | ON | ON | |
| MB91F522FUBPMC | | | OFF | |
| MB91F522FHBPMC | | OFF | ON | |
| MB91F522FKBPMC | | | OFF | |

| Part number | Sub clock | CSV Initial value | LVD Initial value | Package*2 |
|---|---|---|---|---|
| MB91F526JWCPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| MB91F526JYCPMC | | | OFF | |
| MB91F526JJCPMC | | OFF | ON | |
| MB91F526JLCPMC | | | OFF | |
| MB91F525JWCPMC | | ON | ON | |
| MB91F525JYCPMC | | | OFF | |
| MB91F525JJCPMC | | OFF | ON | |
| MB91F525JLCPMC | | | OFF | |
| MB91F524JWCPMC | | ON | ON | |
| MB91F524JYCPMC | | | OFF | |
| MB91F524JJCPMC | | OFF | ON | |
| MB91F524JLCPMC | | | OFF | |
| MB91F523JWCPMC | | ON | ON | |
| MB91F523JYCPMC | | | OFF | |
| MB91F523JJCPMC | | OFF | ON | |
| MB91F523JLCPMC | | | OFF | |
| MB91F522JWCPMC | | ON | ON | |
| MB91F522JYCPMC | | | OFF | |
| MB91F522JJCPMC | | OFF | ON | |
| MB91F522JLCPMC | | | OFF | |
| MB91F526JSCPMC | None | ON | ON | |
| MB91F526JUCPMC | | | OFF | |
| MB91F526JHCPMC | | OFF | ON | |
| MB91F526JKCPMC | | | OFF | |
| MB91F525JSCPMC | | ON | ON | |
| MB91F525JUCPMC | | | OFF | |
| MB91F525JHCPMC | | OFF | ON | |
| MB91F525JKCPMC | | | OFF | |
| MB91F524JSCPMC | | ON | ON | |
| MB91F524JUCPMC | | | OFF | |
| MB91F524JHCPMC | | OFF | ON | |
| MB91F524JKCPMC | | | OFF | |
| MB91F523JSCPMC | | ON | ON | |
| MB91F523JUCPMC | | | OFF | |
| MB91F523JHCPMC | | OFF | ON | |
| MB91F523JKCPMC | | | OFF | |
| MB91F522JSCPMC | | ON | ON | |
| MB91F522JUCPMC | | | OFF | |
| MB91F522JHCPMC | | OFF | ON | |
| MB91F522JKCPMC | | | OFF | |

## LQN144 , 144 Lead Plastic Low Profile Quad Flat Package




| PACKAGE | LQN144 | | |
|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. |
| A | —— | —— | 1.70 |
| A1 | 0.05 | —— | 0.15 |
| b | 0.145 | 0.18 | 0.215 |
| c | 0.115 | —— | 0.195 |
| D | 18.00 BSC. | | |
| D1 | 16.00 BSC. | | |
| e | 0.40 BSC | | |
| E | 18.00 BSC. | | |
| E1 | 16.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| aaa | —— | —— | 0.20 |
| bbb | —— | —— | 0.10 |
| ccc | —— | —— | 0.08 |
| ddd | —— | —— | 0.07 |
| N | 144 | | |

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

| Page | Section | Change Results |
|---|---|---|
| 23, 24 | ■PIN Description | (Continued)<br>(Correct) |

| Pin no. | | | | | | Pin Name |
|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | |
| 15 *1 | 18 *1 | 23 *1 | 27 *1 | 30 | 37 | P047 |
| | | | | | | A17 *2, *3, *4, *5 |
| | | | | | | AN45 |
| | | | | | | TRG8_0 |
| | | | | | | TIN3_2 |
| | | | | | | SOT0_1 |
| - | - | - | - | - | 38 | P177 |
| | | | | | | TRG11_0 |
| - | - | - | 28 *1 | 31 | 39 | P050 |
| | | | | | | A18 *5 |
| | | | | | | TRG5_1 |
| | | | | | | PPG33_0 |
| - | - | - | - | 32 | 40 | P051 |
| | | | | | | A19 |
| | | | | | | TRG9_0 |
| - | - | - | - | 33 | 41 | P052 |
| | | | | | | A20 |
| | | | | | | PPG34_0 |
| | | | | | | INT14_0 |
| 16 *1 | 19 *1 | 24 *1 | 29 *1 | 34 | 42 | P053 |
| | | | | | | A21 *2, *3, *4, *5 |
| | | | | | | AN44 |
| | | | | | | PPG35_0 |
| | | | | | | INT14_1 |
| | | | | | | SCK0_1 |
| - | - | - | - | 35 | 43 | P054 |
| | | | | | | SYSCLK |
| | | | | | | PPG36_0 |
| 17 *1 | 22 *1 | 27 *1 | 32 *1 | 38 | 46 | P055 |
| | | | | | | CS2X *2, *3, *4, *5 |
| | | | | | | SIN10_0 |
| | | | | | | AN43 |
| | | | | | | PPG37_0 |
| | | | | | | TIN4_1 |
| | | | | | | |
| - | - | - | 33 *1 | 39 | 49 | P056 |
| | | | | | | CS3X *5 |
| | | | | | | ICU9_0 |
| | | | | | | PPG0_1 |
| | | | | | | ICU0_1 |
| | | | | | | TIN5_1 |
| | | | | | | DTTI_2 |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type L in "I/O Circuit Types" modified as follows:<br><br>(Error)<br>- Open-drain I/O<br>- Output 25mA (NOD)<br>- TTL input<br><br>(Correct)<br>- Open-drain I/O<br>- Output 25mA (Nch open-drain)<br>- TTL input</td></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type M in "I/O Circuit Types" modified as follows:<br><br>(Error)<br>- CMOS hysteresis input<br>- Pull-up resistor 50kΩ (5V cont)<br><br>(Correct)<br>- CMOS hysteresis input<br>- Pull-up resistor 50kΩ</td></tr>
<tr><td>121</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 64pins.<br>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>124</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 80pin modified as follows:<br><br>(Error)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">$308_H$</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45*5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">$308_H$</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
</table>

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | (4-1-5)SCK↑⇒SCS↑hold time $t_{CSHI}$<br>(4-1-6)SCK↓⇒SCS↑hold time $t_{CSHI}$<br>(4-1-7)SCK↑⇒SCS↓hold time $t_{CSHI}$<br>(4-1-8)SCK↓⇒SCS↓hold time $t_{CSHI}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSHD}$-50 Max $t_{CSHD}$+0<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSHD}$-10 Max $t_{CSHD}$+50<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $t_{CSHD}$-300 Max $t_{CSHD}$+50<br>(4-1-5),(4-1-6)SCS↓⇒SOT delay time $t_{DSE}$<br>(4-1-7),(4-1-8)SCS↑⇒SOT delay time $t_{DSE}$<br>Corrected the following description.<br>Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>SOT1 to SOT11<br>Value: Min - Max 40<br>↓<br>Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1,SOT2,SOT5 to SOT11<br>Value: Min - Max 40<br>Pin name: SCS3,SCS40 to SCS43<br>SOT3,SOT4<br>Value: Min - Max 300<br>(4-1-5)SCK↓⇒SCS↓ clock switch time $t_{SCC}$<br>(4-1-6)SCK↑⇒SCS↓ clock switch time $t_{SCC}$<br>(4-1-7)SCK↓⇒SCS↑ clock switch time $t_{SCC}$<br>(4-1-8)SCK↑⇒SCS↑ clock switch time $t_{SCC}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $3t_{CPP}$+0 Max $3t_{CPP}$+50<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $3t_{CPP}$-10 Max $3t_{CPP}$+50<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $3t_{CPP}$-300 Max $3t_{CPP}$+50<br>Added the following description.<br>Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again<br><br>Electrical Characteristics<br>5.A/D Converter |