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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

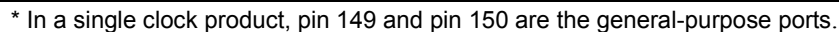
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525fsbpmc-gse2



MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L



Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	P032	-	A	General-purpose I/O port
						A04 ^{*2, *3, *4, *5}	-		External bus/Address bit4 output (0)
						SCS43_1	-		Serial chip select 43 output (1)
						PPG30_0	-		PPG ch.30 output (0)
						TOT3_0	-		Reload timer ch.3 output (0)
						RTO2_1	-		Waveform generator ch.2 output pin (1)
6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	P033	-	A	General-purpose I/O port
						A05 ^{*2, *3, *4, *5}	-		External bus/Address bit5 output (0)
						PPG31_0	-		PPG ch.31 output (0)
						ICU3_3	-		Input capture ch.3 input (3)
						TIN4_0	-		Reload timer ch.4 event input (0)
						RTO1_1	-		Waveform generator ch.1 output pin (1)
7 ^{*1}	9 ^{*1}	11 ^{*1}	14 ^{*1}	17	21	SCK3_2	-		Multi-function serial ch.3 clock I/O (2)
						P034	-	A	General-purpose I/O port
						A06 ^{*2, *3, *4, *5}	-		External bus/Address bit6 output (0)
						OCU11_1	-		Output compare ch.11 output (1)
						ICU2_3	-		Input capture ch.2 input (3)
						TIN5_0	-		Reload timer ch.5 event input (0)
-	-	12	15	18	22	RTO0_1	-		Waveform generator ch.0 output pin (1)
						SOT3_2	-		Multi-function serial ch.3 serial data output (2)
						P150	-	F	General-purpose I/O port
						SOT8_0/ SDA8	-		Multi-function serial ch.8 serial data output (0)/ I ² C bus serial data I/O
						OCU10_1	-		Output compare ch.10 output (1)
						TRG6_0	-		PPG trigger 6 input (0)
8 ^{*1}	10 ^{*1}	13	16	19	23	ICU1_3	-		Input capture ch.1 input (3)
						TIN6_0	-		Reload timer ch.6 event input (0)
						P151	-	F	General-purpose I/O port
						SCK8_0/ SCL8 ^{*2, *3}	-		Multi-function serial ch.8 clock I/O (0)/ I ² C bus serial clock I/O
						OCU9_1	-		Output compare ch.9 output (1)
						TRG7_0	-		PPG trigger 7 input (0)
						ICU0_3	-		Input capture ch.0 input (3)
						TIN7_0	-		Reload timer ch.7 event input (0)
						ZIN0_2	-		U/D counter ch.0 ZIN input (2)
						DTTI_1	-		Waveform generator ch.1 input pin (1)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
13 *1	15 *1	19 *1	22 *1	25	31	P042	-	B	General-purpose I/O port
						A12 *2, *3, *4, *5	-		External bus/Address bit12 output
						SOT9_0	-		Multi-function serial ch.9 serial data output (0)
						AN47	-		ADC analog 47 input
						ICU8_1	-		Input capture ch.8 input (1)
						TRG0_1	-		PPG trigger 0 input (1)
						ZIN1_0	-		U/D counter ch.1 ZIN input (0)
-	-	20 *1	23 *1	26	32	P043	-	A	General-purpose I/O port
						A13 *4, *5	-		External bus/Address bit13 output (0)
						ICU7_1	-		Input capture ch.7 input (1)
						TRG1_1	-		PPG trigger 1 input (1)
-	16 *1	21 *1	24 *1	27	33	P044	-	A	General-purpose I/O port
						A14 *3, *4, *5	-		External bus/Address bit14 output (0)
						SCS9_0	-		Serial chip select 9 I/O (0)
						ICU6_1	-		Input capture ch.6 input (1)
						TRG2_1	-		PPG trigger 2 input (1)
14 *1	17 *1	22 *1	25 *1	28	34	P045	-	G	General-purpose I/O port
						A15 *2, *3, *4, *5	-		External bus/Address bit15 output (0)
						SCK9_0	-		Multi-function serial ch.9 clock I/O (0)
						AN46	-		ADC analog 46 input
						ICU5_1	-		Input capture ch.5 input (1)
						TRG3_1	-		PPG trigger 3 input (1)
						TOT1_2	-		Reload timer ch.1 output (2)
-	-	-	26 *1	29	35	P046	-	A	General-purpose I/O port
						A16 *5	-		External bus/Address bit16 output (0)
						ICU4_1	-		Input capture ch.4 input (1)
						TRG4_1	-		PPG trigger 4 input (1)
-	-	-	-	-	36	P176	-	A	General-purpose I/O port
						TRG10_0	-		PPG trigger 10 input (0)
15 *1	18 *1	23 *1	27 *1	30	37	P047	-	B	General-purpose I/O port
						A17 *2, *3, *4, *5	-		External bus/Address bit17 output (0)
						AN45	-		ADC analog 45 input
						TRG8_0	-		PPG trigger 8 input (0)
						TIN3_2	-		Reload timer ch.3 event input (2)
						SOT0_1	-		Multi-function serial ch.0 serial data output (1)
-	-	-	-	-	38	P177	-	A	General-purpose I/O port
						TRG11_0	-		PPG trigger 11 input (0)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
23	28	34	40	48	59	P062	-	B	General-purpose I/O port
						SCS10_1	-		Serial chip select 10 I/O (1)
						SCS40_0	-		Serial chip select 40 I/O (0)
						AN40	-		ADC analog 40 input
						PPG4_1	-		PPG ch.4 output (1)
						FRCK0_0	-		Free-run timer 0 clock input (0)
						TOT7_1	-		Reload timer ch.7 output (1)
						ZIN1_1	-		U/D counter ch.1 ZIN input (1)
-	29	35	41	49	60	P063	-	B	General-purpose I/O port
						SCS41_0	-		Serial chip select 41 output (0)
						AN39	-		ADC analog 39 input
						PPG5_1	-		PPG ch.5 output (1)
						FRCK1_0	-		Free-run timer 1 clock input (0)
						BIN1_1	-		U/D counter ch.1 BIN input (1)
-	-	-	-	-	61	P183	-	A	General-purpose I/O port
						PPG43_0	-		PPG ch.43 output (0)
24	30	36	42	50	62	P064	-	B	General-purpose I/O port
						SCS42_0	-		Serial chip select 42 output (0)
						AN38	-		ADC analog 38 input
						FRCK2_0	-		Free-run timer 2 clock input (0)
						AIN1_1	-		U/D counter ch.1 AIN input (1)
						PPG43_1	-		PPG ch.43 output (1)
-	-	37	43	51	63	P065	-	A	General-purpose I/O port
						SCS43_0	-		Serial chip select 43 output (0)
						FRCK3_0	-		Free-run timer 3 clock input (0)
						ZIN0_1	-		U/D counter ch.0 ZIN input (1)
						PPG44_1	-		PPG ch.44 output (1)
-	-	-	-	-	64	P184	-	A	General-purpose I/O port
						PPG44_0	-		PPG ch.44 output (0)
-	-	-	-	-	65	P185	-	A	General-purpose I/O port
						PPG45_0	-		PPG ch.45 output (0)
25	31	38	44	52	66	P066	-	B	General-purpose I/O port
						SOT4_2	-		Multi-function serial ch.4 serial data output (2)
						SCS3_0	-		Serial chip select 3 I/O (0)
						AN37	-		ADC analog 37 input
						FRCK4_0	-		Free-run timer 4 clock input (0)
						BIN0_1	-		U/D counter ch.0 BIN input (1)
-	32	39	45	53	67	P067	-	B	General-purpose I/O port
						AN36	-		ADC analog 36 input
						FRCK5_0	-		Free-run timer 5 clock input (0)
						AIN0_1	-		U/D counter ch.0 AIN input (1)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	76	94	P092	-	B	General-purpose I/O port
						AN6	-		ADC analog 6 input
						PPG40_1	-		PPG ch.40 output (1)
						ICU2_0	-		Input capture ch.2 input (0)
						TOT0_1	-		Reload timer ch.0 output (1)
-	-	-	-	-	95	P192	-	A	General-purpose I/O port
						PPG24_1	-		PPG ch.24 output (1)
						TOT1_1	-		Reload timer ch.1 output (1)
34 *1	42 *1	52	62	77	96	P093	-	J	General-purpose I/O port
						TX0_1	-		CAN transmission data 0 output (1)
						SIN11_0	-		Multi-function serial ch.11 serial data input (0)
						AN7	-		ADC analog 7 input
						ICU4_2	-		Input capture ch.4 input (2)
						PPG16_1	-		PPG ch.16 output (1)
						ICU3_0	-		Input capture ch.3 input (0)
						TOT2_1 *2, *3	-		Reload timer ch.2 output (1)
-	-	-	-	78	97	P094	-	B	General-purpose I/O port
						AN8	-		ADC analog 8 input
						ICU4_0	-		Input capture ch.4 input (0)
						TOT3_1	-		Reload timer ch.3 output (1)
-	-	53	63	79	98	P095	-	B	General-purpose I/O port
						TX0(128)	-		CAN transmission data 0 output
						SCS11_0	-		Serial chip select 11 I/O (0)
						AN9	-		ADC analog 9 input
35	43	54	64	80	99	P096	-	G	General-purpose I/O port
						RX0(128)	-		CAN reception data 0 input
						SOT11_0 / SDA11	-		Multi-function serial ch.11 serial data output (0)/I ² C bus serial data I/O
						AN10	-		ADC analog 10 input
						INT0_0	-		INT0 External interrupt input (0)
36	44	55	65	81	100	P097	-	G	General-purpose I/O port
						SCK11_0 / SCL11	-		Multi-function serial ch.11 clock I/O (0)/I ² C bus serial clock I/O
						AN11	-		ADC analog 11 input
						ICU5_0	-		Input capture ch.5 input (0)
						PPG17_1	-		PPG ch.17 output (1)

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000120 _H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU
000124 _H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128 _H	—	—	OCSH67 [R/W] B,H,W ---0--00	OCSL67 [R/W] B,H,W 0000--00	
00012C _H	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU
000130 _H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134 _H	—	—	OCSH89 [R/W] B,H,W ---0--00	OCSL89 [R/W] B,H,W 0000--00	
000138 _H to 0001B4 _H	—	—	—	—	Reserved
0001B8 _H	EPFR64 [R/W] B,H,W ----00-	EPFR65 [R/W] B,H,W 0000-000	EPFR66 [R/W] B,H,W --000000	EPFR67 [R/W] B,H,W ----0000	Extended port function register
0001BC _H	EPFR68 [R/W] B,H,W ----0000	EPFR69 [R/W] B,H,W ----0000	EPFR70 [R/W] B,H,W ---00000	EPFR71 [R/W] B,H,W -0-0-0-0	
0001C0 _H	EPFR72 [R/W] B,H,W 000000-0	EPFR73 [R/W] B,H,W 00000000	EPFR74 [R/W] B,H,W 00000000	EPFR75 [R/W] B,H,W 00000000	
0001C4 _H	EPFR76 [R/W] B,H,W 00000000	EPFR77 [R/W] B,H,W --000000	EPFR78 [R/W] B,H,W -----00	EPFR79 [R/W] B,H,W 00000000	
0001C8 _H	EPFR80 [R/W] B,H,W ---00000	EPFR81 [R/W] B,H,W 00000000	EPFR82 [R/W] B,H,W 00000000	EPFR83 [R/W] B,H,W -0000000	
0001CC _H	EPFR84 [R/W] B,H,W 00000000	EPFR85 [R/W] B,H,W --000000	EPFR86 [R/W] B,H,W ---00000	EPFR87 [R/W] B,H,W -----00	
0001D0 _H	EPFR88 [R/W] B,H,W -----0	—	—	—	
0001D4 _H	—	—	—	—	Reserved
0001D8 _H	TMRLRA4 [R/W] H XXXXXXXX XXXXXXXX		TMR4 [R] H XXXXXXXX XXXXXXXX		Reload Timer 4
0001DC _H	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXX		TMCSR4 [R/W] B, H,W 00000000 0-000000		
0001E0 _H to 0001EC _H	—	—	—	—	Reserved
0001F0 _H	TMRLRA5 [R/W] H XXXXXXXX XXXXXXXX		TMR5 [R] H XXXXXXXX XXXXXXXX		Reload Timer 5
0001F4 _H	TMRLRB5 [R/W] H XXXXXXXX XXXXXXXX		TMCSR5 [R/W] B, H,W 00000000 0-000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440 _H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444 _H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448 _H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
00044C _H	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450 _H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454 _H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458 _H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
00045C _H	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460 _H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464 _H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468 _H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
00046C _H	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470 _H to 00047C _H	—	—	—	—	Reserved [S]
000480 _H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111---0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484 _H	—	—	—	—	Reserved [S]
000488 _H	DIVR0 [R/W] B,H,W 000----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
00048C _H	—	—	—	—	Reserved [S]
000490 _H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494 _H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498 _H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001394 _H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		12-bit A/D converter 1/2 unit
001398 _H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
00139C _H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
0013A0 _H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
0013A4 _H	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
0013A8 _H	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
0013AC _H	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
0013B0 _H	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
0013B4 _H	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
0013B8 _H	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
0013BC _H	ADTCD24[R] B,H,W 10--0000 00000000		ADTCD25[R] B,H,W 10--0000 00000000		
0013C0 _H	ADTCD26[R] B,H,W 10--0000 00000000		ADTCD27[R] B,H,W 10--0000 00000000		
0013C4 _H	ADTCD28[R] B,H,W 10--0000 00000000		ADTCD29[R] B,H,W 10--0000 00000000		
0013C8 _H	ADTCD30[R] B,H,W 10--0000 00000000		ADTCD31[R] B,H,W 10--0000 00000000		
0013CC _H	ADTECS0[R/W] B,H,W -----0 ---00000		ADTECS1[R/W] B,H,W -----0 ---00000		
0013D0 _H	ADTECS2[R/W] B,H,W -----0 ---00000		ADTECS3[R/W] B,H,W -----0 ---00000		
0013D4 _H	ADTECS4[R/W] B,H,W -----0 ---00000		ADTECS5[R/W] B,H,W -----0 ---00000		
0013D8 _H	ADTECS6[R/W] B,H,W -----0 ---00000		ADTECS7[R/W] B,H,W -----0 ---00000		
0013DC _H	ADTECS8[R/W] B,H,W -----0 ---00000		ADTECS9[R/W] B,H,W -----0 ---00000		
0013E0 _H	ADTECS10[R/W] B,H,W -----0 ---00000		ADTECS11[R/W] B,H,W -----0 ---00000		
0013E4 _H	ADTECS12[R/W] B,H,W -----0 ---00000		ADTECS13[R/W] B,H,W -----0 ---00000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001750 _H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W]] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754 _H	—/(RDR10/(TDR10))[R/W] B,H,W ----- ^{*3}		RDR00/(TDR00)[R/W] B,H,W -----0 00000000 ^{*1}		
001758 _H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175C _H	STMCR0[R/W] B,H,W 00000000 00000000		—/(SCSCR0/SFUR0)[R/W] B,H,W ----- ^{*3} ^{*4}		
001760 _H	—/(SCSTR30)/ (LAMSR0) [R/W] B,H,W ----- ^{*3}	—/(SCSTR20)/ (LAMCR0) [R/W] B,H,W ----- ^{*3}	—/(SCSTR10)/ (SFLR10) [R/W] B,H,W ----- ^{*3}	—/(SCSTR00)/ (SFLR00) [R/W] B,H,W ----- ^{*3}	
001764 _H	—	—/(SCSFR20) [R/W] B,H,W ----- ^{*3}	—/(SCSFR10) [R/W] B,H,W ----- ^{*3}	—/(SCSFR00) [R/W] B,H,W ----- ^{*3}	
001768 _H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W ----- ^{*3}	—/(TBYTE20)/ (LAMERT0) [R/W] B,H,W ----- ^{*3}	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W ----- ^{*3}	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
00176C _H	BGR0[R/W] H, W 00000000 00000000		—/(ISMK0) [R/W] B,H,W ----- ^{*2}	—/(ISBA0) [R/W] B,H,W ----- ^{*2}	
001770 _H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774 _H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	
001778 _H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W]] B,H,W 00000000	Multi-UART1
00177C _H	—/(RDR11/(TDR11))[R/W] B,H,W ----- ^{*3}		RDR01/(TDR01)[R/W] B,H,W -----0 00000000 ^{*1}		
001780 _H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
001784 _H	STMCR1[R/W] B,H,W 00000000 00000000		—/(SCSCR1/SFUR1)[R/W] B,H,W ----- ^{*3} ^{*4}		
001788 _H	—/(SCSTR31)/ (LAMSR1) [R/W] B,H,W ----- ^{*3}	—/(SCSTR21)/ (LAMCR1) [R/W] B,H,W ----- ^{*3}	—/(SCSTR11)/ (SFLR11) [R/W] B,H,W ----- ^{*3}	—/(SCSTR01)/ (SFLR01) [R/W] B,H,W ----- ^{*3}	
00178C _H	—	—/(SCSFR21)[R/W] B,H,W ----- ^{*3}	—/(SCSFR11) [R/W] B,H,W ----- ^{*3}	—/(SCSFR01) [R/W] B,H,W ----- ^{*3}	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B24 _H	PDUT11 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR11 [R] H,W 11111111 11111111		PPG11
001B28 _H	PCN211 [R/W] B,H,W --000000 -----110		PSDR11 [R/W] H,W 00000000 00000000		
001B2C _H	PTPC11 [R/W] H,W 00000000 00000000		—	—	
001B30 _H	PCN12 [R/W] B,H,W 00000000 000000-0		PCSR12 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG12
001B34 _H	PDUT12 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR12 [R] H,W 11111111 11111111		
001B38 _H	PCN212 [R/W] B,H,W --000000 -----110		PSDR12 [R/W] H,W 00000000 00000000		
001B3C _H	PTPC12 [R/W] H,W 00000000 00000000		—	—	
001B40 _H	PCN13 [R/W] B,H,W 00000000 000000-0		PCSR13 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG13
001B44 _H	PDUT13 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR13 [R] H,W 11111111 11111111		
001B48 _H	PCN213 [R/W] B,H,W --000000 -----110		PSDR13 [R/W] H,W 00000000 00000000		
001B4C _H	PTPC13 [R/W] H,W 00000000 00000000		—	—	
001B50 _H	PCN14 [R/W] B,H,W 00000000 000000-0		PCSR14 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG14
001B54 _H	PDUT14 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR14 [R] H,W 11111111 11111111		
001B58 _H	PCN214 [R/W] B,H,W --000000 -----110		PSDR14 [R/W] H,W 00000000 00000000		
001B5C _H	PTPC14 [R/W] H,W 00000000 00000000		—	—	
001B60 _H	PCN15 [R/W] B,H,W 00000000 000000-0		PCSR15 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG15
001B64 _H	PDUT15 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR15 [R] H,W 11111111 11111111		
001B68 _H	PCN215 [R/W] B,H,W --000000 -----110		PSDR15 [R/W] H,W 00000000 00000000		
001B6C _H	PTPC15 [R/W] H,W 00000000 00000000		—	—	
001B70 _H	PCN16 [R/W] B,H,W 00000000 000000-0		PCSR16 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG16
001B74 _H	PDUT16 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR16 [R] H,W 11111111 11111111		

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29* ¹
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)	47	2F	ICR31	340 _H	000FFF40 _H	31* ¹ , * ⁴
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/7/9/10/11/12/13/14/15/16/ 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	33C _H	000FFF3C _H	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334 _H	000FFF34 _H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5	51	33	ICR35	330 _H	000FFF30 _H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching/measurement)	52	34	ICR36	32C _H	000FFF2C _H	36* ¹
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching/measurement)	53	35	ICR37	328 _H	000FFF28 _H	37
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching/measurement)						
Multi-function serial interface ch.11 (reception completed)	54	36	ICR38	324 _H	000FFF24 _H	38* ¹
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)						
WG dead timer underflow 0/1/2	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer reload 0/1/2						
WG DTTI 0						
32-bit ICU4 (fetching/measurement)	56	38	ICR40	31C _H	000FFF1C _H	40
Multi-function serial interface ch.11 (transmission completed)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31/40/41	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44/45	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 6/7/16/17/26/27/36/37/46/47	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/9/18/19/28/29/38/39	44	2C	ICR28	34C _H	000FFF4C _H	28* ³

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
32-bit ICU5 (fetching/measurement)	57	39	ICR41	318 _H	000FFF18 _H	41
A/D converter						
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47						
32-bit OCU 6/7/10/11 (match)						
32-bit OCU 8/9 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
Base timer 0 IRQ0	59	3B	ICR43	310 _H	000FFF10 _H	43
Base timer 0 IRQ1						
Base timer 1 IRQ0	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 1 IRQ1						
-						
-						
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	61	3D	ICR45	308 _H	000FFF08 _H	45
Delay interrupt	62	3E	ICR46	304 _H	000FFF04 _H	-
System reserved (Used for REALOS)	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFEFC _H	-
Used with the INT instruction	66	42	-	2F4 _H	000FFEFC _H	-
			-			-
	255	FF		000 _H	000FFC00 _H	

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

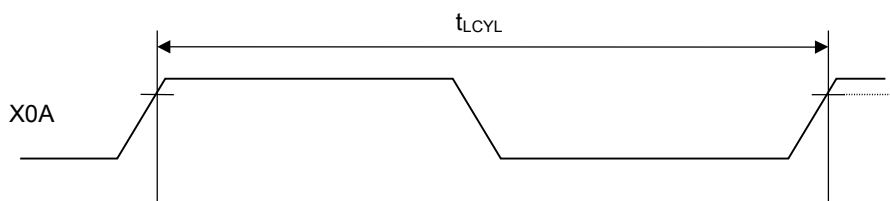
*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

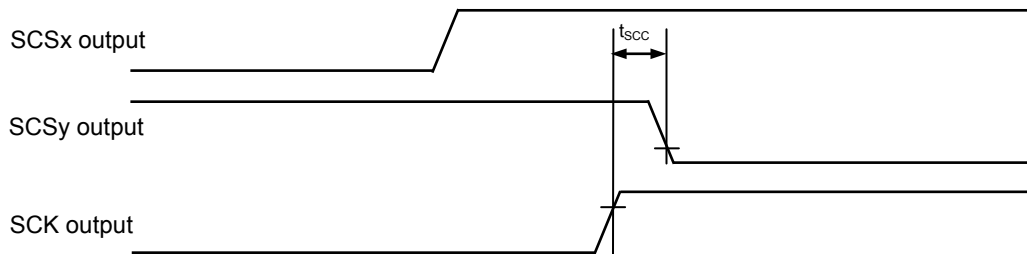
(1-2) Sub clock timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F _{CL}	X0A, X1A	-	-	32.7 68	-	kHz	
Source oscillation clock cycle time	t _{LCYL}	X0A, X1A		-	30.5 2	-	μs	

· X0A,X1A clock timing





When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-7) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,

When Serial chip select is used : SCSCR:CSEN=1,

Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,

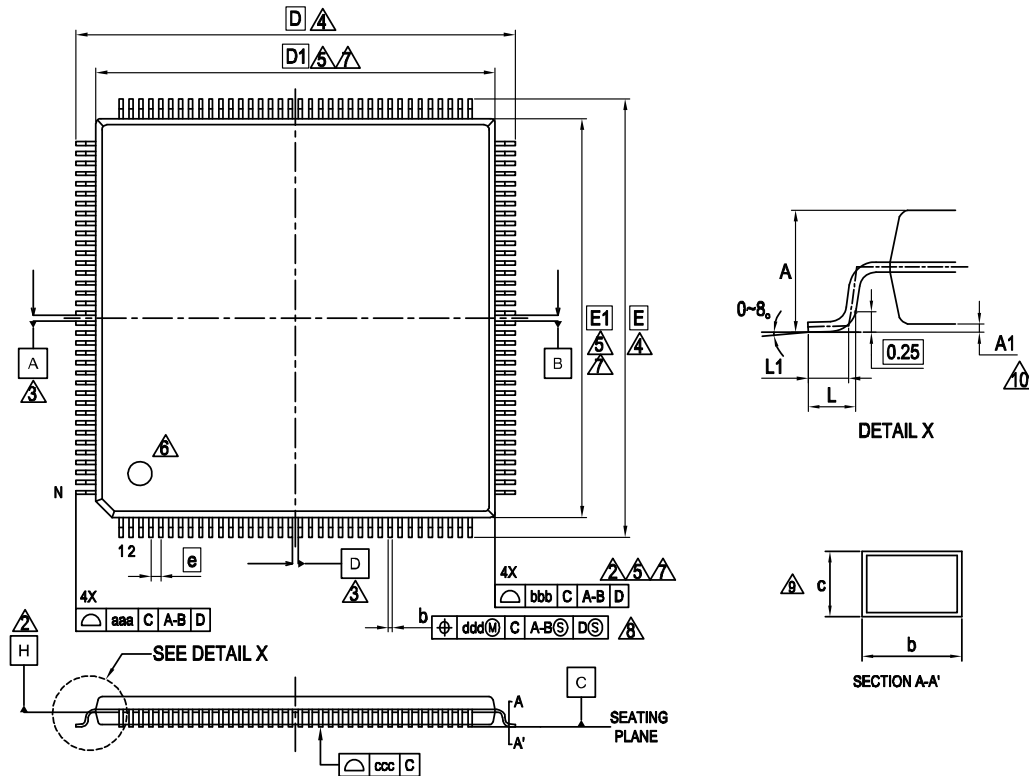
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t _{CSSI}	SCK1, SCK2, SCK5 to SCK11 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CSSU} -50 *1	t _{CSSU} +0 *1	ns	Internal shift clock mode output pin : C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSSU} -50 *1	t _{CSSU} +30 0 *1	ns	
SCK↑→SCS↓ hold time	t _{CSHI}	SCK1 to SCK2, SCK5 to SCK11 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSHD} -10 *2	t _{CSHD} +50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSHD} -300 *2	t _{CSHD} +50 *2	ns	
SCS deselect time	t _{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSDS} -50 *3	t _{CSDS} +50 *3	ns	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWDCMC	Yes	ON	ON	LQI • 100 pin, Plastic
MB91F526FJDCMC		OFF	ON	
MB91F525FWDCMC		ON	ON	
MB91F525FJDCMC		OFF	ON	
MB91F524FWDCMC		ON	ON	
MB91F524FJDCMC		OFF	ON	
MB91F523FWDCMC		ON	ON	
MB91F523FJDCMC		OFF	ON	
MB91F522FWDCMC		ON	ON	
MB91F522FJDCMC		OFF	ON	
MB91F526FSDCMC	None	ON	ON	
MB91F526FHDPMC		OFF	ON	
MB91F525FSDCMC		ON	ON	
MB91F525FHDPMC		OFF	ON	
MB91F524FSDCMC		ON	ON	
MB91F524FHDPMC		OFF	ON	
MB91F523FSDCMC		ON	ON	
MB91F523FHDPMC		OFF	ON	
MB91F522FSDCMC		ON	ON	
MB91F522FHDPMC		OFF	ON	
MB91F526DWDPMC	Yes	ON	ON	LQH • 80 pin, Plastic
MB91F526DJDCMC		OFF	ON	
MB91F525DWDPMC		ON	ON	
MB91F525DJDCMC		OFF	ON	
MB91F524DWDPMC		ON	ON	
MB91F524DJDCMC		OFF	ON	
MB91F523DWDPMC		ON	ON	
MB91F523DJDCMC		OFF	ON	
MB91F522DWDPMC		ON	ON	
MB91F522DJDCMC		OFF	ON	
MB91F526DSDPMC	None	ON	ON	
MB91F526DHDPMC		OFF	ON	
MB91F525DSDPMC		ON	ON	
MB91F525DHDPMC		OFF	ON	
MB91F524DSDPMC		ON	ON	
MB91F524DHDPMC		OFF	ON	
MB91F523DSDPMC		ON	ON	
MB91F523DHDPMC		OFF	ON	
MB91F522DSDPMC		ON	ON	
MB91F522DHDPMC		OFF	ON	

LQN144 , 144 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQN144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.145	0.18	0.215
c	0.115	—	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.40 BSC.		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.07
N	144		

NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Page	Section	Change Results																																																																																																																																																																																																																																																																																																					
34, 35	■PIN Description	A List of "Pin Description" modified.																																																																																																																																																																																																																																																																																																					
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		<table><tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr><tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr><tr><td>-</td><td>-</td><td>-</td><td>113</td><td>133</td><td>161</td><td>P002</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D18</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SCK1_0</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>TIOB0_1</td></tr><tr><td>-</td><td>76</td><td>96</td><td>114</td><td>134</td><td>162</td><td>P003</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D19</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SIN2_0</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>TIOB1_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>INT3_0</td></tr><tr><td>-</td><td>-</td><td>-</td><td>-</td><td>135</td><td>163</td><td>P004</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D20</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SOT2_0</td></tr><tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>164</td><td>P164</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>PPG32_1</td></tr><tr><td>61</td><td>77</td><td>97</td><td>115</td><td>136</td><td>165</td><td>P005</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D21</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SCK2_0</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>ADTG0_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>INT7_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>(RX2(64))</td></tr><tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>166</td><td>P165</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>PPG33_1</td></tr><tr><td>62</td><td>78</td><td>98</td><td>116</td><td>137</td><td>167</td><td>P006</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D22</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SCS2_0</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>ADTG1_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>INT2_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>(TX2(64))</td></tr><tr><td>-</td><td>-</td><td>-</td><td>117</td><td>138</td><td>168</td><td>P007</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D23</td></tr><tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>169</td><td>P166</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>PPG34_1</td></tr><tr><td>-</td><td>-</td><td>-</td><td>118</td><td>139</td><td>170</td><td>P010</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D24</td></tr><tr><td>63</td><td>79</td><td>99</td><td>119</td><td>140</td><td>171</td><td>P011</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>WOT</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>D25</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SOT2_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>TIOA0_0</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>INT3_1</td></tr></table>	Pin no.						Pin Name	64	80	100	120	144	176	-	-	-	113	133	161	P002							D18							SCK1_0							TIOB0_1	-	76	96	114	134	162	P003							D19							SIN2_0							TIOB1_1							INT3_0	-	-	-	-	135	163	P004							D20							SOT2_0	-	-	-	-	-	164	P164							PPG32_1	61	77	97	115	136	165	P005							D21							SCK2_0							ADTG0_1							INT7_1							(RX2(64))	-	-	-	-	-	166	P165							PPG33_1	62	78	98	116	137	167	P006							D22							SCS2_0							ADTG1_1							INT2_1							(TX2(64))	-	-	-	117	138	168	P007							D23	-	-	-	-	-	169	P166							PPG34_1	-	-	-	118	139	170	P010							D24	63	79	99	119	140	171	P011							WOT							D25							SOT2_1							TIOA0_0							INT3_1
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Page	Section	Change Results																				
125	■Interrupt Vector Table	The following sentence deleted from Interrupt vector 80pins. (Error) *5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.																				
129	■Interrupt Vector Table	The interrupt factor in Interrupt vector 100pin modified as follows: (Error) <table><tr><td>Base timer 0 IRQ0</td><td rowspan="2">60</td><td rowspan="2">3 C</td><td rowspan="2">ICR 44</td><td rowspan="2">30C_H</td><td rowspan="2">000F FF0C_H</td><td rowspan="2">44</td></tr><tr><td>Base timer 0 IRQ1</td></tr></table> (Correct) <table><tr><td>-</td><td rowspan="2">60</td><td rowspan="2">3 C</td><td rowspan="2">ICR 44</td><td rowspan="2">30C_H</td><td rowspan="2">000F FF0C_H</td><td rowspan="2">44</td></tr><tr><td>-</td></tr></table>	Base timer 0 IRQ0	60	3 C	ICR 44	30C _H	000F FF0C _H	44	Base timer 0 IRQ1	-	60	3 C	ICR 44	30C _H	000F FF0C _H	44	-				
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129	■Interrupt Vector Table	The interrupt factor in Interrupt vector 100pin modified as follows: (Error) <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08_H</td><td rowspan="4">45 *5</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>-</td></tr><tr><td>-</td></tr></table> (Correct) <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08_H</td><td rowspan="4">45</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>-</td></tr><tr><td>-</td></tr></table>	Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45 *5	Base timer 1 IRQ1	-	-	Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45	Base timer 1 IRQ1	-	-
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