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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525fscpmc-gs-ere2

1. Product Lineup

Product lineup comparison 64 pins

	MB91F522B	MB91F523B	MB91F524B	MB91F525B	MB91F526B
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB	(64+8)KB	(96+8)KB	(128+8)KB	
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	None				
Free-run Timer	16bit×3ch, 32bit×1ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×21ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×13ch (1unit), 12bit×13ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	8ch ^{*1}				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	44 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
NMI request function	Yes				
Operation guaranteed temperature (T _A)	-40°C to +125°C				
Power supply	2.7V to 5.5V ^{*2}				
Package	LQD064				

*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
23	28	34	40	48	59	P062	-	B	General-purpose I/O port
						SCS10_1	-		Serial chip select 10 I/O (1)
						SCS40_0	-		Serial chip select 40 I/O (0)
						AN40	-		ADC analog 40 input
						PPG4_1	-		PPG ch.4 output (1)
						FRCK0_0	-		Free-run timer 0 clock input (0)
						TOT7_1	-		Reload timer ch.7 output (1)
						ZIN1_1	-		U/D counter ch.1 ZIN input (1)
-	29	35	41	49	60	P063	-	B	General-purpose I/O port
						SCS41_0	-		Serial chip select 41 output (0)
						AN39	-		ADC analog 39 input
						PPG5_1	-		PPG ch.5 output (1)
						FRCK1_0	-		Free-run timer 1 clock input (0)
						BIN1_1	-		U/D counter ch.1 BIN input (1)
-	-	-	-	-	61	P183	-	A	General-purpose I/O port
						PPG43_0	-		PPG ch.43 output (0)
24	30	36	42	50	62	P064	-	B	General-purpose I/O port
						SCS42_0	-		Serial chip select 42 output (0)
						AN38	-		ADC analog 38 input
						FRCK2_0	-		Free-run timer 2 clock input (0)
						AIN1_1	-		U/D counter ch.1 AIN input (1)
						PPG43_1	-		PPG ch.43 output (1)
-	-	37	43	51	63	P065	-	A	General-purpose I/O port
						SCS43_0	-		Serial chip select 43 output (0)
						FRCK3_0	-		Free-run timer 3 clock input (0)
						ZIN0_1	-		U/D counter ch.0 ZIN input (1)
						PPG44_1	-		PPG ch.44 output (1)
-	-	-	-	-	64	P184	-	A	General-purpose I/O port
						PPG44_0	-		PPG ch.44 output (0)
-	-	-	-	-	65	P185	-	A	General-purpose I/O port
						PPG45_0	-		PPG ch.45 output (0)
25	31	38	44	52	66	P066	-	B	General-purpose I/O port
						SOT4_2	-		Multi-function serial ch.4 serial data output (2)
						SCS3_0	-		Serial chip select 3 I/O (0)
						AN37	-		ADC analog 37 input
						FRCK4_0	-		Free-run timer 4 clock input (0)
						BIN0_1	-		U/D counter ch.0 BIN input (1)
-	32	39	45	53	67	P067	-	B	General-purpose I/O port
						AN36	-		ADC analog 36 input
						FRCK5_0	-		Free-run timer 5 clock input (0)
						AIN0_1	-		U/D counter ch.0 AIN input (1)

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

■ Notes When Writing Data in a Register Having the Status Flag

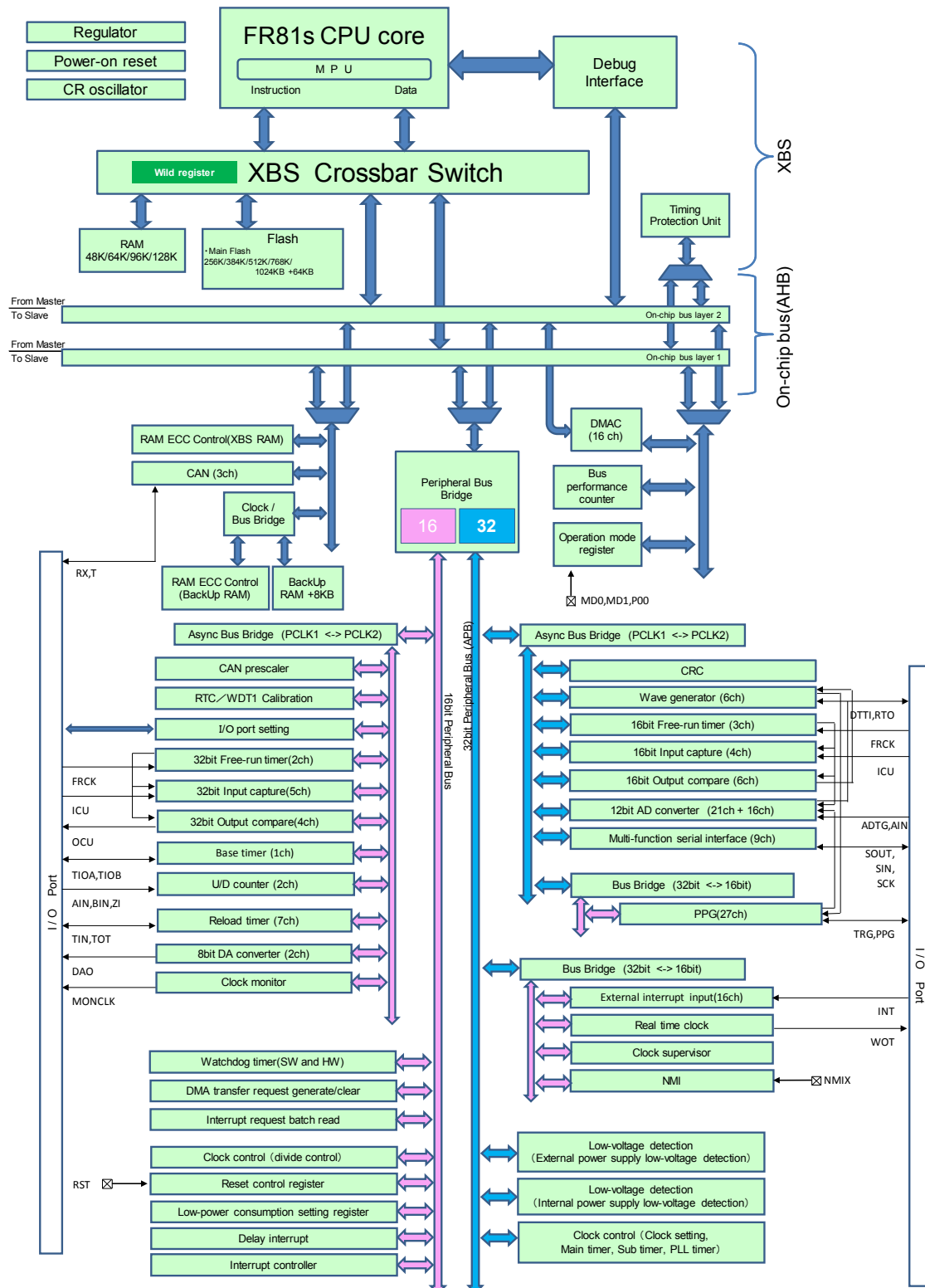
When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

Note: These points can be ignored because the bit instructions are already taken the points into consideration.

MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D



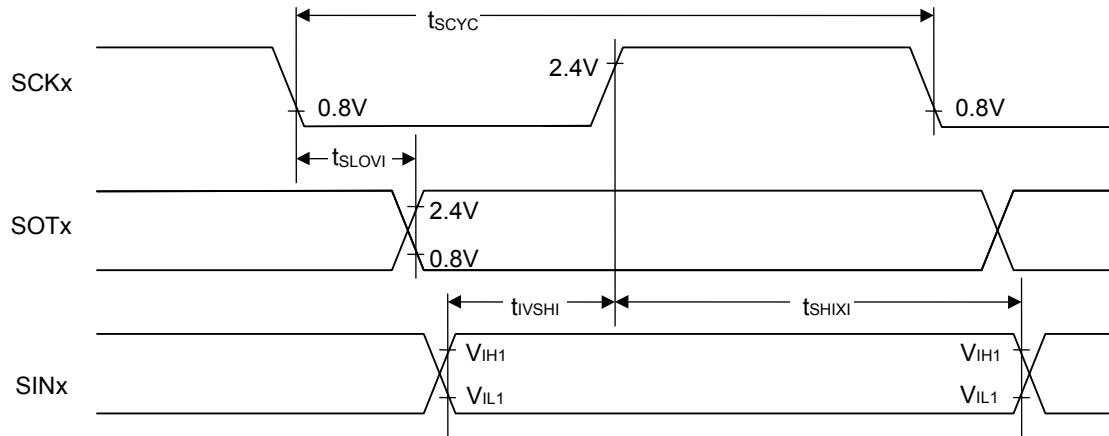
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0001F8 _H	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXX		Reload Timer 6
0001FC _H	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000		
000200 _H to 000238 _H	—	—	—	—	Reserved
00023C _H	DACR0 [R/W] B,H,W -----0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -----0	DADR1 [R/W] B,H,W XXXXXXXX	DA Converter
000240 _H	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 3 32-bit FRT
000244 _H	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000248 _H	TCCSH3 [R/W] B,H,W 0-----00	TCCSL3 [R/W] B,H,W -1-00000	—	—	
00024C _H	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 4 32-bit FRT
000250 _H	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000254 _H	TCCSH4 [R/W] B,H,W 0-----00	TCCSL4 [R/W] B,H,W -1-00000	—	—	
000258 _H to 0002C0 _H	—	—	—	—	Reserved
0002C4 _H to 0002FC _H	—	—	—	—	Reserved
000300 _H to 00030C _H	—	—	—	—	Reserved
000310 _H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314 _H	—	—	—	—	
000318 _H	—				
00031C _H	—	—	—		
000320 _H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324 _H	—	—	DPVSR [R/W] H ----- 00000--0		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000710 _H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter
000714 _H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718 _H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
00071C _H	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720 _H to 0007F8 _H	—	—	—	—	Reserved
0007FC _H	BMODR [R] B, H, W XXXXXXXX	—	—	—	Mode Register
000800 _H to 00083C _H	—	—	—	—	Reserved [S]
000840 _H	FCTL R [R/W] H -0--1000 0--0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]
000844 _H to 000854 _H	—	—	—	—	Reserved [S]
000858 _H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]
00085C _H to 00087C _H	—	—	—	—	Reserved [S]
000880 _H	WRAR00 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000884 _H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888 _H	WRAR01 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00088C _H	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890 _H	WRAR02 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000894 _H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898 _H	WRAR03 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00089C _H	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

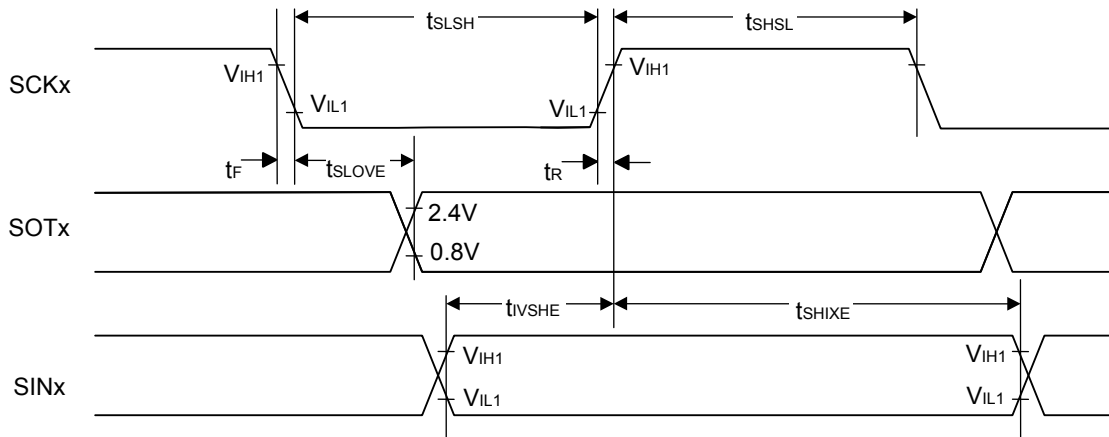
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000CA0 _H	DCCR10 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
000CA4 _H	DCSR10 [R/W] H 0----- ----000		DTCR10 [R/W] H 00000000 00000000		
000CA8 _H	DSAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CAC _H	DDAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CB0 _H	DCCR11 [R/W] W 0----000 --00--00 00000000 0-000000				
000CB4 _H	DCSR11 [R/W] H 0----- ----000		DTCR11 [R/W] H 00000000 00000000		
000CB8 _H	DSAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CBC _H	DDAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CC0 _H	DCCR12 [R/W] W 0----000 --00--00 00000000 0-000000				
000CC4 _H	DCSR12 [R/W] H 0----- ----000		DTCR12 [R/W] H 00000000 00000000		
000CC8 _H	DSAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CCC _H	DDAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CD0 _H	DCCR13 [R/W] W 0----000 --00--00 00000000 0-000000				
000CD4 _H	DCSR13 [R/W] H 0----- ----000		DTCR13 [R/W] H 00000000 00000000		
000CD8 _H	DSAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CDC _H	DDAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CE0 _H	DCCR14 [R/W] W 0----000 --00--00 00000000 0-000000				
000CE4 _H	DCSR14 [R/W] H 0----- ----000		DTCR14 [R/W] H 00000000 00000000		
000CE8 _H	DSAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CEC _H	DDAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E3C _H	—	—	—	—	Reserved
000E40 _H	PDDR00 [R] B,H,W XXXXXXXXXX	PDDR01 [R] B,H,W XXXXXXXXXX	PDDR02 [R] B,H,W XXXXXXXXXX	PDDR03 [R] B,H,W XXXXXXXXXX	Port Direct Read Register
000E44 _H	PDDR04 [R] B,H,W XXXXXXXXXX	PDDR05 [R] B,H,W XXXXXXXXXX	PDDR06 [R] B,H,W XXXXXXXXXX	PDDR07 [R] B,H,W XXXXXXXXXX	
000E48 _H	PDDR08 [R] B,H,W XXXXXXXXXX	PDDR09 [R] B,H,W XXXXXXXXXX	PDDR10 [R] B,H,W XXXXXXXXXX	PDDR11 [R] B,H,W XXXXXXXXXX	
000E4C _H	PDDR12 [R] B,H,W XXXXXXXXXX	PDDR13 [R] B,H,W -XXXXXXXX	PDDR14 [R] B,H,W ---XXX--	PDDR15 [R] B,H,W --XXXXXX	
000E50 _H	—	—	—	—	
000E54 _H	—	—	—	—	
000E58 _H	PDDR16 [R] B,H,W XXXXXXXXXX	PDDR17 [R] B,H,W XXXXXXXXXX	PDDR18 [R] B,H,W XXXXXXXXXX	PDDR19 [R] B,H,W XXXXXXXXXX	
000E5C _H	—	—	—	—	Reserved
000E60 _H	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ---0000	EPFR03 [R/W] B,H,W --000-0	Extended Port Function Register
000E64 _H	EPFR04 [R/W] B,H,W ---00-0	EPFR05 [R/W] B,H,W ---0000	EPFR06 [R/W] B,H,W ---000-	EPFR07 [R/W] B,H,W --00000	
000E68 _H	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W ----00-	EPFR10 [R/W] B,H,W ---0000	EPFR11 [R/W] B,H,W ----0000	
000E6C _H	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W -----00	EPFR14 [R/W] B,H,W -----00	EPFR15 [R/W] B,H,W -----000	
000E70 _H	—	—	—	—	
000E74 _H	—	—	—	—	
000E78 _H	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0----	
000E7C _H	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
000E80 _H	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	
000E84 _H	EPFR36 [R/W] B,H,W ----000-	—	—	—	
000E88 _H	—	—	EPFR42 [R/W] B,H,W -----00	EPFR43 [R/W] B,H,W 0--0000-	
000E8C _H	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
000E90 _H	—	—	—	—	

• Internal shift clock mode



• External shift clock mode



(4-1-6) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,

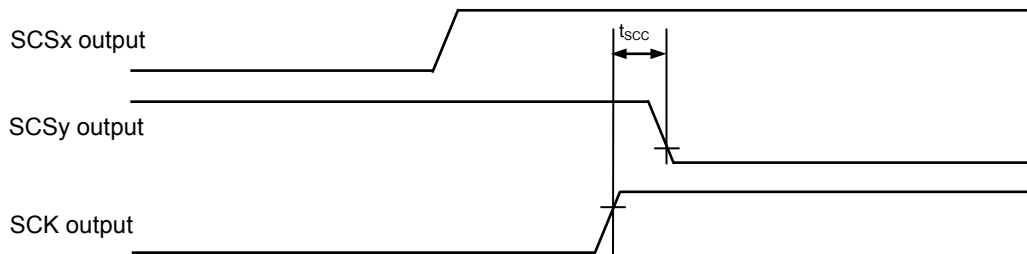
When Serial chip select is used : SCSCR:CSSEN=1,

Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,

Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t _{CSSI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t _{CSSU} -50 *1	t _{CSSU} +0 *1	ns	Internal shift clock mode output pin : C _L =50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSSU} -50 *1	t _{CSSU} +300 *1	ns	
SCK↓→SCS↑ hold time	t _{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSHD} -10 *2	t _{CSHD} +50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t _{CSHD} -300 *2	t _{CSHD} +50 *2	ns	
SCS deselect time	t _{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t _{CSDS} -50 *3	t _{CSDS} +50 *3	ns	



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMP1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYBPMP1			OFF	
MB91F526KJBPM1		OFF	ON	
MB91F526KLBPM1			OFF	
MB91F525KWBPMP1		ON	ON	
MB91F525KYBPMP1			OFF	
MB91F525KJBPM1		OFF	ON	
MB91F525KLBPM1			OFF	
MB91F524KWBPMP1		ON	ON	
MB91F524KYBPMP1			OFF	
MB91F524KJBPM1		OFF	ON	
MB91F524KLBPM1			OFF	
MB91F523KWBPMP1		ON	ON	
MB91F523KYBPMP1			OFF	
MB91F523KJBPM1		OFF	ON	
MB91F523KLBPM1			OFF	
MB91F522KWBPMP1		ON	ON	
MB91F522KYBPMP1			OFF	
MB91F522KJBPM1		OFF	ON	
MB91F522KLBPM1			OFF	
MB91F526KSBPM1	None	ON	ON	
MB91F526KUBPM1			OFF	
MB91F526KHBPM1		OFF	ON	
MB91F526KKBPM1			OFF	
MB91F525KSBPM1		ON	ON	
MB91F525KUBPM1			OFF	
MB91F525KHBPM1		OFF	ON	
MB91F525KKBPM1			OFF	
MB91F524KSBPM1		ON	ON	
MB91F524KUBPM1			OFF	
MB91F524KHBPM1		OFF	ON	
MB91F524KKBPM1			OFF	
MB91F523KSBPM1		ON	ON	
MB91F523KUBPM1			OFF	
MB91F523KHBPM1		OFF	ON	
MB91F523KKBPM1			OFF	
MB91F522KSBPM1		ON	ON	
MB91F522KUBPM1			OFF	
MB91F522KHBPM1		OFF	ON	
MB91F522KKBPM1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526JWBPMC	Yes	ON	ON	LQM • 120 pin, Plastic
MB91F526JYBPMC			OFF	
MB91F526JJBPMC		OFF	ON	
MB91F526JLBPMC			OFF	
MB91F525JWBPMC		ON	ON	
MB91F525JYBPMC			OFF	
MB91F525JJBPMC		OFF	ON	
MB91F525JLBPMC			OFF	
MB91F524JWBPMC		ON	ON	
MB91F524JYBPMC			OFF	
MB91F524JJBPMC		OFF	ON	
MB91F524JLBPMC			OFF	
MB91F523JWBPMC		ON	ON	
MB91F523JYBPMC			OFF	
MB91F523JJBPMC		OFF	ON	
MB91F523JLBPMC			OFF	
MB91F522JWBPMC		ON	ON	
MB91F522JYBPMC			OFF	
MB91F522JJBPMC		OFF	ON	
MB91F522JLBPMC			OFF	
MB91F526JSBPMC	None	ON	ON	
MB91F526JUBPMC			OFF	
MB91F526JHBPMC		OFF	ON	
MB91F526JKBPMC			OFF	
MB91F525JSBPMC		ON	ON	
MB91F525JUBPMC			OFF	
MB91F525JHBPMC		OFF	ON	
MB91F525JKBPMC			OFF	
MB91F524JSBPMC		ON	ON	
MB91F524JUBPMC			OFF	
MB91F524JHBPMC		OFF	ON	
MB91F524JKBPMC			OFF	
MB91F523JSBPMC		ON	ON	
MB91F523JUBPMC			OFF	
MB91F523JHBPMC		OFF	ON	
MB91F523JKBPMC			OFF	
MB91F522JSBPMC		ON	ON	
MB91F522JUBPMC			OFF	
MB91F522JHBPMC		OFF	ON	
MB91F522JKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526DWBPMC	Yes	ON	ON	LQH • 80 pin, Plastic
MB91F526DYBPMC			OFF	
MB91F526DJBPMC		OFF	ON	
MB91F526DLBPMC			OFF	
MB91F525DWBPMC		ON	ON	
MB91F525DYBPMC			OFF	
MB91F525DJBPMC		OFF	ON	
MB91F525DLBPMC			OFF	
MB91F524DWBPMC		ON	ON	
MB91F524DYBPMC			OFF	
MB91F524DJBPMC		OFF	ON	
MB91F524DLBPMC			OFF	
MB91F523DWBPMC		ON	ON	
MB91F523DYBPMC			OFF	
MB91F523DJBPMC		OFF	ON	
MB91F523DLBPMC			OFF	
MB91F522DWBPMC		ON	ON	
MB91F522DYBPMC			OFF	
MB91F522DJBPMC		OFF	ON	
MB91F522DLBPMC			OFF	
MB91F526DSBPMC	None	ON	ON	
MB91F526DUBPMC			OFF	
MB91F526DHBPMC		OFF	ON	
MB91F526DKBPMC			OFF	
MB91F525DSBPMC		ON	ON	
MB91F525DUBPMC			OFF	
MB91F525DHBPMC		OFF	ON	
MB91F525DKBPMC			OFF	
MB91F524DSBPMC		ON	ON	
MB91F524DUBPMC			OFF	
MB91F524DHBPMC		OFF	ON	
MB91F524DKBPMC			OFF	
MB91F523DSBPMC		ON	ON	
MB91F523DUBPMC			OFF	
MB91F523DHBPMC		OFF	ON	
MB91F523DKBPMC			OFF	
MB91F522DSBPMC		ON	ON	
MB91F522DUBPMC			OFF	
MB91F522DHBPMC		OFF	ON	
MB91F522DKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package ⁷²
MB91F526KWCPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYCPMC1			OFF	
MB91F526KJCPMC1		OFF	ON	
MB91F526KLCPMC1			OFF	
MB91F525KWCPMC1		ON	ON	
MB91F525KYCPMC1			OFF	
MB91F525KJCPMC1		OFF	ON	
MB91F525KLCPMC1			OFF	
MB91F524KWCPMC1		ON	ON	
MB91F524KYCPMC1			OFF	
MB91F524KJCPMC1		OFF	ON	
MB91F524KLCPMC1			OFF	
MB91F523KWCPMC1		ON	ON	
MB91F523KYCPMC1			OFF	
MB91F523KJCPMC1		OFF	ON	
MB91F523KLCPMC1			OFF	
MB91F522KWCPMC1		ON	ON	
MB91F522KYCPMC1			OFF	
MB91F522KJCPMC1		OFF	ON	
MB91F522KLCPMC1			OFF	
MB91F526KSCPMC1	None	ON	ON	
MB91F526KUCPMC1			OFF	
MB91F526KHCPMC1		OFF	ON	
MB91F526KKCPMC1			OFF	
MB91F525KSCPMC1		ON	ON	
MB91F525KUCPMC1			OFF	
MB91F525KHCPMC1		OFF	ON	
MB91F525KKCPMC1			OFF	
MB91F524KSCPMC1		ON	ON	
MB91F524KUCPMC1			OFF	
MB91F524KHCPMC1		OFF	ON	
MB91F524KKCPMC1			OFF	
MB91F523KSCPMC1		ON	ON	
MB91F523KUCPMC1			OFF	
MB91F523KHCPMC1		OFF	ON	
MB91F523KKCPMC1			OFF	
MB91F522KSCPMC1		ON	ON	
MB91F522KUCPMC1			OFF	
MB91F522KHCPMC1		OFF	ON	
MB91F522KKCPMC1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWDPMC	Yes	ON	ON	LQI • 100 pin, Plastic
MB91F526FJDPMC		OFF	ON	
MB91F525FWDPMC		ON	ON	
MB91F525FJDPMC		OFF	ON	
MB91F524FWDPMC		ON	ON	
MB91F524FJDPMC		OFF	ON	
MB91F523FWDPMC		ON	ON	
MB91F523FJDPMC		OFF	ON	
MB91F522FWDPMC		ON	ON	
MB91F522FJDPMC		OFF	ON	
MB91F526FSDPMC	None	ON	ON	
MB91F526FHDPMC		OFF	ON	
MB91F525FSDPMC		ON	ON	
MB91F525FHDPMC		OFF	ON	
MB91F524FSDPMC		ON	ON	
MB91F524FHDPMC		OFF	ON	
MB91F523FSDPMC		ON	ON	
MB91F523FHDPMC		OFF	ON	
MB91F522FSDPMC		ON	ON	
MB91F522FHDPMC		OFF	ON	
MB91F526DWDPMC	Yes	ON	ON	LQH • 80 pin, Plastic
MB91F526DJDP		OFF	ON	
MB91F525DWDPMC		ON	ON	
MB91F525DJDP		OFF	ON	
MB91F524DWDPMC		ON	ON	
MB91F524DJDP		OFF	ON	
MB91F523DWDPMC		ON	ON	
MB91F523DJDP		OFF	ON	
MB91F522DWDPMC		ON	ON	
MB91F522DJDP		OFF	ON	
MB91F526DSDPMC	None	ON	ON	
MB91F526DHDPMC		OFF	ON	
MB91F525DSDPMC		ON	ON	
MB91F525DHDPMC		OFF	ON	
MB91F524DSDPMC		ON	ON	
MB91F524DHDPMC		OFF	ON	
MB91F523DSDPMC		ON	ON	
MB91F523DHDPMC		OFF	ON	
MB91F522DSDPMC		ON	ON	
MB91F522DHDPMC		OFF	ON	

■ Workaround

It is necessary to satisfy the below both conditions of (1) and (2).

- (1) Interrupt levels that are used as sources for recovering from the watch mode (power off) are '31', before CPU state changes to the watch mode (power off)
- (2) Don't use NMIX pin as source for recovering from the watch mode (power off)

■ Fix Status

Will not be planned

Page	Section	Change Results																																																																																																																										
20	■PIN Description	A List of "Pin Description" modified.																																																																																																																										
		(Error)																																																																																																																										
		<table><tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr><tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr><tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">4</td><td rowspan="5">7</td><td rowspan="5">10</td><td rowspan="5">12</td><td>P025</td></tr><tr><td>WR1X</td></tr><tr><td>SOT4_1</td></tr><tr><td>PPG25_0</td></tr><tr><td>TIN2_0</td></tr><tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">13</td><td>P172</td></tr><tr><td>PPG38_1</td></tr><tr><td rowspan="5">-</td><td rowspan="5">4</td><td rowspan="5">5</td><td rowspan="5">8</td><td rowspan="5">11</td><td rowspan="5">14</td><td>P026</td></tr><tr><td>A00</td></tr><tr><td>SCK4_1</td></tr><tr><td>PPG26_0</td></tr><tr><td>TIN3_0</td></tr><tr><td rowspan="5">4</td><td rowspan="5">5</td><td rowspan="5">6</td><td rowspan="5">9</td><td rowspan="5">12</td><td rowspan="5">15</td><td>P027</td></tr><tr><td>A01</td></tr><tr><td>SCS40_1</td></tr><tr><td>PPG27_0</td></tr><tr><td>TOT0_0</td></tr><tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">16</td><td>RTO3_1</td></tr><tr><td>P173</td></tr><tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">7</td><td rowspan="5">10</td><td rowspan="5">13</td><td rowspan="5">17</td><td>PPG39_1</td></tr><tr><td>P030</td></tr><tr><td>A02</td></tr><tr><td>SCS41_1</td></tr><tr><td>PPG28_0</td></tr><tr><td rowspan="5">-</td><td rowspan="5">6</td><td rowspan="5">8</td><td rowspan="5">11</td><td rowspan="5">14</td><td rowspan="5">18</td><td>TOT1_0</td></tr><tr><td>P031</td></tr><tr><td>A03</td></tr><tr><td>SCS42_1</td></tr><tr><td>PPG29_0</td></tr><tr><td rowspan="5">5</td><td rowspan="5">7</td><td rowspan="5">9</td><td rowspan="5">12</td><td rowspan="5">15</td><td rowspan="5">19</td><td>TOT2_0</td></tr><tr><td>P032</td></tr><tr><td>A04</td></tr><tr><td>SCS43_1</td></tr><tr><td>PPG30_0</td></tr><tr><td rowspan="5">6</td><td rowspan="5">8</td><td rowspan="5">10</td><td rowspan="5">13</td><td rowspan="5">16</td><td rowspan="5">20</td><td>TOT3_0</td></tr><tr><td>RTO2_1</td></tr><tr><td>P033</td></tr><tr><td>A05</td></tr><tr><td>PPG31_0</td></tr><tr><td rowspan="3">6</td><td rowspan="3">8</td><td rowspan="3">10</td><td rowspan="3">13</td><td rowspan="3">16</td><td rowspan="3">20</td><td>ICU3_3</td></tr><tr><td>TIN4_0</td></tr><tr><td>RTO1_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SCK3_2</td></tr></table>	Pin no.						Pin Name	64	80	100	120	144	176	-	-	4	7	10	12	P025	WR1X	SOT4_1	PPG25_0	TIN2_0	-	-	-	-	-	13	P172	PPG38_1	-	4	5	8	11	14	P026	A00	SCK4_1	PPG26_0	TIN3_0	4	5	6	9	12	15	P027	A01	SCS40_1	PPG27_0	TOT0_0	-	-	-	-	-	16	RTO3_1	P173	-	-	7	10	13	17	PPG39_1	P030	A02	SCS41_1	PPG28_0	-	6	8	11	14	18	TOT1_0	P031	A03	SCS42_1	PPG29_0	5	7	9	12	15	19	TOT2_0	P032	A04	SCS43_1	PPG30_0	6	8	10	13	16	20	TOT3_0	RTO2_1	P033	A05	PPG31_0	6	8	10	13	16	20	ICU3_3	TIN4_0	RTO1_1							SCK3_2
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131	■Interrupt Vector Table	"42" is deleted as shown below from the interrupt factor in Interrupt vector 120pin. (Error) <table><tr><td>PPG2/3/12/13/22 /23/32/33/42/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000F FF58 H</td><td rowspan="2">25 *3</td></tr><tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr></table> (Correct) <table><tr><td>PPG2/3/12/13/22 /23/32/33/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000F FF58 H</td><td rowspan="2">25 *3</td></tr><tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr></table>	PPG2/3/12/13/22 /23/32/33/42/43	41	29	ICR 25	358 H	000F FF58 H	25 *3	16-bit free-run timer 2 (0 detection) / (compare clear)	PPG2/3/12/13/22 /23/32/33/43	41	29	ICR 25	358 H	000F FF58 H	25 *3	16-bit free-run timer 2 (0 detection) / (compare clear)				
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16-bit free-run timer 2 (0 detection) / (compare clear)																						
133	■Interrupt Vector Table	The interrupt factor in Interrupt vector 120pin modified as follows: (Error) <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45 *5</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>—</td></tr><tr><td>—</td></tr></table> (Correct) <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>—</td></tr><tr><td>—</td></tr></table>	Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45 *5	Base timer 1 IRQ1	—	—	Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45	Base timer 1 IRQ1	—	—
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Base timer 1 IRQ1																						
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133	■Interrupt Vector Table	The following sentence deleted from Interrupt vector 120pins. (Error) *5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.																				