Infineon Technologies - MB91F525FSCPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525fscpmc-gse1

Product lineup comparison 80 pins

	MB91F522D	MB91F523D	MB91F524D	MB91F525D	MB91F526D
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch, 32bit×2ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×27ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×16ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	9ch*1				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	56 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V *2				
Package	LQH080				

*1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	64	80	P080	-	A	General-purpose I/O port
						SCS52_0	-		Serial chip select 52 output (0)
						PPG0_0	-		PPG ch.0 output (0)
29	37	46	56	65	81	P081	-	G	General-purpose I/O port
						SOT5_0/ SDA5	-		Multi-function serial ch.5 serial data output (0)/I^{2}C bus serial data I/O
						AN0	-		ADC analog 0 input
						PPG1_0	-		PPG ch.1 output (0)
30	38	47	57	66	82	P082	-	G	General-purpose I/O port
						SIN5_0	-		Multi-function serial ch.5 serial data input (0)
						AN1	-		ADC analog 1 input
						PPG2_0	-		PPG ch.2 output (0)
-	-	-	-	67	83	P083	-	B	General-purpose I/O port
						SCS50_0	-		Serial chip select 50 I/O (0)
						AN2	-		ADC analog 2 input
						PPG3_0	-		PPG ch.3 output (0)
-	-	-	-	68	84	P084	-	B	General-purpose I/O port
						SCS51_0	-		Serial chip select 51 output (0)
						AN3	-		ADC analog 3 input
						PPG4_0	-		PPG ch.4 output (0)
-	-	-	-	69	85	P085	-	A	General-purpose I/O port
						PPG5_0	-		PPG ch.5 output (0)
-	-	48	58	70	86	P086	-	C	General-purpose I/O port
						DAO1	-		DAC analog 1 output
						PPG6_0	-		PPG ch.6 output (0)
31	39	49	59	71	87	P087	-	C	General-purpose I/O port
						DAO0	-		DAC analog 0 output
						PPG7_0	-		PPG ch.7 output (0)
						INT8_0	-		INT8 External interrupt input (0)
-	-	-	-	-	90	P190	-	A	General-purpose I/O port
						TIN0_1	-		Reload timer ch.0 event input (1)
-	-	-	-	-	91	P191	-	A	General-purpose I/O port
						TIN1_1	-		Reload timer ch.1 event input (1)
-	-	-	-	74	92	P090	-	B	General-purpose I/O port
						AN4	-		ADC analog 4 input
						ICU0_0	-		Input capture ch.0 input (0)
						TIN2_1	-		Reload timer ch.2 event input (1)
-	-	-	-	75	93	P091	-	B	General-purpose I/O port
						AN5	-		ADC analog 5 input
						PPG41_1	-		PPG ch.41 output (1)
						ICU1_0	-		Input capture ch.1 input (0)
						TIN3_1	-		Reload timer ch.3 event input (1)

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00049C$_H$	IORR12 [R/W] B,H,W -0000000	IORR13 [R/W] B,H,W -0000000	IORR14 [R/W] B,H,W -0000000	IORR15 [R/W] B,H,W -0000000	DMA request by peripheral [S]
0004A0$_H$	—	—	—	—	Reserved
0004A4$_H$	CANPRE [R/W] B,H,W ---00000	—	—	—	CAN prescaler
0004A8$_H$	—	—	CSCFG[R/W]B,H,W ---0----	CMCFG[R/W]B,H,W 00000000	Clock monitor control register
0004AC$_H$	ADERH0[R/W] B,H 11111111 11111111		ADERL0[R/W] B,H 11111111 11111111		Analog input control register 0
0004B0$_H$	—		ADERL1[R/W] B,H 11111111 11111111		Analog input control register 1
0004B4$_H$	—	—	—	—	Reserved
0004B8$_H$	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration
0004BC$_H$	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
0004C0$_H$	—	—	—	—	
0004C4$_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1 [R/W] B,H,W 11000011 01010000		
0004C8$_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
0004CC$_H$ to 00050C$_H$	—	—	—	—	Reserved
000510$_H$	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock Control [S]
000514$_H$	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518$_H$	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset Control [S]
00051C$_H$	—	—	—	—	Reserved [S]
000520$_H$	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock Control 2 [S]
000524$_H$	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528$_H$	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000954_H	TPUTCN11 [R/W] B,H,W ---00000	—	—	—	Time Protection Unit [S]
000958_H	TPUTCN12 [R/W] B,H,W ---00000	—	—	—	
$00095C_H$	TPUTCN13 [R/W] B,H,W ---00000	—	—	—	
000960_H	TPUTCN14 [R/W] B,H,W ---00000	—	—	—	
000964_H	TPUTCN15 [R/W] B,H,W ---00000	—	—	—	
000968_H	TPUTCN16 [R/W] B,H,W ---00000	—	—	—	
$00096C_H$	TPUTCN17 [R/W] B,H,W ---00000	—	—	—	
000970_H	TPUTCC0 [R] B,H,W -------- 00000000 00000000 00000000				
000974_H	TPUTCC1 [R] B,H,W -------- 00000000 00000000 00000000				
000978_H	TPUTCC2 [R] B,H,W -------- 00000000 00000000 00000000				
$00097C_H$	TPUTCC3 [R] B,H,W -------- 00000000 00000000 00000000				
000980_H	TPUTCC4 [R] B,H,W -------- 00000000 00000000 00000000				
000984_H	TPUTCC5 [R] B,H,W -------- 00000000 00000000 00000000				
000988_H	TPUTCC6 [R] B,H,W -------- 00000000 00000000 00000000				
$00098C_H$	TPUTCC7 [R] B,H,W -------- 00000000 00000000 00000000				
000990_H to $0009FC_H$	—	—	—	—	
$000A00_H$ to $000BEC_H$	—	—	—	—	Reserved
$000BF0_H$	HSCFR [R/W] B,H,W -------- ------00 00000000 00000000				OCDU
$000BF4_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001750H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754H	— /(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001758H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175CH	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W -------- -------- *3 *4		
001760H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W -------- *3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W -------- *3	— /(SCSTR10) /(SFLR10) [R/W] B,H,W -------- *3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W -------- *3	
001764H	—	— /(SCSFR20) [R/W] B,H,W -------- *3	— /(SCSFR10) [R/W] B,H,W -------- *3	— /(SCSFR00) [R/W] B,H,W -------- *3	
001768H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -------- *3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W -------- *3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -------- *3	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
00176CH	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W -------- *2	— /(ISBA0) [R/W] B,H,W -------- *2	
001770H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	
001778H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W] B,H,W 00000000	Multi-UART1
00177CH	— /(RDR11/(TDR11))[R/W] B,H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
001780H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset.
001784H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W -------- -------- *3 *4		
001788H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W -------- *3	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W -------- *3	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W -------- *3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W -------- *3	
00178CH	—	— /(SCSFR21)[R/W] B,H,W -------- *3	— /(SCSFR11) [R/W] B,H,W -------- *3	— /(SCSFR01) [R/W] B,H,W -------- *3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0020BC$_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0$_H$ to 0020FC$_H$	—				
002100$_H$	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002104$_H$	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108$_H$	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
00210C$_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110$_H$	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114$_H$	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118$_H$	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C$_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120$_H$	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124$_H$	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128$_H$	—	—	—	—	
00212C$_H$	—	—	—	—	
002130$_H$, 002134$_H$	Reserved (IF1 data mirror)				CAN1 (64msb)
002138$_H$	—	—	—	—	
00213C$_H$	—	—	—	—	
002140$_H$	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144$_H$	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148$_H$	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C$_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				RAM/ diagnosis Backup RAM
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W ------00 00001100		RAM/ diagnosis Backup RAM
003044_H	TSRCRA [R/W] B,H,W 0-------	—	—	TKCCRA [R/W] B,H,W 00----00	
003048_H to $0030FC_H$	—				Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		BUS diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114_H	—	—	BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
$00311C_H$	—	—	—	—	
003120_H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128_H to $003FFC_H$	—				Reserved
004000_H to $005FFC_H$	Backup-RAM				Backup RAM area

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt vector
64 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*6
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*6
-	24	18	ICR08	$39C_H$	$000FFF9C_H$	-*6
-	25	19	ICR09	398_H	$000FFF98_H$	-*6
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

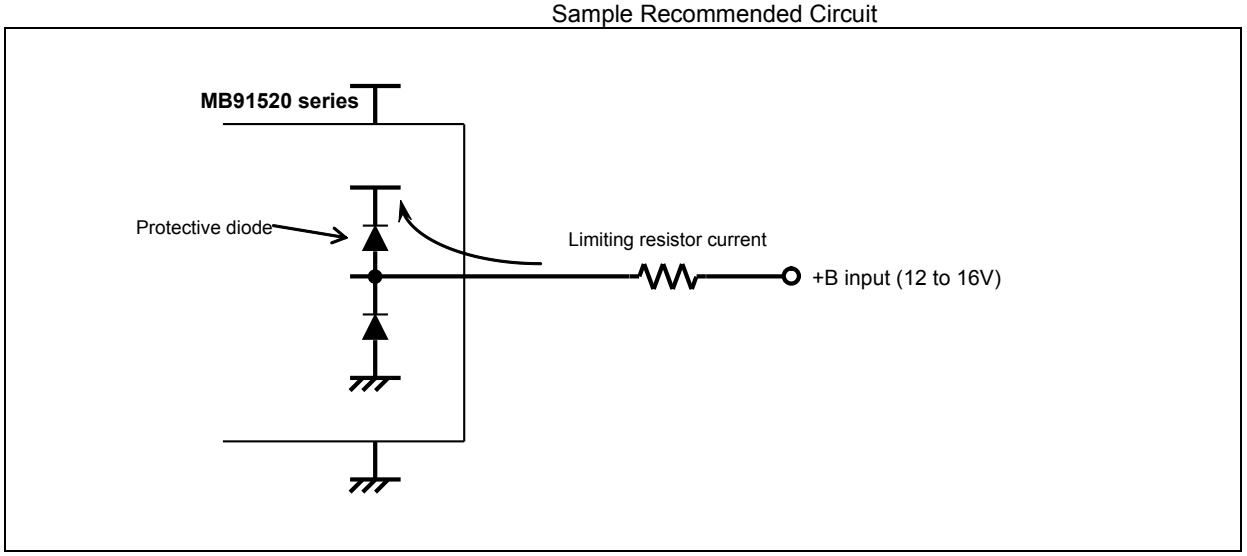
*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: REALOS is a trademark of Cypress.

*8: It is a standard when four-layer substrate is used.

*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.
*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample Recommended Circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Recommended operating conditions

(V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0V is used)
		3.0	3.6	V	Recommended operation guarantee range (When 3.3V is used)
		2.7	5.5	V	Operation guarantee range *1
Smoothing capacitor *2	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative.
The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the

AC Characteristics

(1) Main Clock Timing

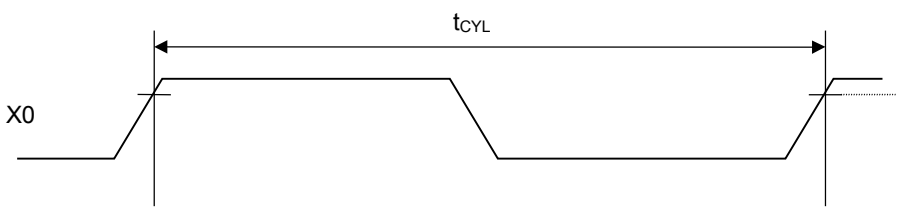
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS} =AV_{SS}=0.0V)

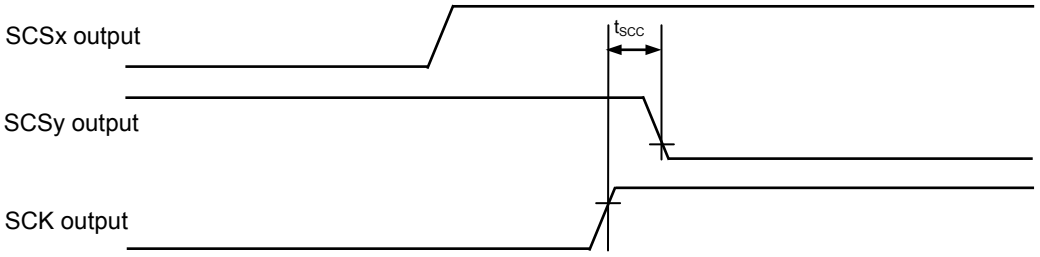
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1		-	4	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency*1	F_{CP}	-		2	-	80	MHz	CPU clock
	F_{CPP}			1		40		Peripheral bus clock
	F_{CPT}			1		40		External bus clock (When V_{CC}=5.0V is used) *2
				1		32		External bus clock (When V_{CC}=3.3V is used)
Internal operating clock cycle time*1	t_{CP}	-	-	12.5	-	500	ns	CPU clock
	t_{CPP}			25		1000		Peripheral bus clock
	t_{CPT}			25		1000		External bus clock (When V_{CC}=5.0V is used)
				31.25		1000		External bus clock (When V_{CC}=3.3V is used)
CAN PLL jitter (during lock)	t_{PJ}	-		-10	-	10	ns	F_{CP}=80MHz (4MHz□Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	-		50	100	150	kHz	

*1: The maximum / minimum value is defined when using the main clock and PLL clock.

*2: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

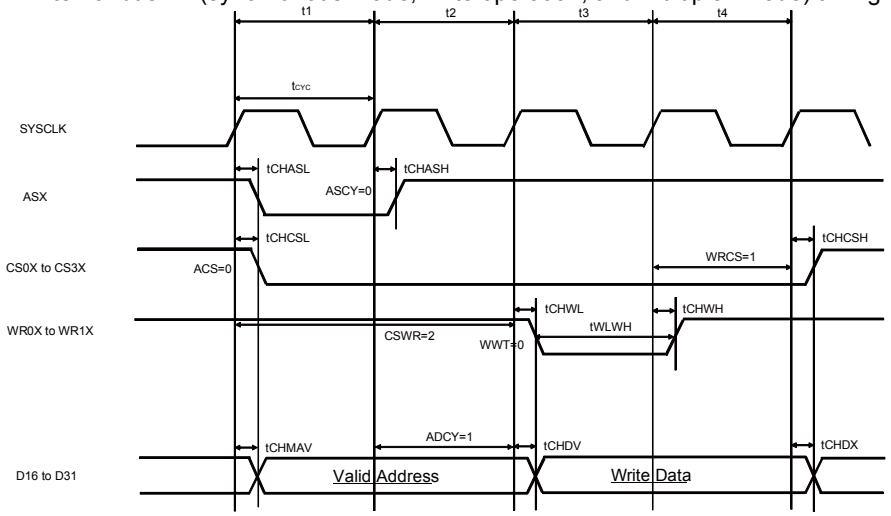
• X0,X1 clock timing



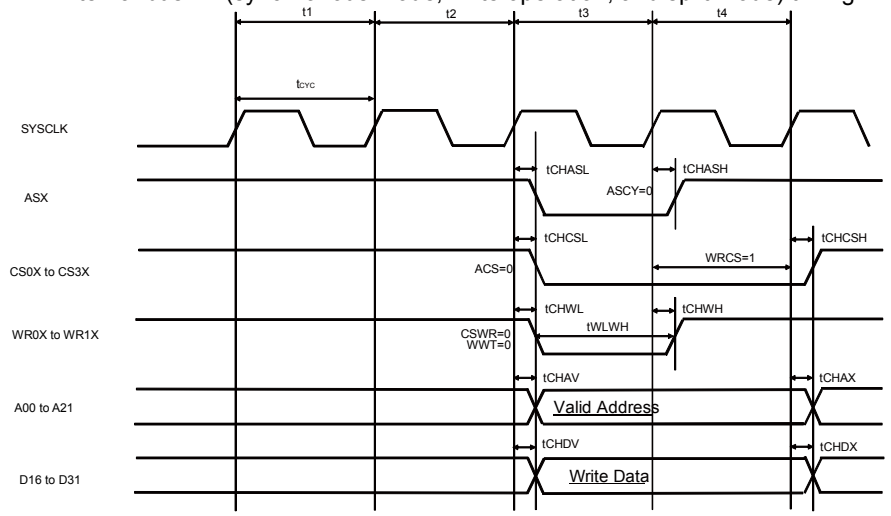


When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing



A/D Converter

(1) 12-bit A/D Converter Electrical Characteristics

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±12	LSB	
Linearity error	-	-	-	-	± 4.0	LSB	
Differential linearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN47	AVRL-11.5LSB	-	AVRL+12.5LSB	V	1LSB= (V_{FST}-V_{OT})/4094
Full-scale transition voltage	V_{FST}	AN0 to AN47	AVRH-13.5LSB	-	AVRH+10.5LSB	V	
Sampling time	t_{SMP}	-	0.7	-	-	µs	*1
Compare time	t_{CMP}	-	0.7	-	-	µs	*1
A/D conversion time	t_{CNV}	-	1.4	-	-	µs	*1
Analog port input current	I_{AIN}	AN0 to AN47	-1.0	-	+1.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN47	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH	3.0	-	5.5	V	
	AVRL	AVSS/AVRL	-	0.0	-	V	
Power supply current	I_A	AVCC*3	-	0.47	0.63	mA	Per unit T_A: +105°C
			-	0.47	0.7	mA	Per unit T_A: +125°C
	I_{AH}		-	-	2.5	µA	*2
	I_R	AVRH	-	1	1.96	mA	Per unit
	I_{RH}		-	-	1.6	µA	*2
Variation between channels	-	AN0 to AN47	-	-	4	LSB	

*1: Time for each channel.

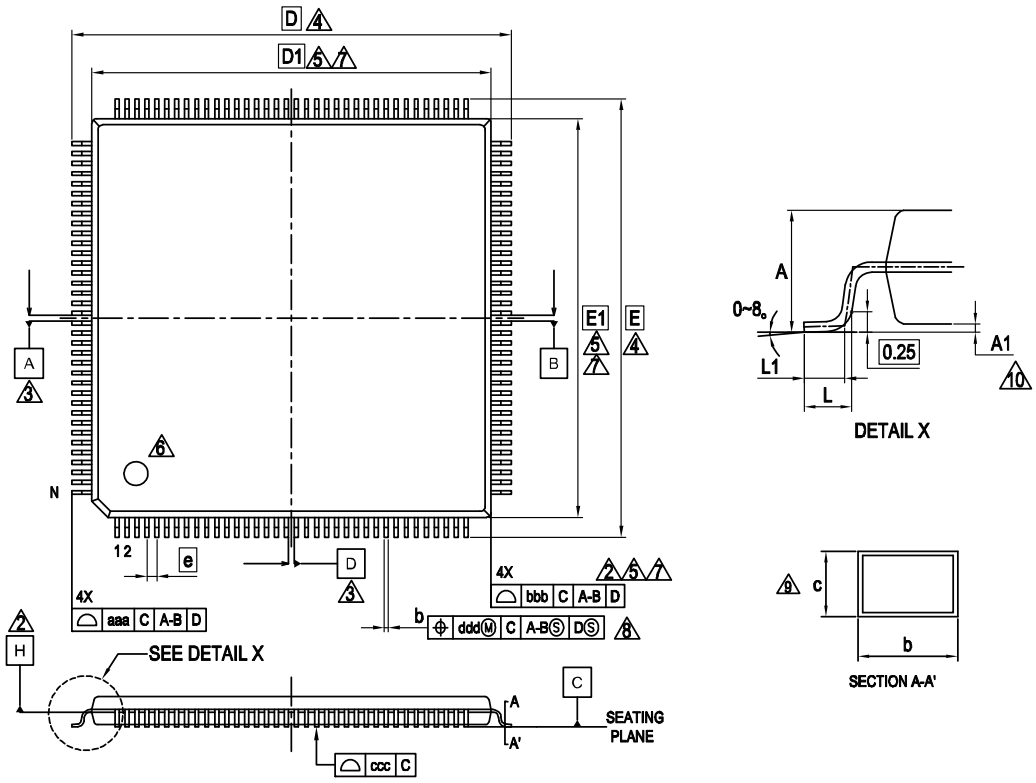
*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

*3: The power supply current described only current value on A/D converter.
The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.

(Note) Please use the clock of 0.5MHz-20MHz for the output clock of A/D converter to guarantee accuracy.

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWEPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FJEPMC		OFF	ON	
MB91F525FWEPMC		ON	ON	
MB91F525FJEPMC		OFF	ON	
MB91F524FWEPMC		ON	ON	
MB91F524FJEPMC		OFF	ON	
MB91F523FWEPMC		ON	ON	
MB91F523FJEPMC		OFF	ON	
MB91F522FWEPMC		ON	ON	
MB91F522FJEPMC		OFF	ON	
MB91F526FSEPMC	None	ON	ON	
MB91F526FHEPMC		OFF	ON	
MB91F525FSEPMC		ON	ON	
MB91F525FHEPMC		OFF	ON	
MB91F524FSEPMC		ON	ON	
MB91F524FHEPMC		OFF	ON	
MB91F523FSEPMC		ON	ON	
MB91F523FHEPMC		OFF	ON	
MB91F522FSEPMC		ON	ON	
MB91F522FHEPMC		OFF	ON	
MB91F526DWEPMC	Yes	ON	ON	LQH・80 pin, Plastic
MB91F526DJEPMC		OFF	ON	
MB91F525DWEPMC		ON	ON	
MB91F525DJEPMC		OFF	ON	
MB91F524DWEPMC		ON	ON	
MB91F524DJEPMC		OFF	ON	
MB91F523DWEPMC		ON	ON	
MB91F523DJEPMC		OFF	ON	
MB91F522DWEPMC		ON	ON	
MB91F522DJEPMC		OFF	ON	
MB91F526DSEPMC	None	ON	ON	
MB91F526DHEPMC		OFF	ON	
MB91F525DSEPMC		ON	ON	
MB91F525DHEPMC		OFF	ON	
MB91F524DSEPMC		ON	ON	
MB91F524DHEPMC		OFF	ON	
MB91F523DSEPMC		ON	ON	
MB91F523DHEPMC		OFF	ON	
MB91F522DSEPMC		ON	ON	
MB91F522DHEPMC		OFF	ON	

LQN144 , 144 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQN144		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.145	0.18	0.215
c	0.115	——	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.40 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.07
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>22, 23</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>28</td><td>P175
TRG9_1</td></tr>
<tr><td>11</td><td>13</td><td>17</td><td>20</td><td>23</td><td>29</td><td>P040
A10
PPG23_1
TOT7_0
AIN1_0
SIN0_1</td></tr>
<tr><td>12</td><td>14</td><td>18</td><td>21</td><td>24</td><td>30</td><td>P041
A11
SIN9_0
ICU9_1
BIN1_0
INT12_0</td></tr>
<tr><td>13</td><td>15</td><td>19</td><td>22</td><td>25</td><td>31</td><td>P042
A12
SOT9_0
AN47
ICU8_1
TRG0_1
ZIN1_0</td></tr>
<tr><td>-</td><td>-</td><td>20</td><td>23</td><td>26</td><td>32</td><td>P043
A13
ICU7_1
TRG1_1</td></tr>
<tr><td>-</td><td>16</td><td>21</td><td>24</td><td>27</td><td>33</td><td>P044
A14
SCS9_0
ICU6_1
TRG2_1</td></tr>
<tr><td>14</td><td>17</td><td>22</td><td>25</td><td>28</td><td>34</td><td>P045
A15
SCK9_0
AN46
ICU5_1
TRG3_1
TOT1_2</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>26</td><td>29</td><td>35</td><td>P046
A16
ICU4_1
TRG4_1</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>36</td><td>P176
TRG10_0</td></tr>
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</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>22, 23</td><td>■PIN Description</td><td>(Continued)
(Correct)
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TRG9_1</td></tr>
<tr><td>11 *1</td><td>13 *1</td><td>17 *1</td><td>20 *1</td><td>23</td><td>29</td><td>P040
A10 *2, *3, *4, *5
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TOT7_0
AIN1_0
SIN0_1</td></tr>
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AN47
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A13 *4, *5
ICU7_1
TRG1_1</td></tr>
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AN46
ICU5_1
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TOT1_2</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>26 *1</td><td>29</td><td>35</td><td>P046
A16 *5
ICU4_1
TRG4_1</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>36</td><td>P176
TRG10_0</td></tr>
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</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type L in "I/O Circuit Types" modified as follows:

(Error)
- Open-drain I/O
- Output 25mA (NOD)
- TTL input

(Correct)
- Open-drain I/O
- Output 25mA (Nch open-drain)
- TTL input</td></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type M in "I/O Circuit Types" modified as follows:

(Error)
- CMOS hysteresis input
- Pull-up resistor 50kΩ (5V cont)

(Correct)
- CMOS hysteresis input
- Pull-up resistor 50kΩ</td></tr>
<tr><td>121</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 64pins.
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>124</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 80pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45*5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
</table>

Page	Section	Change Results
143	■Electrical Characteristics 1. Absolute Maximum Ratings	The following note added. (Correct) *9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.
155	■Electrical Characteristics AC Characteristics (2) Reset Input	Added the At power-on*2 condition to the remarks in Reset input time.
156	■Electrical Characteristics AC Characteristics (3) Power-on Conditions	Deleted the Slope detection undetected specification. Added the Power ramp rate and C pin voltage at Power-on. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on.
6 to 11, 203 to 216	■Product lineup ■Ordering information	Package description modified to JEDEC description.
47	■During Power-on	The following sentence modified as fdeleted from Interrupt (Error) To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.
49, 50	■Block Diagram	The following Block diagram modified as follows: ●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B ●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D (Error) CAN (2ch). (Correct) CAN (3ch)
217 to 220	■Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxD
221 to 227	■Package Dimensions	Package Dimensions modified to JEDEC description.