Infineon Technologies - MB91F525FSCPMC-GTE1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525fscpmc-gte1

Product lineup comparison 80 pins

	MB91F522D	MB91F523D	MB91F524D	MB91F525D	MB91F526D
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch, 32bit×2ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×27ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×16ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	9ch*1				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	56 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V *2				
Package	LQH080				

*1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 144 pins

	MB91F522K	MB91F523K	MB91F524K	MB91F525K	MB91F526K
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	Yes				
DMA Transfer	16ch				
16-bit Base Timer	2ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×44ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×32ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch*1				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	120 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V *2				
Package	LQS144, LQN144				

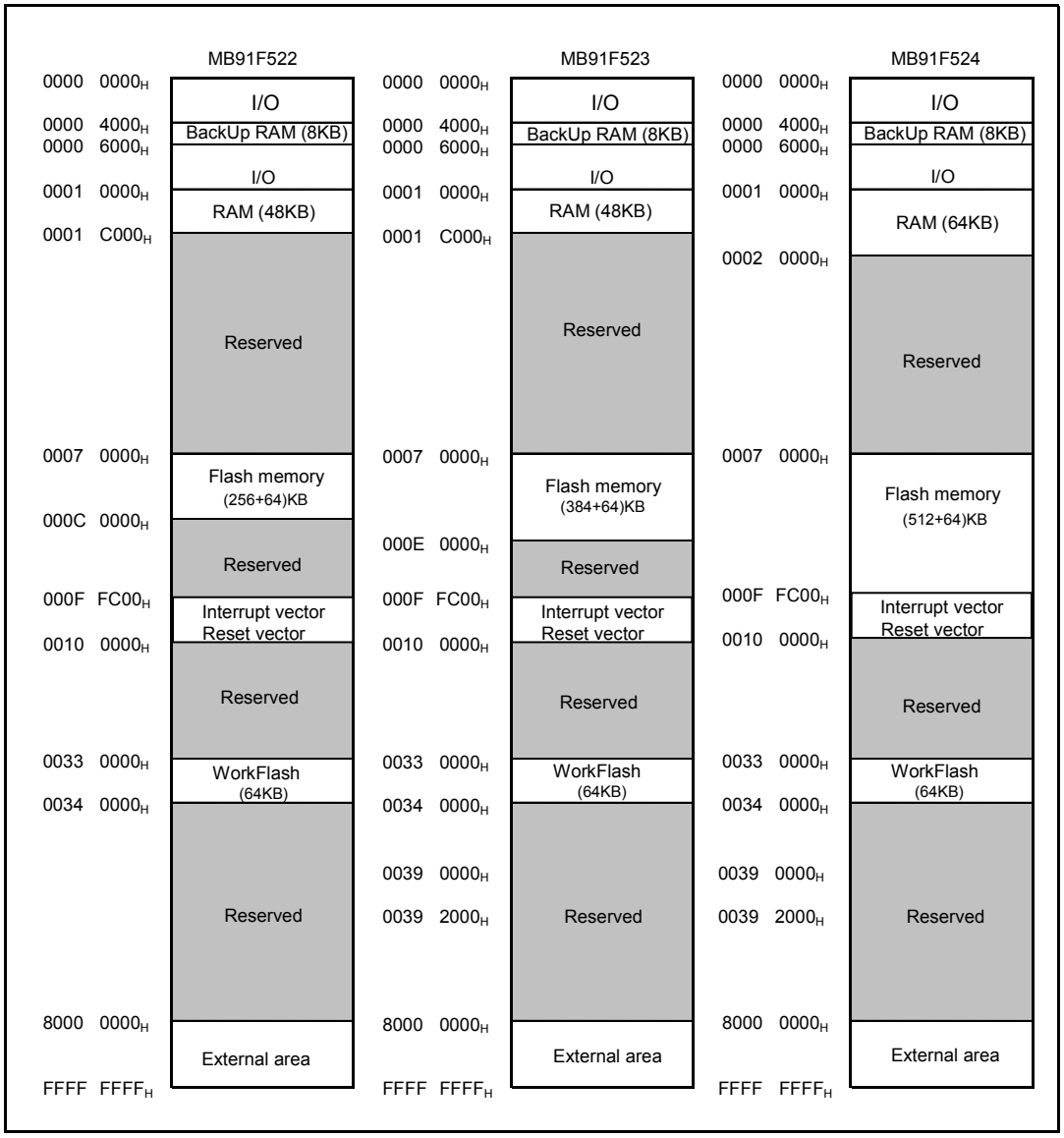
*1: Only channel 3 and channel 4 support the I^2C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	113 *1	133	161	P002	-	F	General-purpose I/O port
						D18 *5	-		External bus data bit18 I/O
						SCK1_0	-		Multi-function serial ch.1 clock I/O (0)
						TIOB0_1	-		TIOB input of Base timer ch.0 (1)
-	76 *1	96 *1	114 *1	134	162	P003	-	F	General-purpose I/O port
						D19 *3, *4, *5	-		External bus data bit19 I/O
						SIN2_0	-		Multi-function serial ch.2 serial data input (0)
						TIOB1_1	-		TIOB input of Base timer ch.1 (1)
						INT3_0	-		INT3 External interrupt input (0)
-	-	-	-	135	163	P004	-	A	General-purpose I/O port
						D20	-		External bus data bit20 I/O (0)
						SOT2_0	-		Multi-function serial ch.2 serial data output (0)
-	-	-	-	-	164	P164	-	A	General-purpose I/O port
						PPG32_1	-		PPG ch.32 output (1)
61 *1	77 *1	97 *1	115 *1	136 *1	165 *1	P005	-	F	General-purpose I/O port
						D21 *2, *3, *4, *5	-		External bus data bit21 I/O (0)
						SCK2_0 *2	-		Multi-function serial ch.2 clock I/O (0)
						ADTG0_1	-		A/D converter external trigger input 0 (1)
						INT7_1	-		INT7 External interrupt input (1)
						RX2(64) *4, *5, *6, *7	-		CAN reception data 2 input
-	-	-	-	-	166	P165	-	A	General-purpose I/O port
						PPG33_1	-		PPG ch.33 output (1)
62 *1	78 *1	98 *1	116 *1	137 *1	167 *1	P006	-	A	General-purpose I/O port
						D22 *2, *3, *4, *5	-		External bus data bit22 I/O (0)
						SCS2_0 *2	-		Serial chip select 2 I/O (0)
						ADTG1_1	-		A/D converter external trigger input 1 (1)
						INT2_1	-		INT2 External interrupt input (1)
						TX2(64) *4, *5, *6, *7	-		CAN transmission data 2 output
-	-	-	117 *1	138	168	P007	-	A	General-purpose I/O port
						D23 *5	-		External bus data bit23 I/O
-	-	-	-	-	169	P166	-	A	General-purpose I/O port
						PPG34_1	-		PPG ch.34 output (1)
-	-	-	118 *1	139	170	P010	-	A	General-purpose I/O port
						D24 *5	-		External bus data bit24 I/O

8. Memory Map

MB91F522, MB91F523, MB91F524



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CF0_H$	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000CF4_H$	DCSR15 [R/W] H 0------- -----000		DTCR15 [R/W] H 00000000 00000000		
$000CF8_H$	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CFC_H$	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000D00_H$ to $000DF0_H$	—	—	—	—	Reserved [S]
$000DF4_H$	—	—	DNMIR [R/W] B 0------0	DILVR [R/W] B ---11111	DMA Controller [S]
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	—	—	—	—	Reserved [S]
$000E00_H$	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
$000E04_H$	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
$000E08_H$	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register
$000E0C_H$	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -0000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000	
$000E10_H$	—	—	—	—	
$000E14_H$	—	—	—	—	
$000E18_H$	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
$000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
$000E24_H$	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
$000E28_H$	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
$000E2C_H$	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
$000E30_H$	—	—	—	—	
$000E34_H$	—	—	—	—	
$000E38_H$	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001434_H	ADRCCS24[R/W] B,H,W 00000000	ADRCCS25[R/W] B,H,W 00000000	ADRCCS26[R/W] B,H,W 00000000	ADRCCS27[R/W] B,H,W 00000000	12-bit A/D converter 1/2 unit
001438_H	ADRCCS28[R/W] B,H,W 00000000	ADRCCS29[R/W] B,H,W 00000000	ADRCCS30[R/W] B,H,W 00000000	ADRCCS31[R/W] B,H,W 00000000	
$00143C_H$	ADRCOT0[R] B,H,W 00000000 00000000 00000000 00000000				
001440_H	ADRCIF0[R,W] B,H,W 00000000 00000000 00000000 00000000				
001444_H	ADSCANS0[R/W] B,H,W 000-----	—	—	—	
001448_H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	
$00144C_H$	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00	
001450_H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00	
001454_H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00	
001458_H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000				
$00145C_H$	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111				
001460_H	ADCS0[R] B,H,W 0------- --------		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0---0000	
001464_H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000	
001468_H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000	
$00146C_H$	—				12-bit A/D converter 2/2 unit
001470_H	ADTSS1[R/W] B,H,W -------0	—	—	—	
001474_H	ADTSE1[R/W] B,H,W -------- -------- 00000000 00000000				
001478_H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0018F0_H$	— /(SCSTR310)/ (LAMSR10) [R/W] B,H,W -------- *3	— /(SCSTR210)/ (LAMCR10) [R/W] B,H,W -------- *3	— /(SCSTR110)/ (SFLR110)[R/W] B,H,W -------- *3	— /(SCSTR010)/ (SFLR010)[R/W] B,H,W -------- *3	Multi-UART10 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$0018F4_H$	—	— /(SCSFR210) [R/W] B,H,W -------- *3	— /(SCSFR110) [R/W] B,H,W -------- *3	— /(SCSFR010) [R/W] B,H,W -------- *3	
$0018F8_H$	—/(TBYTE310)/ (LAMESR10) [R/W] B,H,W -------- *3	—/(TBYTE210)/ (LAMERT10) [R/W] B,H,W -------- *3	—/(TBYTE110)/ (LAMIER10) [R/W] B,H,W -------- *3	TBYTE010/(LAMRID 10)/(LAMTID10) [R/W] B,H,W 00000000	
$0018FC_H$	BGR10[R/W] H, W 00000000 00000000		— /(ISMK10)[R/W] B,H,W -------- *2	— /(ISBA10)[R/W] B,H,W -------- *2	
001900_H	FCR110[R/W] B,H,W ---00100	FCR010[R/W] B,H,W -0000000	FBYTE10[R/W] B,H,W 00000000 00000000		
001904_H	FTICR10[R/W] B,H,W 00000000 00000000		—	—	
001908_H	SCR11/(IBCR11) [R/W] B,H,W 0--00000	SMR11[R/W] B,H,W 000-00-0	SSR11[R/W] B,H,W 0-000011	ESCR11/(IBSR11) [R/W] B,H,W 00000000	Multi-UART11 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00190C_H$	— /(RDR111/(TDR111))[R/W] B,H,W -------- -------- *3		RDR011/(TDR011)[R/W] B,H,W -------0 00000000 *1		
001910_H	SACSR11[R/W] B,H,W 0----000 00000000		STMR11[R] B,H,W 00000000 00000000		
001914_H	STMCR11[R/W] B,H,W 00000000 00000000		— /(SCSCR11/SFUR11)[R/W] B,H,W -------- -------- *3 *4		
001918_H	— /(SCSTR311)/ (LAMSR11) [R/W] B,H,W -------- *3	— /(SCSTR211)/ (LAMCR11) [R/W] B,H,W -------- *3	— /(SCSTR111)/ (SFLR111)[R/W] B,H,W -------- *3	— /(SCSTR011)/ (SFLR011)[R/W] B,H,W -------- *3	
$00191C_H$	—	— /(SCSFR211) [R/W] B,H,W -------- *3	— /(SCSFR111) [R/W] B,H,W -------- *3	— /(SCSFR011) [R/W] B,H,W -------- *3	
001920_H	—/(TBYTE311)/ (LAMESR11) [R/W] B,H,W -------- *3	—/(TBYTE211)/ (LAMERT11) [R/W] B,H,W -------- *3	—/(TBYTE111)/ (LAMIER11) [R/W] B,H,W -------- *3	TBYTE011/(LAMRID 11)/(LAMTID11) [R/W] B,H,W 00000000	
001924_H	BGR11[R/W] H, W 00000000 00000000		— /(ISMK11)[R/W] B,H,W -------- *2	— /(ISBA11)[R/W] B,H,W -------- *2	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002254_H	IF2DTB12 [R/W] B,H,W 00000000 00000000		IF2DTB22 [R/W] B,H,W 00000000 00000000		CAN2 (64msb)
002258_H	—	—	—	—	
$00225C_H$	—	—	—	—	
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H to $00227C_H$	—				
002280_H	TREQR22 [R] B,H,W 00000000 00000000		TREQR12 [R] B,H,W 00000000 00000000		
002284_H	TREQR42 [R] B,H,W 00000000 00000000		TREQR32 [R] B,H,W 00000000 00000000		
002288_H	—	—	—	—	
$00228C_H$	—	—	—	—	
002290_H	NEWDT22 [R] B,H,W 00000000 00000000		NEWDT12 [R] B,H,W 00000000 00000000		
002294_H	NEWDT42 [R] B,H,W 00000000 00000000		NEWDT32 [R] B,H,W 00000000 00000000		
002298_H	—	—	—	—	
$00229C_H$	—	—	—	—	
$0022A0_H$	INTPND22 [R] B,H,W 00000000 00000000		INTPND12 [R] B,H,W 00000000 00000000		
$0022A4_H$	INTPND42 [R] B,H,W 00000000 00000000		INTPND32 [R] B,H,W 00000000 00000000		
$0022A8_H$	—	—	—	—	
$0022AC_H$	—	—	—	—	
$0022B0_H$	MSGVAL22 [R] B,H,W 00000000 00000000		MSGVAL12 [R] B,H,W 00000000 00000000		
$0022B4_H$	MSGVAL42 [R] B,H,W 00000000 00000000		MSGVAL32 [R] B,H,W 00000000 00000000		
$0022B8_H$	—	—	—	—	
$0022BC_H$	—	—	—	—	
$0022C0_H$ to $0022FC_H$	—				

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt vector
64 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*6
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*6
-	24	18	ICR08	$39C_H$	$000FFF9C_H$	-*6
-	25	19	ICR09	398_H	$000FFF98_H$	-*6
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
-	38	26	ICR22	364_H	$000FFF64_H$	-*6
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358_H	$000FFF58_H$	25*3
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/24/35	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 7/16/17/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 19	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29
Main timer	46	2E	ICR30	344_H	$000FFF44_H$	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
- -	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

(3-2) [MB9152xxxE]

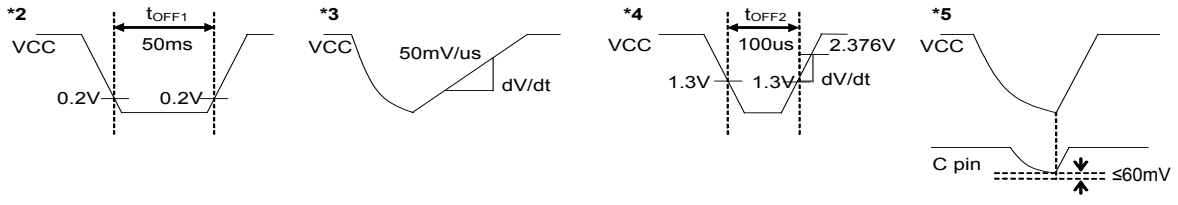
(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Power off time	t_{OFF1}	V_{CC}	Vcc ≤ 0.2V	50	–	–	ms	*2
	t_{OFF2}	V_{CC}	Vcc ≤ 1.3V	100	–	–	µs	*4
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2V to 2.376V (t_{OFF1}＜50ms)	–	–	50	mV/µs	*3
	dV/dt	V_{CC}	VCC: 1.3V to 2.376V (t_{OFF2} ≥ 100µs)	–	–	1000	mV/µs	*4
C pin voltage at Power-on	–	C	–	–	–	60	mV	*5
Maximum ramp rate guaranteed to not generate power-on reset	|dV/dt|	Vcc	VCC: Between 2.4V and 4.5V	–	–	50	mV/µs	*6

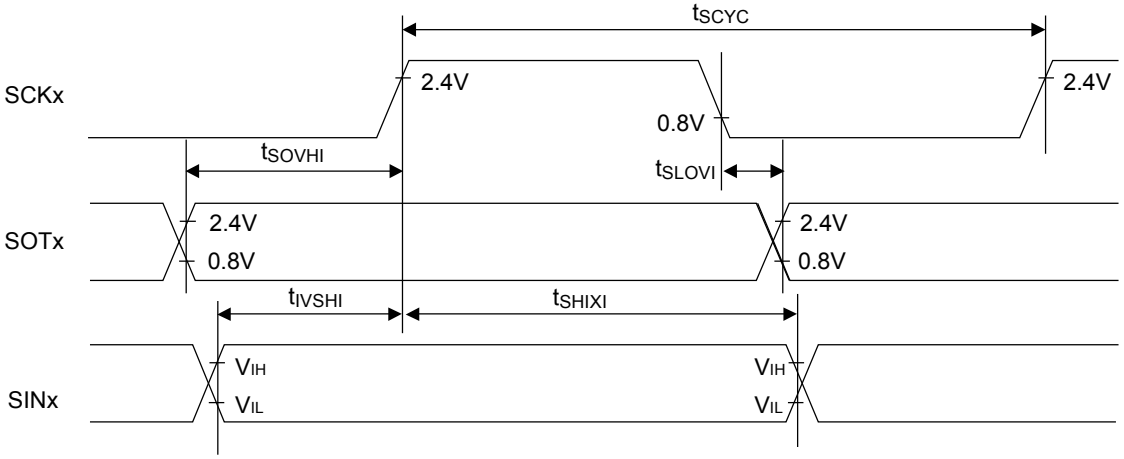
*1: The specified level detection time applies only for power ramp rate of 1000mV/µs or less.
*2: Vcc must be held below 0.2V for a minimum period of t_{OFF1}.
*3: Power-on can detect by satisfying power ramp rate when t_{OFF1} is not satisfied.
*4: Vcc must be held below 1.3V for a minimum period of t_{OFF2}.
Power ramp rate must be 1000mV/µs or less from 1.3V to 2.376V.
Power-on can detect by satisfying power ramp rate and power off time.
*5: C-pin voltage is below 60 mV when VCC is turned on again.
*6: This specification is specified the power supply fluctuation after power on detection. When VCC voltage is between 2.4V and 4.5V, the power supply fluctuation is below 50mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.

Note: When using MB91F52xxxE, either *2 or *3 or *4 or *5 must be satisfied. When neither *2 nor *3 nor *4 nor *5 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

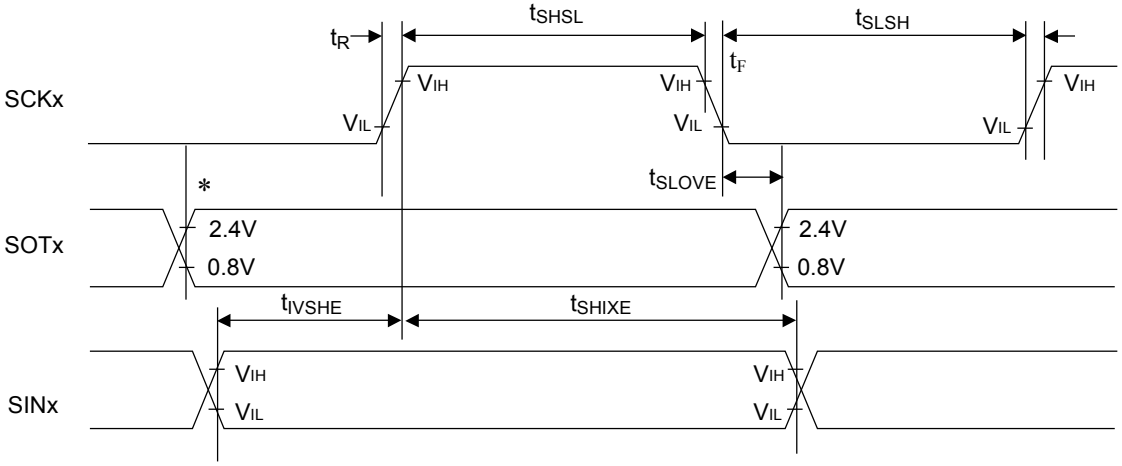
・Power off time, Power ramp rate, C pin voltage at Power-on



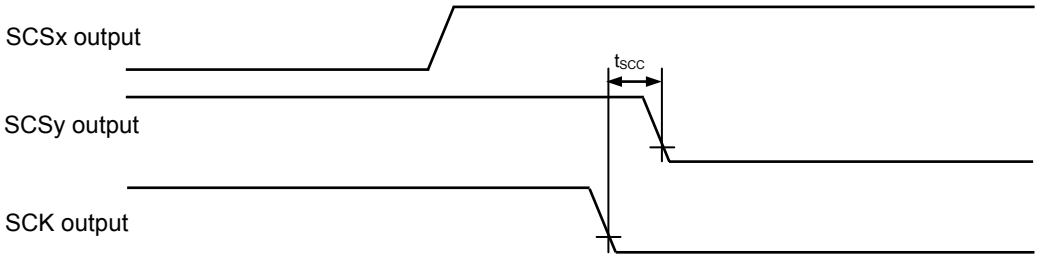
• Internal shift clock mode



• External shift clock mode

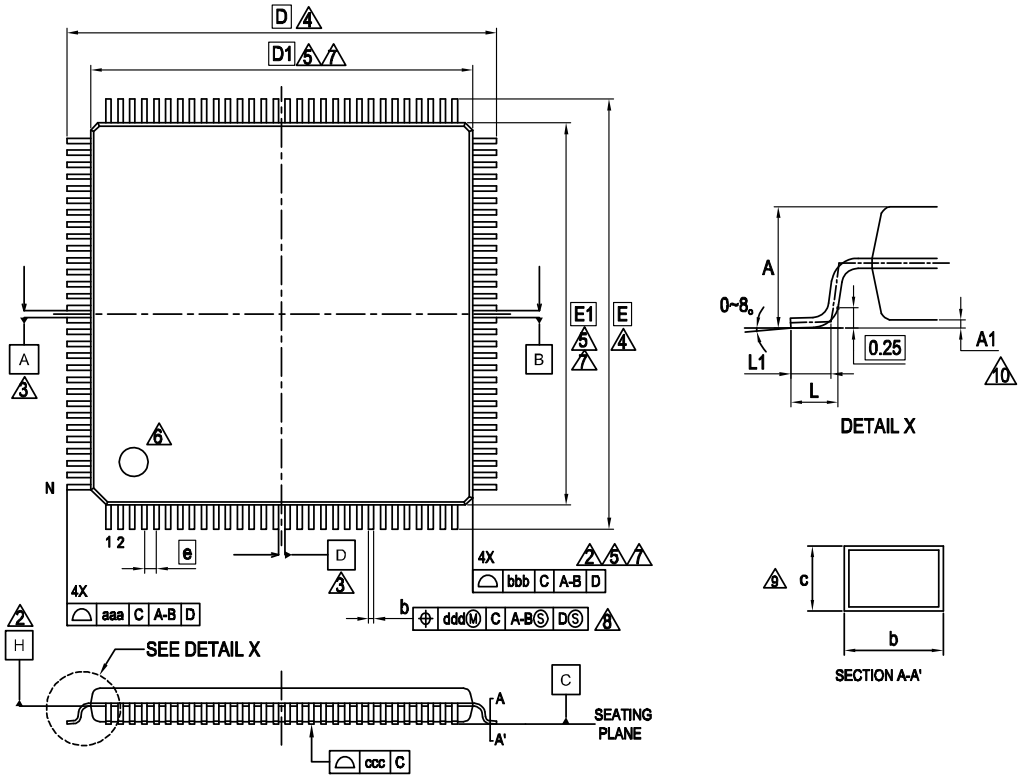


*: It writes in the TDR register and, then, it changes.



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

LQM120 , 120 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQM120		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.17	0.22	0.27
c	0.115	——	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.50 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	120		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

18. Errata

This section describes the errata for the MB91520 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
MB91F522B/D/F/J/K/L MB91F523B/D/F/J/K/L MB91F524B/D/F/J/K/L MB91F525B/D/F/J/K/L MB91F526B/D/F/J/K/L

MB91F522/3/4/5/6 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available MB91520 Series devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Power-on Conditions is not enough in the Datasheet Specification	MB91F522B/D/F/J/K/L MB91F523B/D/F/J/K/L MB91F524B/D/F/J/K/L MB91F525B/D/F/J/K/L MB91F526B/D/F/J/K/L	B, C	Will be fixed in production silicon version D, E
[2]. Limitation for Watch mode (power off)		B, C, D, E	-

1. Power-on Conditions is not enough in the Datasheet Specification

■ **Problem Definition**

If the Power-On-Reset and Internal Low Voltage Detection are not generated, some port functions will not be available.

■ **Parameters Affected**

t_{OFF} for Power off time on Power-on Conditions

VCC Power ramp rate on Power-on Conditions

■ **Trigger Condition**

When the power supply voltage to the MCU has been turned off but has not reached 0 V when the power supply voltage is turned on again, MCU does not generate an internal power-on-reset signal (Power-On reset or Internal LVD reset). Then, some port functions will not be available.

If below condition (1) or (2) or (3) is satisfied, Power-On Reset (Initialization-Reset signal) is generated and no problem occurs.

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

Page	Section	Change Results
158,161, 164,167	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	(4-1-5),(4-1-6)SCS↓⇒SOT delay time t_{DSE} (4-1-7),(4-1-8)SCS↑⇒SOT delay time t_{DSE} Corrected the following description. Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 SOT1 to SOT11 Value: Min - Max 40 ↓ Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73, SCS8 to SCS11 SOT1,SOT2,SOT5 to SOT11 Value: Min - Max 40 Pin name: SCS3,SCS40 to SCS43 SOT3,SOT4 Value: Min - Max 300
159,162, 165,168	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	(4-1-5)SCK↓⇒SCS↓ clock switch time t_{SCC} (4-1-6)SCK↑⇒SCS↓ clock switch time t_{SCC} (4-1-7)SCK↓⇒SCS↑ clock switch time t_{SCC} (4-1-8)SCK↑⇒SCS↑ clock switch time t_{SCC} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $3t_{CPP}$+0 Max $3t_{CPP}$+50 ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $3t_{CPP}$-10 Max $3t_{CPP}$+50 Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $3t_{CPP}$-300 Max $3t_{CPP}$+50
159,162, 165,168	■ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) CSIO timing (4-1-5),(4-1-6),(4-1-7),(4-1-8)	Added the following description. Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Added the value of "Total error". Total error value Min – Typ – Max ±12 LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB

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<tr><td>RTO0_1</td></tr>
<tr><td>SOT3_2</td></tr>
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<tr><td>SCK8_0/ SCL8</td></tr>
<tr><td>OCU9_1</td></tr>
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BIN1_0
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TRG4_1</td></tr>
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