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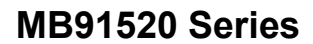
What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

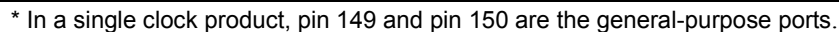
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525fscpmc-gte2



MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L





9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map

Read/Write attribute (R: Read W: Write)

Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090 _H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094 _H	-	BT1STC[R/W] B 00000000	-	-	
000098 _H	BT1PCSR/BT1PRL[R/W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
00009C _H	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -----11		
0000A0 _H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4 _H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W -----XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8 _H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

Data access attribute
B: Byte
H: Half-word
W: Word
(Note)The access by the data access attribute not described is disabled.

Initial register value after reset

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000400 _H	ICSEL0 [R/W] B,H,W ----000	ICSEL1 [R/W] B,H,W ----000	ICSEL2 [R/W] B,H,W -----0	ICSEL3 [R/W] B,H,W -----0	DMA request generation and clear
000404 _H	—	ICSEL5 [R/W] B,H,W ----000	ICSEL6 [R/W] B,H,W ---0000	ICSEL7 [R/W] B,H,W ---0000	
000408 _H	ICSEL8 [R/W] B,H,W -----00	ICSEL9 [R/W] B,H,W -----00	ICSEL10 [R/W] B,H,W -----00	ICSEL11 [R/W] B,H,W -----000	
00040C _H	—	ICSEL13 [R/W] B,H,W -----00	ICSEL14 [R/W] B,H,W -----00	ICSEL15 [R/W] B,H,W -----00	
000410 _H	ICSEL16 [R/W] B,H,W ---0000	ICSEL17 [R/W] B,H,W -----00	ICSEL18 [R/W] B,H,W ---00000	ICSEL19 [R/W] B,H,W -----000	
000414 _H	ICSEL20 [R/W] B,H,W -----000	ICSEL21 [R/W] B,H,W -----00	ICSEL22 [R/W] B,H,W -----00	ICSEL23 [R/W] B,H,W -----00	
000418 _H	IRPR0H [R] B,H,W 00-----	IRPR0L [R] B,H,W 00-----	IRPR1H [R] B,H,W 00-----	IRPR1L [R] B,H,W 00-----	Interrupt Request Batch Reading Register
00041C _H	—	—	IRPR3H [R] B,H,W 000000--	IRPR3L [R] B,H,W 000000--	
000420 _H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 000-----	
000424 _H	IRPR6H [R] B,H,W --00----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W -0-00--	IRPR7L [R] B,H,W -----00	
000428 _H	IRPR8H [R] B,H,W --0-----	IRPR8L [R] B,H,W -00-----	IRPR9H [R] B,H,W -0-----	IRPR9L [R] B,H,W -0-----	
00042C _H	IRPR10H [R] B,H,W -0-----	IRPR10L [R] B,H,W -0-----	IRPR11H [R] B,H,W 0-----	IRPR11L [R] B,H,W 0-----	
000430 _H	IRPR12H [R] B,H,W --0000--	IRPR12L [R] B,H,W ---00--	IRPR13H [R] B,H,W 00-----	IRPR13L [R] B,H,W 00-----	
000434 _H	IRPR14H [R] B,H,W 00000000	IRPR14L [R] B,H,W 00000000	IRPR15H [R] B,H,W 000-----	IRPR15L [R] B,H,W 0000000-	
000438 _H	ICSEL24 [R/W] B,H,W -----00	ICSEL25 [R/W] B,H,W ---00000	ICSEL26 [R/W] B,H,W -----0	ICSEL27 [R/W] B,H,W -----0	DMA request generation and clear
00043C _H	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000CF0 _H	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
000CF4 _H	DCSR15 [R/W] H 0-----000		DTCR15 [R/W] H 00000000 00000000		
000CF8 _H	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CFC _H	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000D00 _H to 000DF0 _H	—	—	—	—	Reserved [S]
000DF4 _H	—	—	DNMIR [R/W] B 0-----0	DILVR [R/W] B ---11111	DMA Controller [S]
000DF8 _H	DMACR[R/W] W 0-----0-----0-----0-----				
000DFC _H	—	—	—	—	Reserved [S]
000E00 _H	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
000E04 _H	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
000E08 _H	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register
000E0C _H	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -0000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000	
000E10 _H	—	—	—	—	
000E14 _H	—	—	—	—	
000E18 _H	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
000E1C _H	—	—	—	—	Reserved
000E20 _H	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
000E24 _H	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
000E28 _H	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
000E2C _H	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
000E30 _H	—	—	—	—	
000E34 _H	—	—	—	—	
000E38 _H	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001344 _H	ADCOMP28/ADCOMPB28[R/W] H,W 00000000 00000000		ADCOMP29/ADCOMPB29[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001348 _H	ADCOMP30/ADCOMPB30[R/W] H,W 00000000 00000000		ADCOMP31/ADCOMPB31[R/W] H,W 00000000 00000000		
00134C _H	ADTCS0[R/W] B,H,W 00000000 0010----		ADTCS1[R/W] B,H,W 00000000 0010----		
001350 _H	ADTCS2[R/W] B,H,W 00000000 0010----		ADTCS3[R/W] B,H,W 00000000 0010----		
001354 _H	ADTCS4[R/W] B,H,W 00000000 0010----		ADTCS5[R/W] B,H,W 00000000 0010----		
001358 _H	ADTCS6[R/W] B,H,W 00000000 0010----		ADTCS7[R/W] B,H,W 00000000 0010----		
00135C _H	ADTCS8[R/W] B,H,W 00000000 0010----		ADTCS9[R/W] B,H,W 00000000 0010----		
001360 _H	ADTCS10[R/W] B,H,W 00000000 0010----		ADTCS11[R/W] B,H,W 00000000 0010----		
001364 _H	ADTCS12[R/W] B,H,W 00000000 0010----		ADTCS13[R/W] B,H,W 00000000 0010----		
001368 _H	ADTCS14[R/W] B,H,W 00000000 0010----		ADTCS15[R/W] B,H,W 00000000 0010----		
00136C _H	ADTCS16[R/W] B,H,W 00000000 0010----		ADTCS17[R/W] B,H,W 00000000 0010----		
001370 _H	ADTCS18[R/W] B,H,W 00000000 0010----		ADTCS19[R/W] B,H,W 00000000 0010----		
001374 _H	ADTCS20[R/W] B,H,W 00000000 0010----		ADTCS21[R/W] B,H,W 00000000 0010----		
001378 _H	ADTCS22[R/W] B,H,W 00000000 0010----		ADTCS23[R/W] B,H,W 00000000 0010----		
00137C _H	ADTCS24[R/W] B,H,W 00000000 0010----		ADTCS25[R/W] B,H,W 00000000 0010----		
001380 _H	ADTCS26[R/W] B,H,W 00000000 0010----		ADTCS27[R/W] B,H,W 00000000 0010----		
001384 _H	ADTCS28[R/W] B,H,W 00000000 0010----		ADTCS29[R/W] B,H,W 00000000 0010----		
001388 _H	ADTCS30[R/W] B,H,W 00000000 0010----		ADTCS31[R/W] B,H,W 00000000 0010----		
00138C _H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001390 _H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
006000 _H to 00E _{FFC} _H	—	—	—	—	Reserved
00F000 _H to 00FE _{FC} _H	—	—	—	—	Reserved [S]
00FF00 _H	DSUCR [R/W] B,H,W -----0		—	—	OCDU [S]
00FF04 _H to 00FF0C _H	—				Reserved [S]
00FF10 _H	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF14 _H	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF18 _H to 00FF4 _H	—				Reserved [S]
00FF8 _H	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FFFC _H	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Used with the INT instruction	66 255	42 FF	-	2F4 _H 000 _H	000FFE4 _H 000FFC00 _H	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: REALOS is a trademark of Cypress.

80 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFE4 _H	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFD8 _H	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFC8 _H	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFB8 _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁷
External low-voltage detection interrupt						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Reload timer 3/6/7	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFA8 _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
-	22	16	ICR06	3A4 _H	000FFFA4 _H	-* ⁶
-	23	17	ICR07	3A0 _H	000FFFA0 _H	-* ⁶
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF98 _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29 ^{*1}
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)	47	2F	ICR31	340 _H	000FFF40 _H	31 ^{*1, *4}
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/7/9/10/11/12/13/14/15/16 17/18/19/22/23/26/27/28/29/31	48	30	ICR32	33C _H	000FFF3C _H	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334 _H	000FFF34 _H	34 ^{*5}
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5	51	33	ICR35	330 _H	000FFF30 _H	35 ^{*5}
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching/measurement)	52	34	ICR36	32C _H	000FFF2C _H	36 ^{*1}
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching/measurement)	53	35	ICR37	328 _H	000FFF28 _H	37
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching/measurement)	54	36	ICR38	324 _H	000FFF24 _H	38 ^{*1}
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer underflow 0/1/2						
WG dead timer reload 0/1/2						
WG DTTI 0						
32-bit ICU4 (fetching/measurement)	56	38	ICR40	31C _H	000FFF1C _H	40
Multi-function serial interface ch.11 (transmission completed)						

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IH1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	$0.7 \times V_{CC}$	-	V_{CC}	V	
	V_{IH3}	Port other than V_{IH1}	Automotive input level	$0.8 \times V_{CC}$	-	V_{CC}	V	
	V_{IH5}	RSTX,NMIX,M D0,MD1	CMOS hysteresis input level	$0.8 \times V_{CC}$	-	V_{CC}	V	
	V_{IHT}	DEBUGIF	TTL input level	2	-	V_{CC}	V	
“L” level input voltage	V_{IL1}	P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153	CMOS hysteresis input level	V_{SS}	-	$0.3 \times V_{CC}$	V	
	V_{IL3}	Port other than V_{IH1}	Automotive input level	V_{SS}	-	$0.5 \times V_{CC}$	V	
	V_{IL5}	RSTX,NMIX,M D0,MD1	CMOS hysteresis input level	V_{SS}	-	$0.2 \times V_{CC}$	V	
	V_{ILT}	DEBUGIF	TTL input level	V_{SS}	-	0.8	V	

*: It is a standard in BRAMSC (Backup RAM sleep control bit)=1(Enter the state of the sleep at the standby mode) condition.

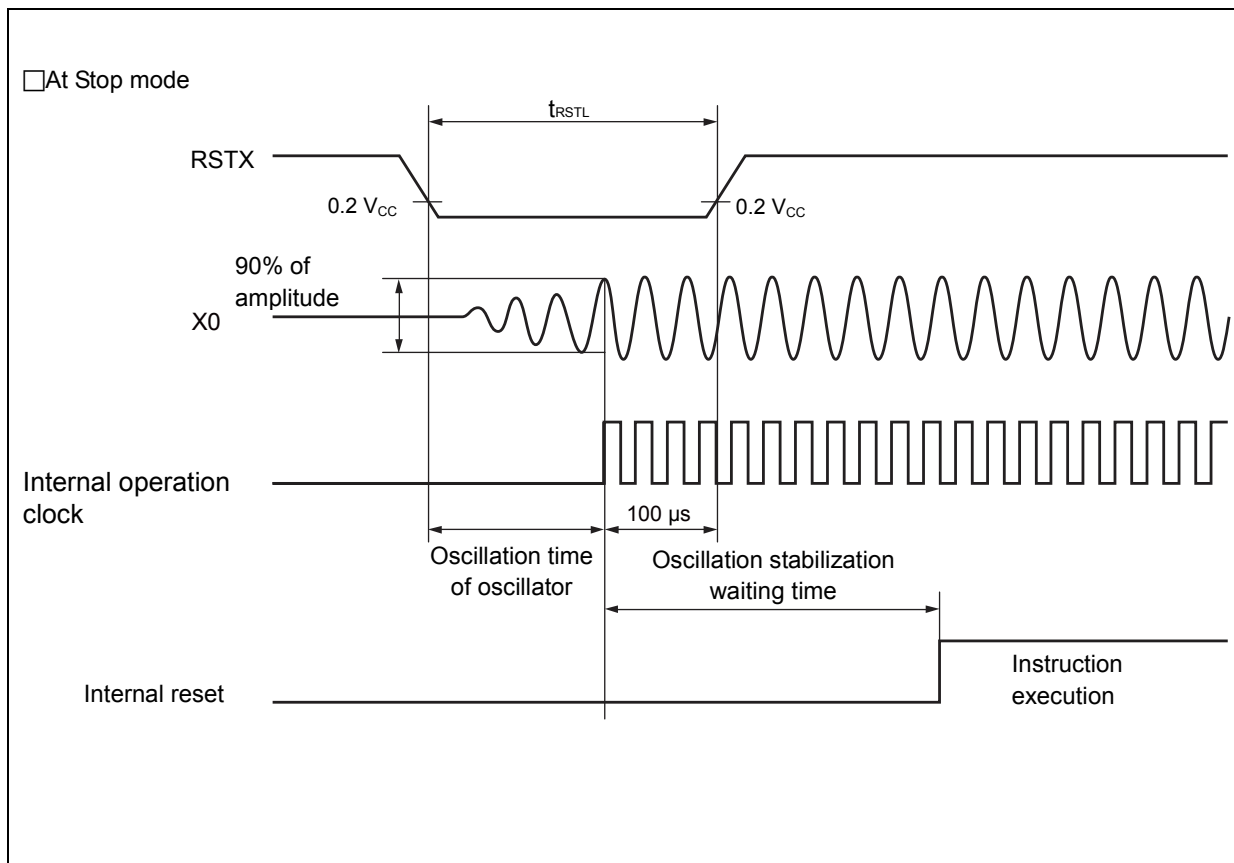
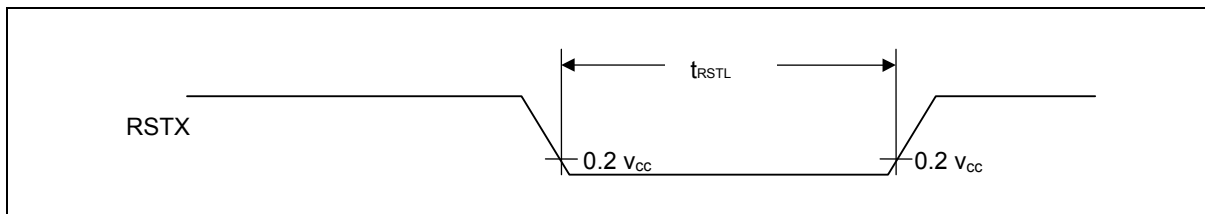
(2) Reset Input

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{RSTL}	RSTX	—	10	—	μs	When normal operation
				Oscillation time of oscillator* +100	—	μs	At Stop mode At Power-on* ²
				100	—	μs	At Watch mode
Width for reset input removal				1	—	μs	

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred μs and several ms, and for an external clock, the time is 0 ms.

*2: In case of using MB91F52xxxD or MB91F52xxxE and corresponding note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.



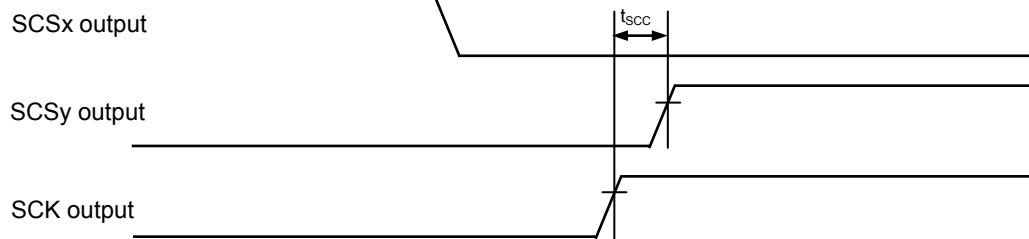
SCSx output

SCSy output

SCK output

t_{scc}

When Serial chip select is used , Serial clock output mark level "H"
 ,Serial chip select Inactive level "H"
 Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

Flash memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbytes sector* ¹ , excluding internal preprogramming time
	–	300	1100	ms	8 Kbytes sector* ¹ , including internal preprogramming time
	–	400	2000	ms	64 Kbytes sector* ¹ , excluding internal preprogramming time
	–	700	3700	ms	64 Kbytes sector* ¹ , including internal preprogramming time
8-bit writing time	–	9	288	μs	Exclusive of overhead time at system level* ¹
16-bit writing time	–	12	384	μs	Exclusive of overhead time at system level* ¹
ECC writing time	–	9	288	μs	Exclusive of overhead time at system level* ¹
Erase cycle* ² / Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T _A =+85°C* ³

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited.

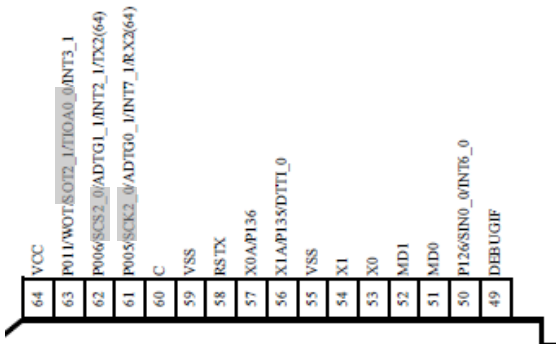
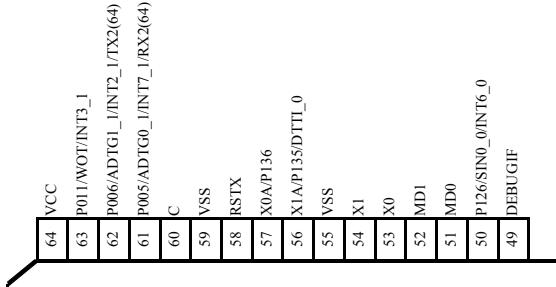
In the application system where V_{CC} might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold V_{CC} at 2.7V or more within the duration calculated by the following expression:

$$T_d^*[\mu s] + (\text{period of PCLK} [\mu s] \times 257) + 50 [\mu s]$$

*: See "4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) "

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWEPMC	Yes	ON	ON	LQI • 100 pin, Plastic
MB91F526FJEPMC		OFF	ON	
MB91F525FWEPMC		ON	ON	
MB91F525FJEPMC		OFF	ON	
MB91F524FWEPMC		ON	ON	
MB91F524FJEPMC		OFF	ON	
MB91F523FWEPMC		ON	ON	
MB91F523FJEPMC		OFF	ON	
MB91F522FWEPMC		ON	ON	
MB91F522FJEPMC		OFF	ON	
MB91F526FSEPMC	None	ON	ON	
MB91F526FHEPMC		OFF	ON	
MB91F525FSEPMC		ON	ON	
MB91F525FHEPMC		OFF	ON	
MB91F524FSEPMC		ON	ON	
MB91F524FHEPMC		OFF	ON	
MB91F523FSEPMC		ON	ON	
MB91F523FHEPMC		OFF	ON	
MB91F522FSEPMC		ON	ON	
MB91F522FHEPMC		OFF	ON	
MB91F526DWEPMC	Yes	ON	ON	LQH • 80 pin, Plastic
MB91F526DJEPMC		OFF	ON	
MB91F525DWEPMC		ON	ON	
MB91F525DJEPMC		OFF	ON	
MB91F524DWEPMC		ON	ON	
MB91F524DJEPMC		OFF	ON	
MB91F523DWEPMC		ON	ON	
MB91F523DJEPMC		OFF	ON	
MB91F522DWEPMC		ON	ON	
MB91F522DJEPMC		OFF	ON	
MB91F526DSEPMC	None	ON	ON	
MB91F526DHEPMC		OFF	ON	
MB91F525DSEPMC		ON	ON	
MB91F525DHEPMC		OFF	ON	
MB91F524DSEPMC		ON	ON	
MB91F524DHEPMC		OFF	ON	
MB91F523DSEPMC		ON	ON	
MB91F523DHEPMC		OFF	ON	
MB91F522DSEPMC		ON	ON	
MB91F522DHEPMC		OFF	ON	

Page	Section	Change Results
13	■ Pin Assignment MB91F52xB	- Top  ↓ 
13	■ Pin Assignment MB91F52xB	The following note added on the bottom left of Figure. * In a single clock product, pin 56 and pin 57 are the general-purpose ports.

Page	Section	Change Results																																																																																																																																																																		
19	■PIN Description	A List of "Pin Description" modified.																																																																																																																																																																		
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Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Value: Min -30 Max 30 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min -30 Max 30 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min -300 Max 300 (4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time t_{IVSHI} (4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time t_{IVSLI} Corrected the following description. Pin name: SCK0 to SCK11 SIN0 to SIN11 Value: Min 34 Max - ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11 Value: Min 34 Max - Pin name: SCK3,SCK4,SIN3,SIN4 Value: Min 300 Max - (4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVE} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVE} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min - Max 33 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min - Max 33 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min - Max 300 (4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time t_f Corrected the following description. Pin name: SCK0 to SCK2,SCK5 to SCK11 Value: Min - Max 5 Pin name: SCK3,SCK4 Value: Min - Max 250 ↓ Pin name: SCK0 to SCK11 Value: Min - Max 5 (4-1-5)SCS↓⇒SCK↓ setup time t_{CSSI} (4-1-6)SCS↓⇒SCK↑ setup time t_{CSSI} (4-1-7)SCS↑⇒SCK↓ setup time t_{CSSI} (4-1-8)SCS↑⇒SCK↑ setup time t_{CSSI} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSSU}+0$ Max $t_{CSSU}+50$ ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSSU}-50$ Max $t_{CSSU}+0$ Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $t_{CSSU}-50$ Max $t_{CSSU}+300$