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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f525khhbpmc-gs-f4e1

1. Product Lineup

Product lineup comparison 64 pins

	MB91F522B	MB91F523B	MB91F524B	MB91F525B	MB91F526B
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB	(64+8)KB	(96+8)KB	(128+8)KB	
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	None				
Free-run Timer	16bit×3ch, 32bit×1ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×21ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×13ch (1unit), 12bit×13ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	8ch ^{*1}				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	44 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
NMI request function	Yes				
Operation guaranteed temperature (T _A)	-40°C to +125°C				
Power supply	2.7V to 5.5V ^{*2}				
Package	LQD064				

*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 100 pins

	MB91F522F	MB91F523F	MB91F524F	MB91F525F	MB91F526F
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
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Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB	(64+8)KB	(96+8)KB	(128+8)KB	
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×34ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×21ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch ^{*1}				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	76 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T _A)	-40°C to +125°C				
Power supply	2.7V to 5.5V ^{*2}				
Package	LQI100				

*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	80	96	115	141	P130	-	F	General-purpose I/O port
						SCK0_0	-		Multi-function serial ch.0 clock I/O (0)
-	-	-	-	-	142	P162	-	A	General-purpose I/O port
						TRG5_2	-		PPG trigger 5 input (2)
-	-	-	-	-	143	P163	-	A	General-purpose I/O port
						TRG6_2	-		PPG trigger 6 input (2)
51	65	81	97	116	144	MD0	-	K	Mode pin 0
52	66	82	98	117	145	MD1	-	K	Mode pin 1
53	67	83	99	118	146	X0	-	N	Main clock oscillation input
54	68	84	100	119	147	X1	-	N	Main clock oscillation output
56	70	86	102	121	149	P135	-	A	General-purpose I/O port
						DTTI_0	-		Waveform generator ch.0-ch.5 input pin (0)
						X1A	-	O	Sub clock oscillation output
57	71	87	103	122	150	P136	-	A	General-purpose I/O port
						X0A	-	O	Sub clock oscillation input
58	72	88	104	123	151	RSTX	N	M	External reset input
-	-	-	-	124	152	P131	-	A	General-purpose I/O port
						ADTG0_0	-		A/D converter external trigger input 0 (0)
-	-	-	105	125	153	P132	-	A	General-purpose I/O port
						SCS1_0	-		Serial chip select 1 I/O (0)
						ADTG1_0	-		A/D converter external trigger input 1 (0)
-	-	89	106	126	154	P133	-	A	General-purpose I/O port
						TX2(64)	-		CAN transmission data 2 output
-	-	90	107	127	155	P134	-	F	General-purpose I/O port
						RX2(64)	-		CAN reception data 2 input
						SCS1_1	-		Serial chip select 1 I/O (1)
						ICU7_0	-		Input capture ch.7 input (0)
						INT7_0	-		INT7 External interrupt input (0)
-	-	91	108	128	156	P144	-	F	General-purpose I/O port
						SCK1_1	-		Multi-function serial ch.1 clock I/O (1)
-	-	94*1	111*1	131	159	P000	-	F	General-purpose I/O port
						D16*4,*5	-		External bus data bit16 I/O (0)
						SIN1_0	-		Multi-function serial ch.1 serial data input (0)
						TIOA0_1*4	-		TIOA output of Base timer ch.0 (1)
						INT2_0	-		INT2 External interrupt input (0)
-	75*1	95*1	112*1	132	160	P001	-	A	General-purpose I/O port
						D17*3,*4,*5	-		External bus data bit17 I/O
						SOT1_0*3	-		Multi-function serial ch.1 serial data output (0)
						TIOA1_1	-		TIOA I/O of Base timer ch.1 (1)

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000120 _H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU
000124 _H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128 _H	—	—	OCSH67 [R/W] B,H,W ---0--00	OCSL67 [R/W] B,H,W 0000--00	
00012C _H	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU
000130 _H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134 _H	—	—	OCSH89 [R/W] B,H,W ---0--00	OCSL89 [R/W] B,H,W 0000--00	
000138 _H to 0001B4 _H	—	—	—	—	Reserved
0001B8 _H	EPFR64 [R/W] B,H,W ----00-	EPFR65 [R/W] B,H,W 0000-000	EPFR66 [R/W] B,H,W --000000	EPFR67 [R/W] B,H,W ----0000	Extended port function register
0001BC _H	EPFR68 [R/W] B,H,W ----0000	EPFR69 [R/W] B,H,W ----0000	EPFR70 [R/W] B,H,W ---00000	EPFR71 [R/W] B,H,W -0-0-0-0	
0001C0 _H	EPFR72 [R/W] B,H,W 000000-0	EPFR73 [R/W] B,H,W 00000000	EPFR74 [R/W] B,H,W 00000000	EPFR75 [R/W] B,H,W 00000000	
0001C4 _H	EPFR76 [R/W] B,H,W 00000000	EPFR77 [R/W] B,H,W --000000	EPFR78 [R/W] B,H,W -----00	EPFR79 [R/W] B,H,W 00000000	
0001C8 _H	EPFR80 [R/W] B,H,W ---00000	EPFR81 [R/W] B,H,W 00000000	EPFR82 [R/W] B,H,W 00000000	EPFR83 [R/W] B,H,W -0000000	
0001CC _H	EPFR84 [R/W] B,H,W 00000000	EPFR85 [R/W] B,H,W --000000	EPFR86 [R/W] B,H,W ---00000	EPFR87 [R/W] B,H,W -----00	
0001D0 _H	EPFR88 [R/W] B,H,W -----0	—	—	—	
0001D4 _H	—	—	—	—	Reserved
0001D8 _H	TMRLRA4 [R/W] H XXXXXXXX XXXXXXXX		TMR4 [R] H XXXXXXXX XXXXXXXX		Reload Timer 4
0001DC _H	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXX		TMCSR4 [R/W] B, H,W 00000000 0-000000		
0001E0 _H to 0001EC _H	—	—	—	—	Reserved
0001F0 _H	TMRLRA5 [R/W] H XXXXXXXX XXXXXXXX		TMR5 [R] H XXXXXXXX XXXXXXXX		Reload Timer 5
0001F4 _H	TMRLRB5 [R/W] H XXXXXXXX XXXXXXXX		TMCSR5 [R/W] B, H,W 00000000 0-000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001434 _H	ADRCSS24[R/W] B,H,W 00000000	ADRCSS25[R/W] B,H,W 00000000	ADRCSS26[R/W] B,H,W 00000000	ADRCSS27[R/W] B,H,W 00000000	12-bit A/D converter 1/2 unit
001438 _H	ADRCSS28[R/W] B,H,W 00000000	ADRCSS29[R/W] B,H,W 00000000	ADRCSS30[R/W] B,H,W 00000000	ADRCSS31[R/W] B,H,W 00000000	
00143C _H	ADRCOT0[R] B,H,W 00000000 00000000 00000000 00000000				
001440 _H	ADRCIF0[R,W] B,H,W 00000000 00000000 00000000 00000000				
001444 _H	ADSCANS0[R/W] B,H,W 000-----	—	—	—	
001448 _H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	
00144C _H	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00	
001450 _H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00	
001454 _H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00	
001458 _H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000				
00145C _H	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111				
001460 _H	ADCS0[R] B,H,W 0-----		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0---0000	
001464 _H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000	
001468 _H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000	
00146C _H	—				12-bit A/D converter 2/2 unit
001470 _H	ADTSS1[R/W] B,H,W -----0	—	—	—	
001474 _H	ADTSE1[R/W] B,H,W ----- 00000000 00000000				
001478 _H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001AD0 _H	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG6
001AD4 _H	PDUT6 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
001AD8 _H	PCN206 [R/W] B,H,W --000000 ----110		PSDR6 [R/W] H,W 00000000 00000000		
001ADC _H	PTPC6 [R/W] H,W 00000000 00000000		—	—	
001AE0 _H	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG7
001AE4 _H	PDUT7 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
001AE8 _H	PCN207 [R/W] B,H,W --000000 ----110		PSDR7 [R/W] H,W 00000000 00000000		
001AEC _H	PTPC7 [R/W] H,W 00000000 00000000		—	—	
001AF0 _H	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG8
001AF4 _H	PDUT8 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
001AF8 _H	PCN208 [R/W] B,H,W --000000 ----110		PSDR8 [R/W] H,W 00000000 00000000		
001AFC _H	PTPC8 [R/W] H,W 00000000 00000000		—	—	
001B00 _H	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG9
001B04 _H	PDUT9 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
001B08 _H	PCN209 [R/W] B,H,W --000000 ----110		PSDR9 [R/W] H,W 00000000 00000000		
001B0C _H	PTPC9 [R/W] H,W 00000000 00000000		—	—	
001B10 _H	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG10
001B14 _H	PDUT10 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR10 [R] H,W 11111111 11111111		
001B18 _H	PCN210 [R/W] B,H,W --000000 ----110		PSDR10 [R/W] H,W 00000000 00000000		PPG10
001B1C _H	PTPC10 [R/W] H,W 00000000 00000000		—	—	
001B20 _H	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG11

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0020BC _H	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0 _H to 0020FC _H	—				
002100 _H	CTRLR1 [R/W] B,H,W ----- 000-0001		STATR1 [R/W] B,H,W ----- 00000000		
002104 _H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108 _H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W ----- X00000--		
00210C _H	BRPER1 [R/W] B,H,W ----- ----0000		—	—	
002110 _H	IF1CREQ1 [R/W] B,H,W 0----- 00000001		IF1CMSK1 [R/W] B,H,W ----- 00000000		
002114 _H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118 _H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C _H	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120 _H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124 _H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128 _H	—	—	—	—	
00212C _H	—	—	—	—	
002130 _H , 002134 _H	Reserved (IF1 data mirror)				CAN1 (64msb)
002138 _H	—	—	—	—	
00213C _H	—	—	—	—	
002140 _H	IF2CREQ1 [R/W] B,H,W 0----- 00000001		IF2CMSK1 [R/W] B,H,W ----- 00000000		
002144 _H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148 _H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C _H	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFE8 _H	-
Used with the INT instruction	66 255	42 FF	-	2F4 _H 000 _H	000FEF4 _H 000FFC00 _H	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

- *1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.
- *2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.
- *3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.
- *4: The clock calibration unit does not support a DMA transfer by the interrupt.
- *5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.
- *6: There is no resource corresponding to the interrupt level.
- *7: It does not support a DMA transfer by the external low-voltage detection interrupt.

100 pins

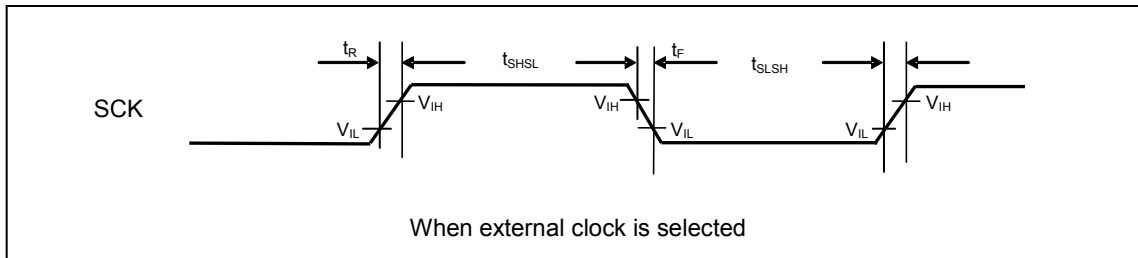
Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFE4 _H	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFD4 _H	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFC4 _H	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation	16	10	ICR00	3BC _H	000FFFB4 _H	0
External interrupt 0-7						
External interrupt 8-15						
External low-voltage detection interrupt						
Reload timer 0/1/4/5	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁷
Reload timer 2/3/6/7	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Multi-function serial interface ch.0 (reception completed)	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (status)	20	14	ICR04	3AC _H	000FFFA4 _H	4* ¹
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.1 (transmission completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (reception completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.2 (status)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						

(4-3) LIN Interface (v2.1)(Asynchronous Serial Interface for LIN (v2.1)) timing

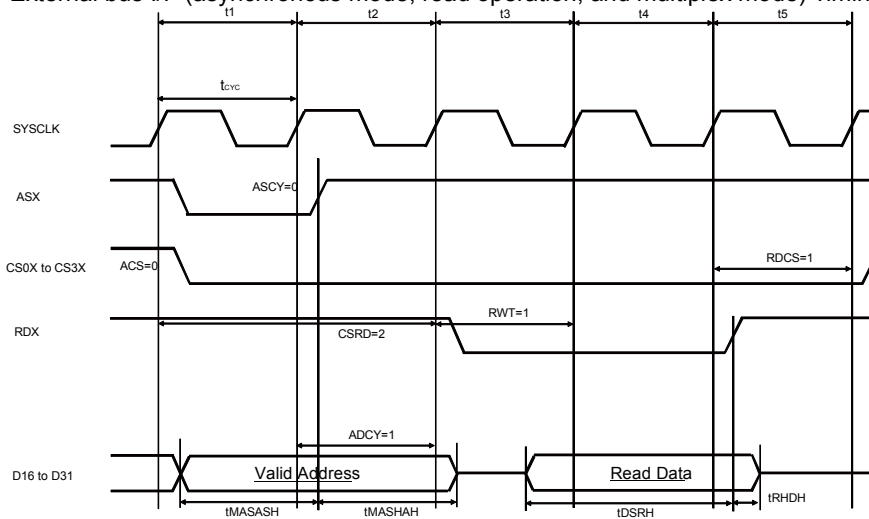
Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

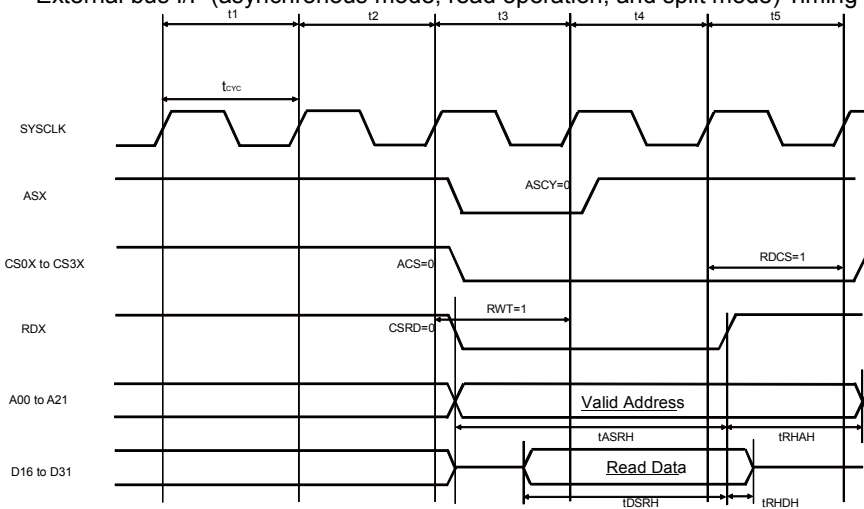
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK11	-	t _{CPP} +10	-	ns	output pin: C _L =50pF
Serial clock "H" pulse width	t _{SHSL}			t _{CPP} +10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	



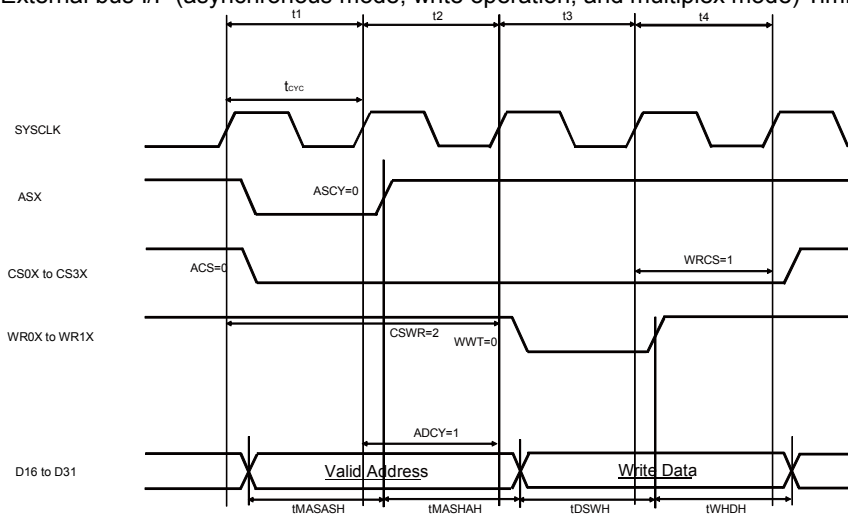
External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



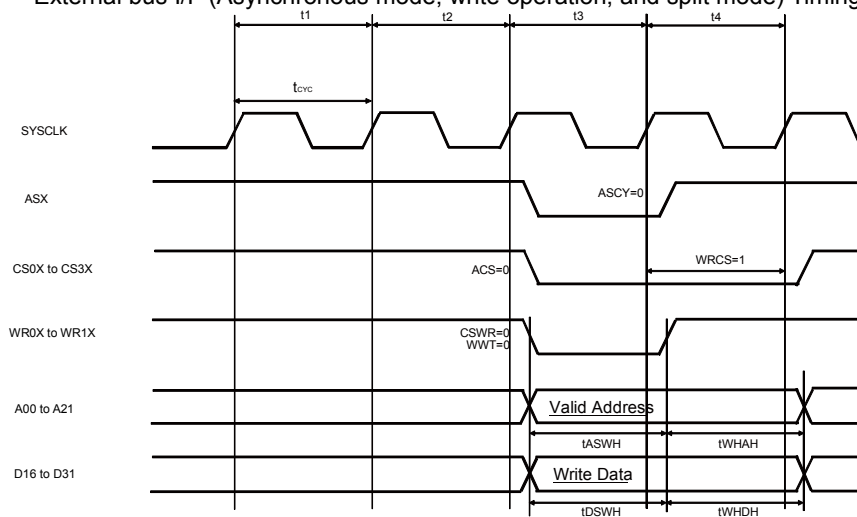
External bus I/F (asynchronous mode, read operation, and split mode) Timing



External bus I/F (asynchronous mode, write operation, and multiplex mode) Timing



External bus I/F (Asynchronous mode, write operation, and split mode) Timing

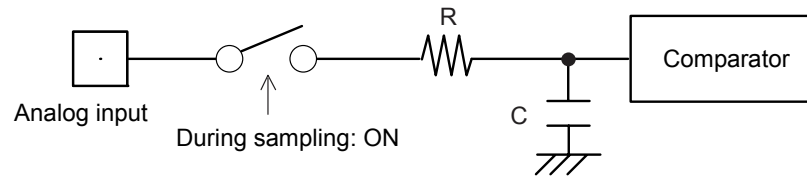


(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 μF) to the analog input pin.

- Analog input circuit model



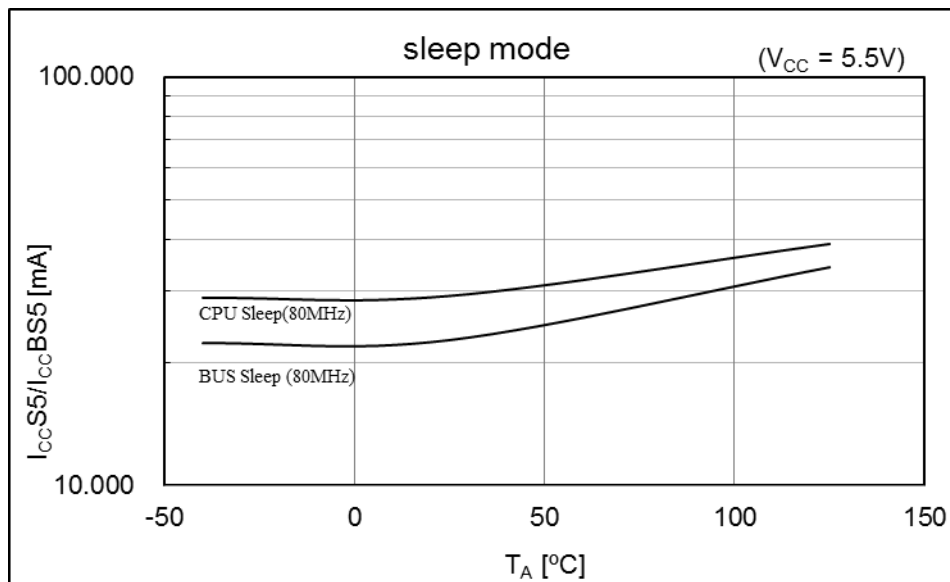
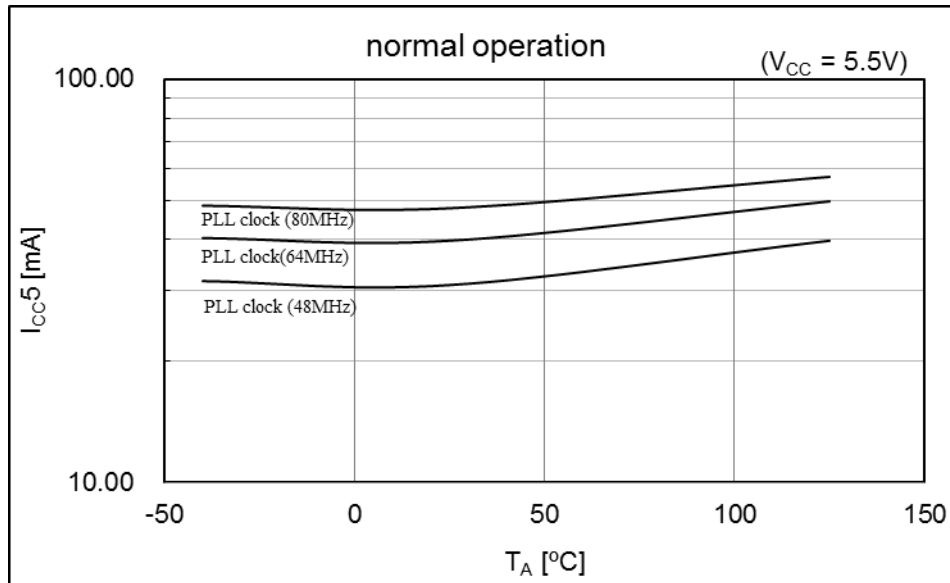
	R	C	
12bit A/D	1.9k Ω (Max)	8.30pF (Max)	(4.5V $\leq$ AV _{CC} $\leq$ 5.5V)
	4.3k Ω (Max)	8.30pF (Max)	(3.0V $\leq$ AV _{CC} $\leq$ 3.6V)

Note: Listed values must be considered as reference values.

12. EXAMPLE CHARACTERISTICS

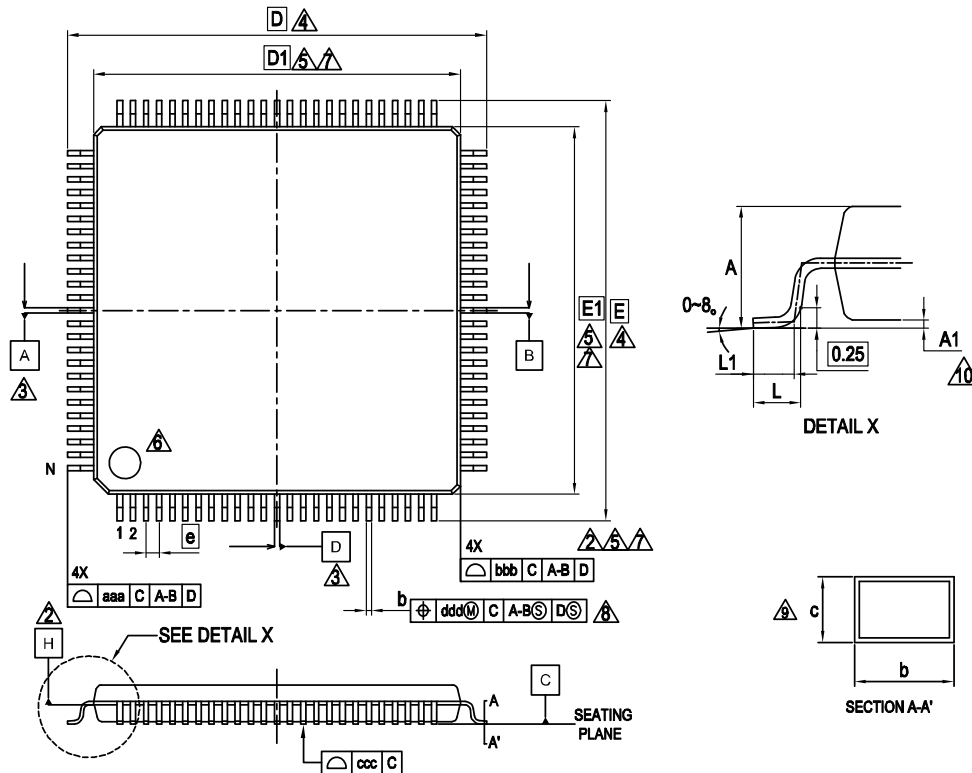
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

MB91F526



Part number	Sub clock	CSV Initial value	LVD Initial value	Package ^{*2}
MB91F526KWCPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYCPMC1			OFF	
MB91F526KJCPMC1		OFF	ON	
MB91F526KLCPMC1			OFF	
MB91F525KWCPMC1		ON	ON	
MB91F525KYCPMC1			OFF	
MB91F525KJCPMC1		OFF	ON	
MB91F525KLCPMC1			OFF	
MB91F524KWCPMC1		ON	ON	
MB91F524KYCPMC1			OFF	
MB91F524KJCPMC1		OFF	ON	
MB91F524KLCPMC1			OFF	
MB91F523KWCPMC1		ON	ON	
MB91F523KYCPMC1			OFF	
MB91F523KJCPMC1		OFF	ON	
MB91F523KLCPMC1			OFF	
MB91F522KWCPMC1		ON	ON	
MB91F522KYCPMC1			OFF	
MB91F522KJCPMC1		OFF	ON	
MB91F522KLCPMC1			OFF	
MB91F526KSCPMC1	None	ON	ON	
MB91F526KUCPMC1			OFF	
MB91F526KHCPMC1		OFF	ON	
MB91F526KKCPMC1			OFF	
MB91F525KSCPMC1		ON	ON	
MB91F525KUCPMC1			OFF	
MB91F525KHCPMC1		OFF	ON	
MB91F525KKCPMC1			OFF	
MB91F524KSCPMC1		ON	ON	
MB91F524KUCPMC1			OFF	
MB91F524KHCPMC1		OFF	ON	
MB91F524KKCPMC1			OFF	
MB91F523KSCPMC1		ON	ON	
MB91F523KUCPMC1			OFF	
MB91F523KHCPMC1		OFF	ON	
MB91F523KKCPMC1			OFF	
MB91F522KSCPMC1		ON	ON	
MB91F522KUCPMC1			OFF	
MB91F522KHCPMC1		OFF	ON	
MB91F522KKCPMC1			OFF	

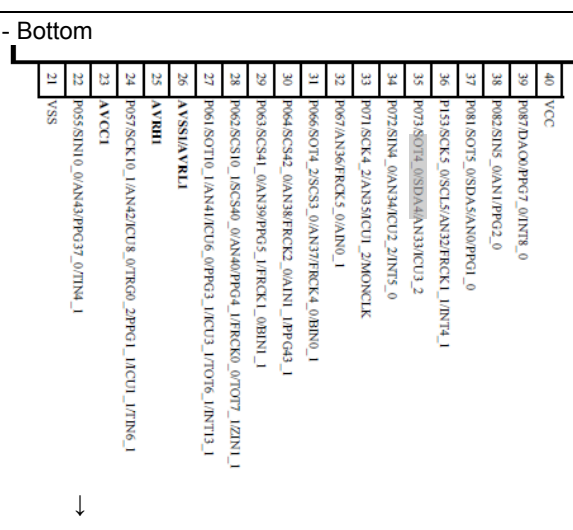
LQI100 , 100 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQI100		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	0.20	0.25
c	0.09	—	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
e	0.50 BSC.		
E	16.00 BSC.		
E1	14.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	100		

NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Page	Section	Change Results
14	■ Pin Assignment MB91F52xD	- Bottom 

Page	Section	Change Results				
Rev *C						
2	Features Peripheral Functions	The following sentence modified in I2C as following: (Error) < I2C > 2 channels ch.3 , ch.4 Standard mode/high-speed mode supported. Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported (Correct) < I2C > 2 channels ch.3 , ch.4 Standard mode/fast mode supported. Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported				
5,6,7,8,9,10	1. Product Lineup	The following *2 added as follows: (Error) <table><tr><td>Power supply</td><td>2.7 V to 5.5 V</td></tr></table> (Correct) <table><tr><td>Power supply</td><td>2.7 V to 5.5 V^{*2}</td></tr></table>	Power supply	2.7 V to 5.5 V	Power supply	2.7 V to 5.5 V ^{*2}
Power supply	2.7 V to 5.5 V					
Power supply	2.7 V to 5.5 V ^{*2}					
5,6,7,8,9,10	1. Product Lineup	The following sentence added as follows: (Correct) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.				
8, 9, 10,	1. Product Lineup	The following sentence modified in the bottom of Product lineup comparison table as following: (Error) *1: Only channel 3 and channel 4 support the I2C (high-speed mode/standard mode). (Correct) *1: Only channel 3 and channel 4 support the I2C (fast mode/standard mode).				
11	1. Product Lineup	Added silicon version E				

Page	Section	Change Results																																				
184	11. Electrical Characteristics AC Characteristics (4-4) I2C timing	The following sentence modified as following: (Error) <table><tr><th colspan="2">High-speed mode^{*3}</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr></table> Notes: Only ch.3 and ch.4 are standard mode/high-speed mode correspondence. *3: A high-speed mode I²C bus device can be used (Correct) <table><tr><th colspan="2">Fast mode^{*3}</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr></table> Notes: Only ch.3 and ch.4 are standard mode/fast mode correspondence. *3: A fast mode I²C bus device can be used	High-speed mode ^{*3}		Unit	Remarks	Min	Max	Fast mode ^{*3}		Unit	Remarks	Min	Max																								
High-speed mode ^{*3}		Unit	Remarks																																			
Min	Max																																					
Fast mode ^{*3}		Unit	Remarks																																			
Min	Max																																					
187	11. Electrical Characteristics (8) Low voltage detection (External low-voltage detection)	The following sentence modified in the Detection voltage as following: (Error) <table><tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr><tr><td>-8%</td><td>2.8</td><td>+8%</td><td>V</td><td>When power-supply voltage falls and detection level is set initially</td></tr></table> (Correct) <table><tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr><tr><td>-8%</td><td>LVD5F_SEL [3:0]</td><td>+8%</td><td>V</td><td>LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.</td></tr></table>	Value			Unit	Remarks	Min	Typ	Max	2.7	-	5.5	V		-8%	2.8	+8%	V	When power-supply voltage falls and detection level is set initially	Value			Unit	Remarks	Min	Typ	Max	2.7	-	5.5	V		-8%	LVD5F_SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Value			Unit	Remarks																																		
Min	Typ	Max																																				
2.7	-	5.5	V																																			
-8%	2.8	+8%	V	When power-supply voltage falls and detection level is set initially																																		
Value			Unit	Remarks																																		
Min	Typ	Max																																				
2.7	-	5.5	V																																			
-8%	LVD5F_SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.																																		
188	11. Electrical Characteristics (9) Low voltage detection (RAM retention low-voltage detection)	The following sentence modified as following: (Error) (9) Low voltage detection (Internal low-voltage detection) (Correct) (9) Low voltage detection (RAM retention low-voltage detection)																																				

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				(1) 12-bit A/D Converter Electrical Characteristics: Added the value of "Total error". Total error value Min – Typ – Max ± 12 LSB Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB Added the following description. Parameter : Power supply current I_AAVCC*3 *3: The power supply current described only current value on A/D converter. The total AVCC current value must be calculated the power supply current for A/D converter and D/A converter. Electrical Characteristics 7.D/A Converter: Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter. The total AVCC current value must be calculated the power supply current for D/A converter and A/D converter. Electrical Characteristics 6.Flash memory: Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing $T_j < +105^\circ\text{C}$" Electrical Characteristics 7.D/A Converter: Corrected the following description. Parameter : Power supply current Symbol I_A Pin name AV_{CC} Symbol I_{AH} Pin name AV_{CC} ↓ Symbol I_A Pin name AVCC Symbol I_{AH} Pin name AVCC Example Characteristics Corrected the following description. Watch mode Ordering Information Corrected the following description. • ORDERING INFORMATION ↓ • ORDERING INFORMATION MB91F52xxB*1