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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

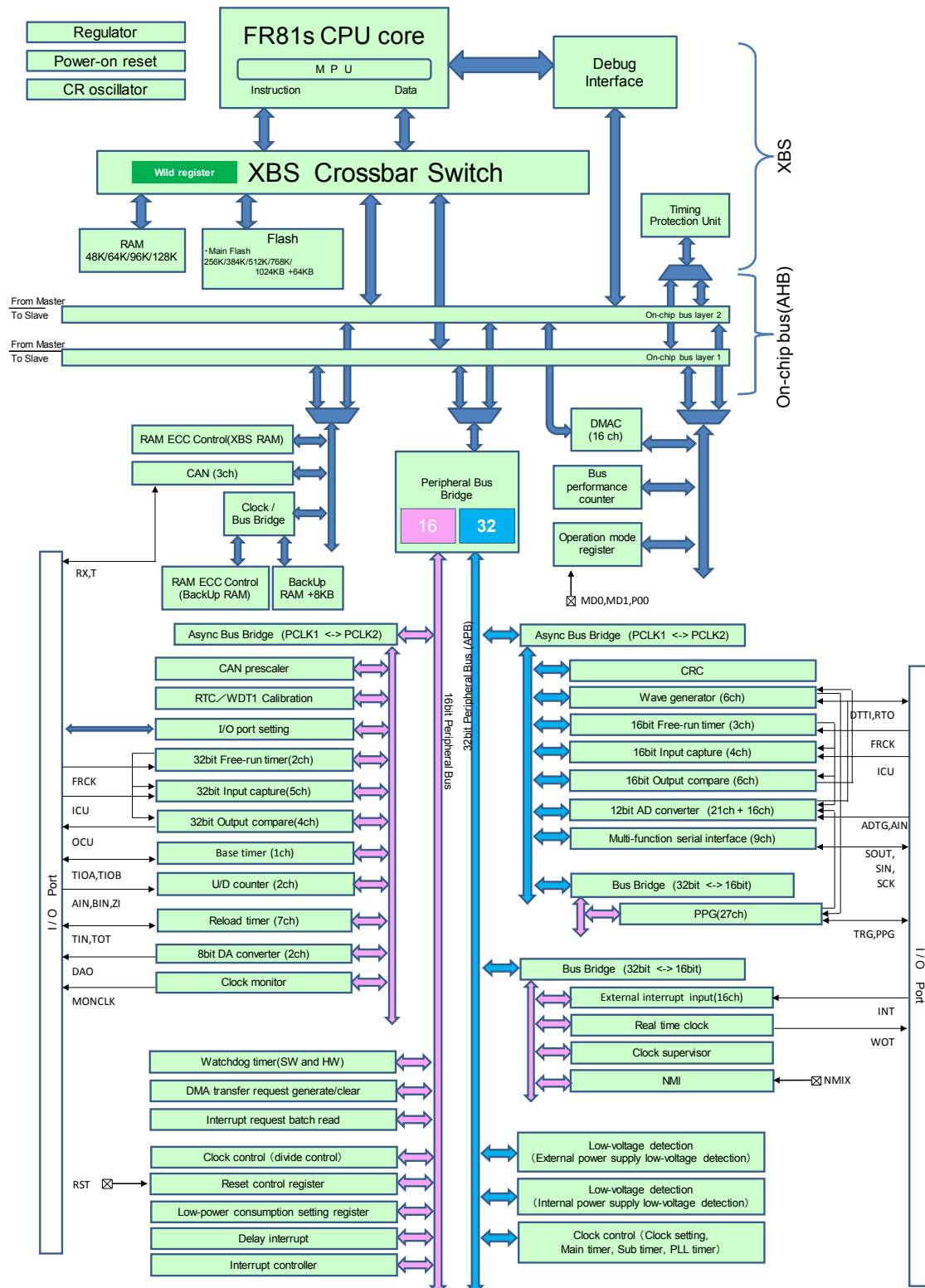
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526bsbpmc1-gse2

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	P032	-	A	General-purpose I/O port
						A04 ^{*2, *3, *4, *5}	-		External bus/Address bit4 output (0)
						SCS43_1	-		Serial chip select 43 output (1)
						PPG30_0	-		PPG ch.30 output (0)
						TOT3_0	-		Reload timer ch.3 output (0)
						RTO2_1	-		Waveform generator ch.2 output pin (1)
6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	P033	-	A	General-purpose I/O port
						A05 ^{*2, *3, *4, *5}	-		External bus/Address bit5 output (0)
						PPG31_0	-		PPG ch.31 output (0)
						ICU3_3	-		Input capture ch.3 input (3)
						TIN4_0	-		Reload timer ch.4 event input (0)
						RTO1_1	-		Waveform generator ch.1 output pin (1)
7 ^{*1}	9 ^{*1}	11 ^{*1}	14 ^{*1}	17	21	SCK3_2	-		Multi-function serial ch.3 clock I/O (2)
						P034	-	A	General-purpose I/O port
						A06 ^{*2, *3, *4, *5}	-		External bus/Address bit6 output (0)
						OCU11_1	-		Output compare ch.11 output (1)
						ICU2_3	-		Input capture ch.2 input (3)
						TIN5_0	-		Reload timer ch.5 event input (0)
-	-	12	15	18	22	RTO0_1	-	A	Waveform generator ch.0 output pin (1)
						SOT3_2	-		Multi-function serial ch.3 serial data output (2)
						P150	-	F	General-purpose I/O port
						SOT8_0/ SDA8	-		Multi-function serial ch.8 serial data output (0)/ I ² C bus serial data I/O
						OCU10_1	-		Output compare ch.10 output (1)
						TRG6_0	-		PPG trigger 6 input (0)
8 ^{*1}	10 ^{*1}	13	16	19	23	ICU1_3	-		Input capture ch.1 input (3)
						TIN6_0	-		Reload timer ch.6 event input (0)
						P151	-	F	General-purpose I/O port
						SCK8_0/ SCL8 ^{*2, *3}	-		Multi-function serial ch.8 clock I/O (0)/ I ² C bus serial clock I/O
						OCU9_1	-		Output compare ch.9 output (1)
						TRG7_0	-		PPG trigger 7 input (0)
						ICU0_3	-		Input capture ch.0 input (3)
						TIN7_0	-		Reload timer ch.7 event input (0)
						ZIN0_2	-		U/D counter ch.0 ZIN input (2)
						DTTI_1	-		Waveform generator ch.1 input pin (1)

MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D



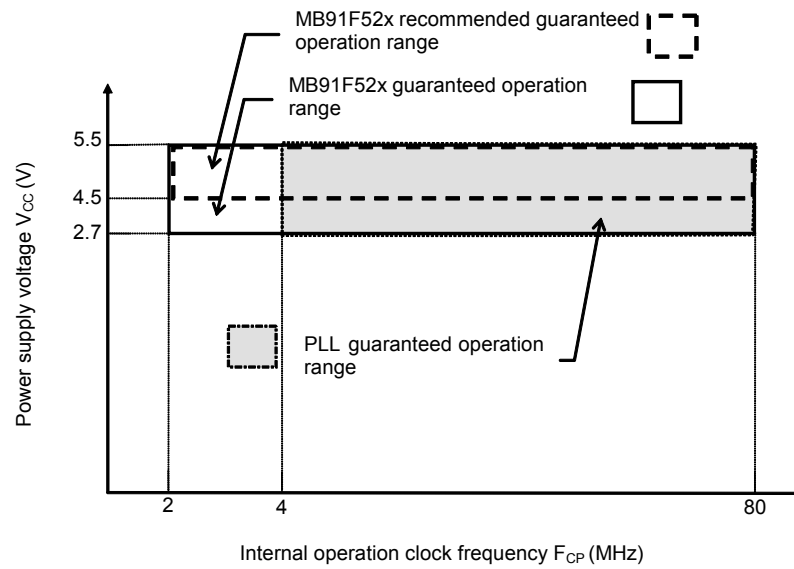
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00052C _H	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	Clock Control 2 [S]
000530 _H	CCRTSEL [R/W] B,H,W 0-----0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	
000534 _H to 00054C _H	—	—	—	—	Reserved
000550 _H	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External Interrupt (INT0 to 7)
000554 _H	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External Interrupt (INT8 to 15)
000558 _H	—	—	—	—	Reserved
00055C _H	—	—	WTDR [R/W] H 00000000 00000000		Real Time Clock (RTC)
000560 _H	—	WTCRH [R/W] B -----00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564 _H	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568 _H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
00056C _H	—	CSVCR [R/W] B 000111--	—	—	Clock Supervisor
000570 _H to 00057C _H	—	—	—	—	Reserved
000580 _H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator Control / Low Voltage Detection
000584 _H	LVD5R [R/W] B,H,W -----1	LVD5F [R/W] B,H,W 00000001	LVD [R/W] B,H,W 01000--0	—	
000588 _H to 00058C _H	—	—	—	—	Reserved
000590 _H	PMUSTR [R/W] B,H,W 0-----1X	PMUCLTR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594 _H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598 _H	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001750 _H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W]] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754 _H	— /(RDR10/(TDR10))[R/W] B,H,W ----- ^{*3}		RDR00/(TDR00)[R/W] B,H,W -----0 00000000 ^{*1}		
001758 _H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175C _H	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W ----- ^{*3} ^{*4}		
001760 _H	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W ----- ^{*3}	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W ----- ^{*3}	— /(SCSTR10)/ (SFLR10) [R/W] B,H,W ----- ^{*3}	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W ----- ^{*3}	
001764 _H	—	— /(SCSFR20) [R/W] B,H,W ----- ^{*3}	— /(SCSFR10) [R/W] B,H,W ----- ^{*3}	— /(SCSFR00) [R/W] B,H,W ----- ^{*3}	
001768 _H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W ----- ^{*3}	—/(TBYTE20)/ (LAMERT0) [R/W] B,H,W ----- ^{*3}	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W ----- ^{*3}	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	
00176C _H	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W ----- ^{*2}	— /(ISBA0) [R/W] B,H,W ----- ^{*2}	
001770 _H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774 _H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	
001778 _H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W]] B,H,W 00000000	Multi-UART1
00177C _H	— /(RDR11/(TDR11))[R/W] B,H,W ----- ^{*3}		RDR01/(TDR01)[R/W] B,H,W -----0 00000000 ^{*1}		
001780 _H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
001784 _H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W ----- ^{*3} ^{*4}		
001788 _H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W ----- ^{*3}	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W ----- ^{*3}	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W ----- ^{*3}	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W ----- ^{*3}	
00178C _H	—	— /(SCSFR21)[R/W] B,H,W ----- ^{*3}	— /(SCSFR11) [R/W] B,H,W ----- ^{*3}	— /(SCSFR01) [R/W] B,H,W ----- ^{*3}	

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
-	38	26	ICR22	364 _H	000FFF64 _H	-* ⁶
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
PPG 1/10/11/20/30/31	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/15/24/35	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 7/16/17/26/27/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/18/19/29	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48 _H	29
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						

• Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage



Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

(3) Power-on Conditions

(3-1) [MB9152xxxB/MB9152xxxC/MB9152xxxD]

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	—	V _{CC}	—	2.024	2.2	2.376	V	
Level detection hysteresis width	—	V _{CC}	—	—	100	—	mV	
Level detection time	—	—	—	—	—	30	μs	*1
Power off time	t _{OFF}	V _{CC}	—	50	—	—	ms	*2
Power ramp rate	dV/dt	V _{CC}	V _{CC} : 0.2V to 2.376V	—	—	4	mV/μs	*3
C pin voltage at Power-on	—	C	—	—	—	60	mV	*4

*1: This spec is at 4mV/μs of power ramp rate. If the power ramp rate is faster than 4mV/μs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}.

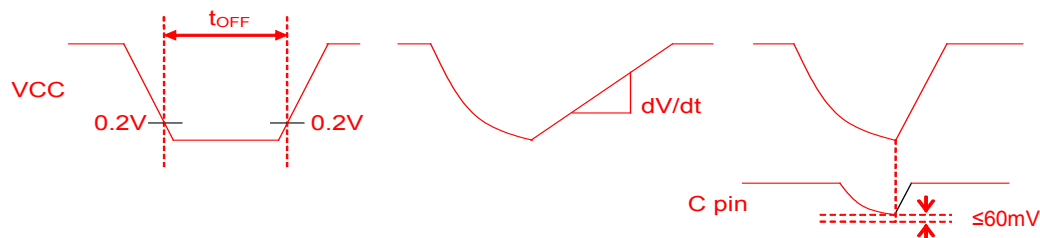
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when V_{CC} is turned on again.

Note:

When using MB91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use MB91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

• Power off time, Power ramp rate, C pin voltage at Power-on



(3-2) [MB9152xxxE]

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	—	V _{CC}	—	2.024	2.2	2.376	V	
Level detection hysteresis width	—	V _{CC}	—	—	100	—	mV	
Level detection time	—	—	—	—	—	30	μs	*1
Power off time	t _{OFF1}	V _{CC}	V _{CC} ≤ 0.2V	50	—	—	ms	*2
	t _{OFF2}	V _{CC}	V _{CC} ≤ 1.3V	100	—	—	μs	*4
Power ramp rate	dV/dt	V _{CC}	V _{CC} : 0.2V to 2.376V (t _{OFF1} < 50ms)	—	—	50	mV/μs	*3
	dV/dt	V _{CC}	V _{CC} : 1.3V to 2.376V (t _{OFF2} ≥ 100μs)	—	—	1000	mV/μs	*4
C pin voltage at Power-on	—	C	—	—	—	60	mV	*5
Maximum ramp rate guaranteed to not generate power-on reset	dV/dt	V _{CC}	V _{CC} : Between 2.4V and 4.5V	—	—	50	mV/μs	*6

*1: The specified level detection time applies only for power ramp rate of 1000mV/μs or less.

*2: V_{CC} must be held below 0.2V for a minimum period of t_{OFF1}.

*3: Power-on can detect by satisfying power ramp rate when t_{OFF1} is not satisfied.

*4: V_{CC} must be held below 1.3V for a minimum period of t_{OFF2}.

Power ramp rate must be 1000mV/μs or less from 1.3V to 2.376V.

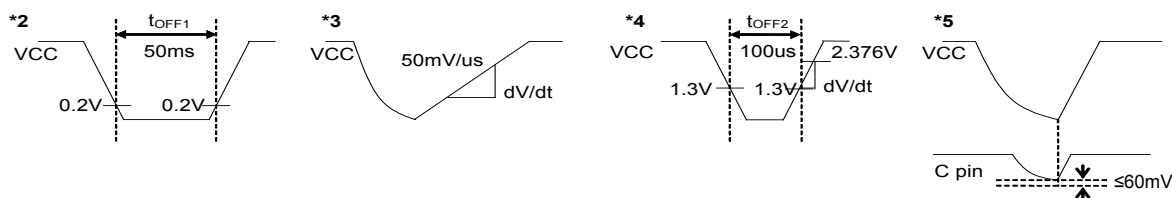
Power-on can detect by satisfying power ramp rate and power off time.

*5: C-pin voltage is below 60 mV when V_{CC} is turned on again.

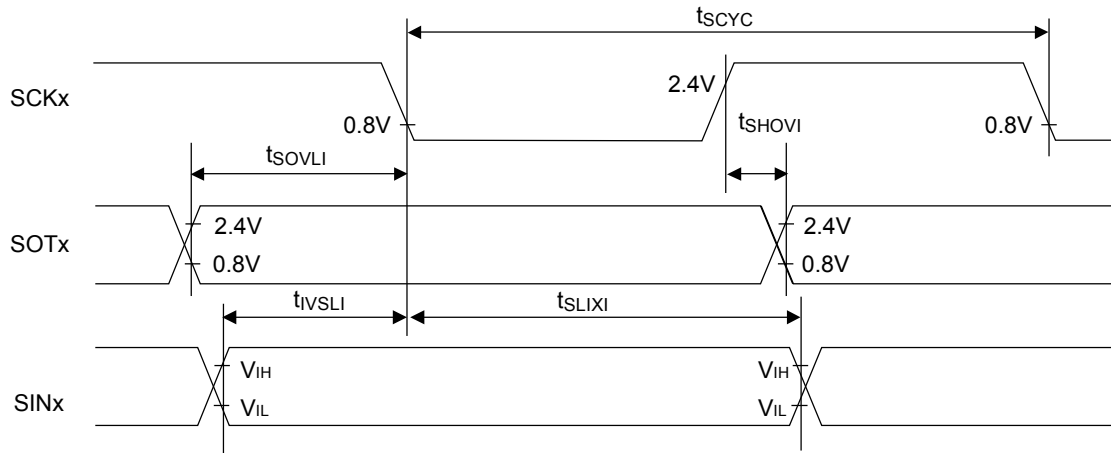
*6: This specification is specified the power supply fluctuation after power on detection. When V_{CC} voltage is between 2.4V and 4.5V, the power supply fluctuation is below 50mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.

Note: When using MB91F52xxxE, either *2 or *3 or *4 or *5 must be satisfied. When neither *2 nor *3 nor *4 nor *5 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

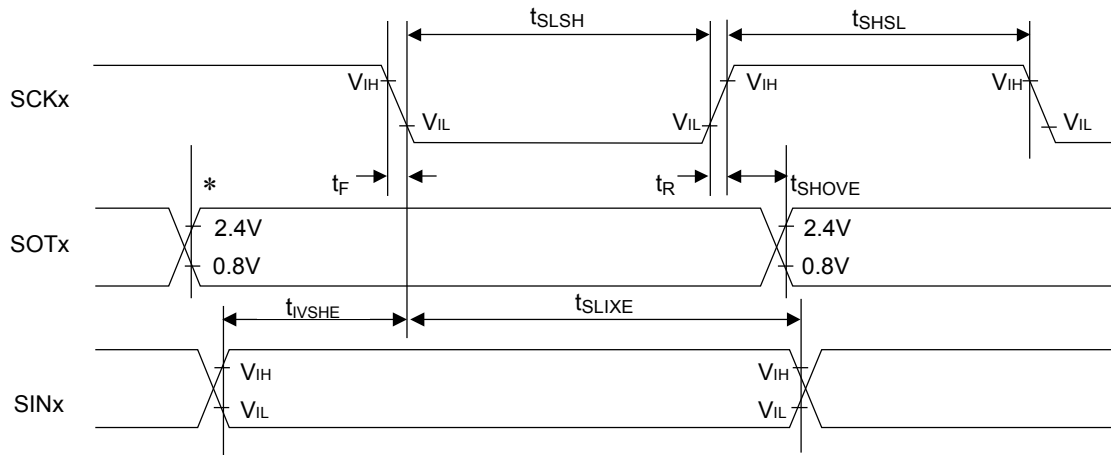
• Power off time, Power ramp rate, C pin voltage at Power-on



□ Internal shift clock mode



• External shift clock mode

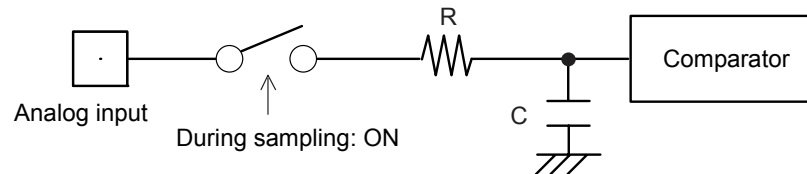


(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 μF) to the analog input pin.

- Analog input circuit model



	R	C	
12bit A/D	1.9k Ω (Max)	8.30pF (Max)	(4.5V $\leq$ AV _{CC} $\leq$ 5.5V)
	4.3k Ω (Max)	8.30pF (Max)	(3.0V $\leq$ AV _{CC} $\leq$ 3.6V)

Note: Listed values must be considered as reference values.

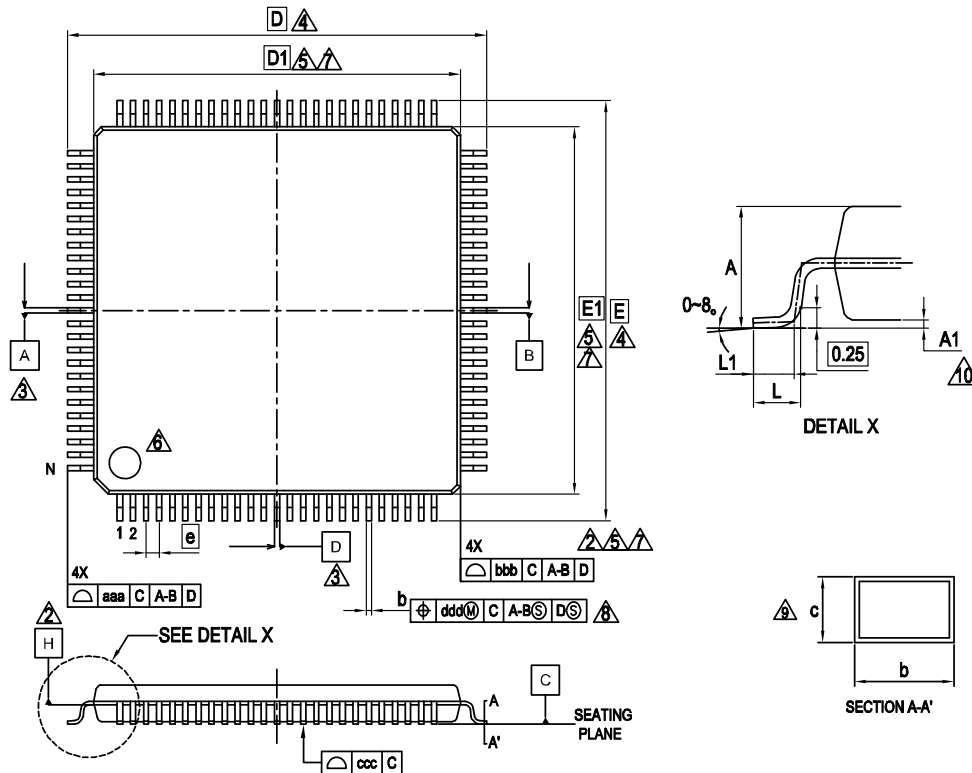
Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526JWBPMC	Yes	ON	ON	LQM • 120 pin, Plastic
MB91F526JYBPMC			OFF	
MB91F526JJBPMC		OFF	ON	
MB91F526JLBPMC			OFF	
MB91F525JWBPMC		ON	ON	
MB91F525JYBPMC			OFF	
MB91F525JJBPMC		OFF	ON	
MB91F525JLBPMC			OFF	
MB91F524JWBPMC		ON	ON	
MB91F524JYBPMC			OFF	
MB91F524JJBPMC		OFF	ON	
MB91F524JLBPMC			OFF	
MB91F523JWBPMC		ON	ON	
MB91F523JYBPMC			OFF	
MB91F523JJBPMC		OFF	ON	
MB91F523JLBPMC			OFF	
MB91F522JWBPMC		ON	ON	
MB91F522JYBPMC			OFF	
MB91F522JJBPMC		OFF	ON	
MB91F522JLBPMC			OFF	
MB91F526JSBPMC	None	ON	ON	
MB91F526JUBPMC			OFF	
MB91F526JHBPMC		OFF	ON	
MB91F526JKBPMC			OFF	
MB91F525JSBPMC		ON	ON	
MB91F525JUBPMC			OFF	
MB91F525JHBPMC		OFF	ON	
MB91F525JKBPMC			OFF	
MB91F524JSBPMC		ON	ON	
MB91F524JUBPMC			OFF	
MB91F524JHBPMC		OFF	ON	
MB91F524JKBPMC			OFF	
MB91F523JSBPMC		ON	ON	
MB91F523JUBPMC			OFF	
MB91F523JHBPMC		OFF	ON	
MB91F523JKBPMC			OFF	
MB91F522JSBPMC		ON	ON	
MB91F522JUBPMC			OFF	
MB91F522JHBPMC		OFF	ON	
MB91F522JKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package ^{*2}
MB91F526KWCPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYCPMC1			OFF	
MB91F526KJCPMC1		OFF	ON	
MB91F526KLCPMC1			OFF	
MB91F525KWCPMC1		ON	ON	
MB91F525KYCPMC1			OFF	
MB91F525KJCPMC1		OFF	ON	
MB91F525KLCPMC1			OFF	
MB91F524KWCPMC1		ON	ON	
MB91F524KYCPMC1			OFF	
MB91F524KJCPMC1		OFF	ON	
MB91F524KLCPMC1			OFF	
MB91F523KWCPMC1		ON	ON	
MB91F523KYCPMC1			OFF	
MB91F523KJCPMC1		OFF	ON	
MB91F523KLCPMC1			OFF	
MB91F522KWCPMC1		ON	ON	
MB91F522KYCPMC1			OFF	
MB91F522KJCPMC1		OFF	ON	
MB91F522KLCPMC1			OFF	
MB91F526KSCPMC1	None	ON	ON	
MB91F526KUCPMC1			OFF	
MB91F526KHCPMC1		OFF	ON	
MB91F526KKCPMC1			OFF	
MB91F525KSCPMC1		ON	ON	
MB91F525KUCPMC1			OFF	
MB91F525KHCPMC1		OFF	ON	
MB91F525KKCPMC1			OFF	
MB91F524KSCPMC1		ON	ON	
MB91F524KUCPMC1			OFF	
MB91F524KHCPMC1		OFF	ON	
MB91F524KKCPMC1			OFF	
MB91F523KSCPMC1		ON	ON	
MB91F523KUCPMC1			OFF	
MB91F523KHCPMC1		OFF	ON	
MB91F523KKCPMC1			OFF	
MB91F522KSCPMC1		ON	ON	
MB91F522KUCPMC1			OFF	
MB91F522KHCPMC1		OFF	ON	
MB91F522KKCPMC1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526BWDPMC1	Yes	ON	ON	LQD • 64 pin, Plastic
MB91F526BJDPMC1		OFF	ON	
MB91F525BWDPMC1		ON	ON	
MB91F525BJDPMC1		OFF	ON	
MB91F524BWDPMC1		ON	ON	
MB91F524BJDPMC1		OFF	ON	
MB91F523BWDPMC1		ON	ON	
MB91F523BJDPMC1		OFF	ON	
MB91F522BWDPMC1		ON	ON	
MB91F522BJDPMC1		OFF	ON	
MB91F526BSDPMC1	None	ON	ON	
MB91F526BHDPHC1		OFF	ON	
MB91F525BSDPMC1		ON	ON	
MB91F525BHDPHC1		OFF	ON	
MB91F524BSDPMC1		ON	ON	
MB91F524BHDPHC1		OFF	ON	
MB91F523BSDPMC1		ON	ON	
MB91F523BHDPHC1		OFF	ON	
MB91F522BSDPMC1		ON	ON	
MB91F522BHDPHC1		OFF	ON	

*: For details of the package, see "■ PACKAGE DIMENSIONS".

LQI100 , 100 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQI100		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	0.20	0.25
c	0.09	—	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
e	0.50 BSC.		
E	16.00 BSC.		
E1	14.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	100		

NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

■ Workaround

It is necessary to satisfy the below both conditions of (1) and (2).

- (1) Interrupt levels that are used as sources for recovering from the watch mode (power off) are '31', before CPU state changes to the watch mode (power off)
- (2) Don't use NMIX pin as source for recovering from the watch mode (power off)

■ Fix Status

Will not be planned

Page	Section	Change Results						
20	■PIN Description	(Continued) (Correct)						
		Pin no.						Pin Name
		64	80	100	120	144	176	
		-	-	4 ^{*1}	7 ^{*1}	10	12	P025
								WR1X ^{*4, *5}
								SOT4_1
								PPG25_0
								TIN2_0
		-	-	-	-	-	13	P172
								PPG38_1
		-	4 ^{*1}	5 ^{*1}	8 ^{*1}	11	14	P026
								A00 ^{*3, *4, *5}
								SCK4_1
								PPG26_0
								TIN3_0
		4 ^{*1}	5 ^{*1}	6 ^{*1}	9 ^{*1}	12	15	P027
								A01 ^{*2, *3, *4, *5}
								SCS40_1
								PPG27_0
								TOT0_0
		-	-	-	-	-	16	RTO3_1
								P173
		-	-	7 ^{*1}	10 ^{*1}	13	17	PPG39_1
								P030
								A02 ^{*4, *5}
								SCS41_1
								PPG28_0
		-	6 ^{*1}	8 ^{*1}	11 ^{*1}	14	18	TOT1_0
								P031
								A03 ^{*3, *4, *5}
								SCS42_1
								PPG29_0
		5 ^{*1}	7 ^{*1}	9 ^{*1}	12 ^{*1}	15	19	TOT2_0 ^{*3}
								P032
								A04 ^{*2, *3, *4, *5}
								SCS43_1
								PPG30_0
		6 ^{*1}	8 ^{*1}	10 ^{*1}	13 ^{*1}	16	20	TOT3_0
								RTO2_1
								P033
A05 ^{*2, *3, *4, *5}								
PPG31_0								
ICU3_3								
TIN4_0								
RTO1_1								
						SCK3_2		

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
				(4-1-5)SCK$\uparrow$$\RightarrowSCS\uparrow$hold time t_{CSHI} (4-1-6)SCK$\downarrow$$\RightarrowSCS\uparrow$hold time t_{CSHI} (4-1-7)SCK$\uparrow$$\RightarrowSCS\downarrow$hold time t_{CSHI} (4-1-8)SCK$\downarrow$$\RightarrowSCS\downarrow$hold time t_{CSHI} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSHD}-50$ Max $t_{CSHD}+0$ ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $t_{CSHD}-10$ Max $t_{CSHD}+50$ Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $t_{CSHD}-300$ Max $t_{CSHD}+50$ (4-1-5),(4-1-6)SCS$\downarrow$$\Rightarrow$SOT delay time t_{DSE} (4-1-7),(4-1-8)SCS$\uparrow$$\Rightarrow$SOT delay time t_{DSE} Corrected the following description. Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 SOT1 to SOT11 Value: Min - Max 40 ↓ Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73, SCS8 to SCS11 SOT1,SOT2,SOT5 to SOT11 Value: Min - Max 40 Pin name: SCS3,SCS40 to SCS43 SOT3,SOT4 Value: Min - Max 300 (4-1-5)SCK$\downarrow$$\RightarrowSCS\downarrow$ clock switch time t_{SCC} (4-1-6)SCK$\uparrow$$\RightarrowSCS\downarrow$ clock switch time t_{SCC} (4-1-7)SCK$\downarrow$$\RightarrowSCS\uparrow$ clock switch time t_{SCC} (4-1-8)SCK$\uparrow$$\RightarrowSCS\uparrow$ clock switch time t_{SCC} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $3t_{CPP}+0$ Max $3t_{CPP}+50$ ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min $3t_{CPP}-10$ Max $3t_{CPP}+50$ Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min $3t_{CPP}-300$ Max $3t_{CPP}+50$ Added the following description. Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again Electrical Characteristics 5.A/D Converter