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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526djbpmc-gs-f4e1

1. Product Lineup

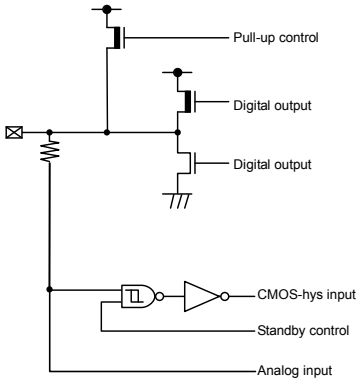
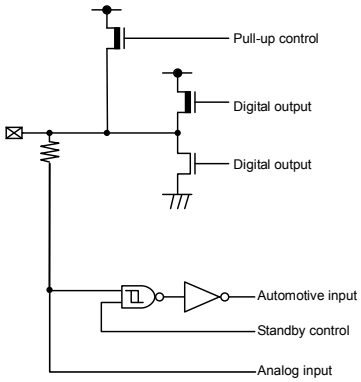
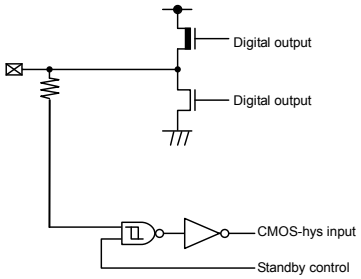
Product lineup comparison 64 pins

	MB91F522B	MB91F523B	MB91F524B	MB91F525B	MB91F526B
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	None				
Free-run Timer	16bit×3ch, 32bit×1ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×21ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×13ch (1unit), 12bit×13ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	8ch[*1]				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	44 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
NMI request function	Yes				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V [*2]				
Package	LQD064				

*1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

*1: There is a restriction of pin functions. See "Pin Name" of this table.
*2: not supported in 64pin
*3: not supported in 80pin
*4: not supported in 100pin
*5: not supported in 120pin
*6: not supported in 144pin
*7: not supported in 176pin
*8: For the I/O circuit types, see "I/O CIRCUIT TYPE".
*9: For switching, see "I/O Port" in HARDWARE MANUAL.

Type	Circuit	Remarks
G		•Analog input, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ • CMOS hysteresis input
H		•Analog input, General-purpose I/O port •Output 12mA •Pull-up resistor control 50kΩ •Automotive input
I		• General-purpose I/O port (5V tolerant) • Output 4mA • CMOS hysteresis input

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

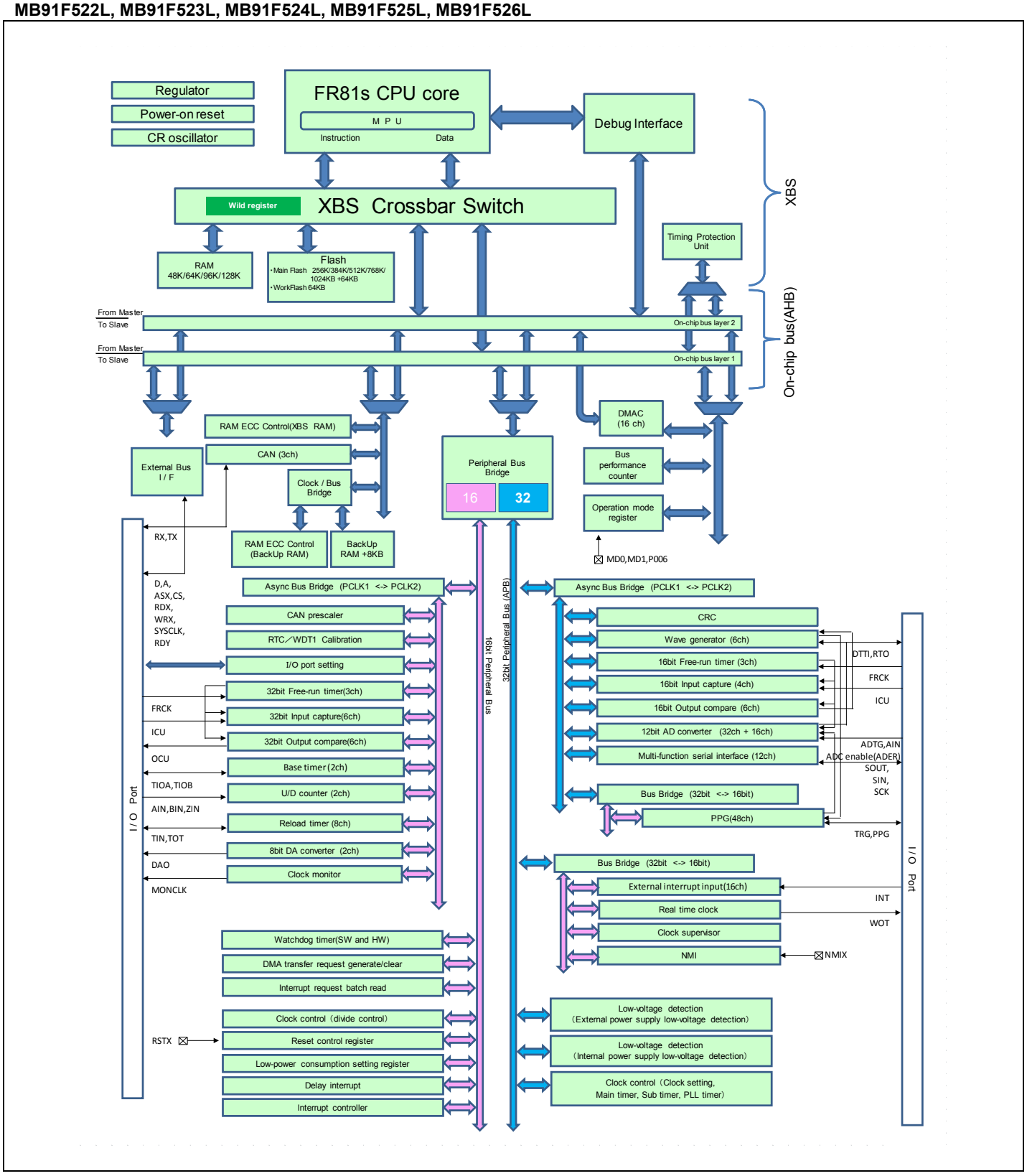
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00059C$_H$ to 0005BC$_H$	—	—	—	—	Reserved
0005C0$_H$ to 0005FC$_H$	—	—	—	—	Reserved
000600$_H$	ASR0 [R/W] W 00000000 00000000 -------- 1111-001				External Bus Interface [S]
000604$_H$	ASR1 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608$_H$	ASR2 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
00060C$_H$	ASR3 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610$_H$ to 00063C$_H$	—	—	—	—	Reserved [S]
000640$_H$	ACR0 [R/W] W -------- -------- -------- 01--00--				External Bus Interface [S]
000644$_H$	ACR1 [R/W] W -------- -------- -------- XX--XX--				
000648$_H$	ACR2 [R/W] W -------- -------- -------- XX--XX--				
00064C$_H$	ACR3 [R/W] W -------- -------- -------- XX--XX--				
000650$_H$ to 00067C$_H$	—	—	—	—	Reserved [S]
000680$_H$	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External Bus Interface [S]
000684$_H$	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688$_H$	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				External Bus Interface [S]
00068C$_H$	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690$_H$ to 0006FC$_H$	—	—	—	—	Reserved [S]
000700$_H$ to 00070C$_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001804_H	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001808_H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
$00180C_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810_H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814_H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818_H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00181C_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820_H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824_H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828_H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
$00182C_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830_H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834_H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838_H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
$00183C_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001B78_H$	PCN216 [R/W] B,H,W --000000 -----110		PSDR16 [R/W] H,W 00000000 00000000		PPG16
$001B7C_H$	PTPC16 [R/W] H,W 00000000 00000000		—	—	
$001B80_H$	PCN17 [R/W] B,H,W 00000000 000000-0		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
$001B84_H$	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PTMR17 [R] H,W 11111111 11111111		
$001B88_H$	PCN217 [R/W] B,H,W --000000 -----110		PSDR17 [R/W] H,W 00000000 00000000		
$001B8C_H$	PTPC17 [R/W] H,W 00000000 00000000		—	—	
$001B90_H$	PCN18 [R/W] B,H,W 00000000 000000-0		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
$001B94_H$	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PTMR18 [R] H,W 11111111 11111111		
$001B98_H$	PCN218 [R/W] B,H,W --000000 -----110		PSDR18 [R/W] H,W 00000000 00000000		
$001B9C_H$	PTPC18 [R/W] H,W 00000000 00000000		—	—	
$001BA0_H$	PCN19 [R/W] B,H,W 00000000 000000-0		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
$001BA4_H$	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PTMR19 [R] H,W 11111111 11111111		
$001BA8_H$	PCN219 [R/W] B,H,W --000000 -----110		PSDR19 [R/W] H,W 00000000 00000000		
$001BAC_H$	PTPC19 [R/W] H,W 00000000 00000000		—	—	
$001BB0_H$	PCN20 [R/W] B,H,W 00000000 000000-0		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
$001BB4_H$	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PTMR20 [R] H,W 11111111 11111111		
$001BB8_H$	PCN220 [R/W] B,H,W --000000 -----110		PSDR20 [R/W] H,W 00000000 00000000		
$001BBC_H$	PTPC20 [R/W] H,W 00000000 00000000		—	—	
$001BC0_H$	PCN21 [R/W] B,H,W 00000000 000000-0		PCSR21 [W] H,W XXXXXXXX XXXXXXXX		PPG21
$001BC4_H$	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PTMR21 [R] H,W 11111111 11111111		
$001BC8_H$	PCN221 [R/W] B,H,W --000000 -----110		PSDR21 [R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0020BC$_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0$_H$ to 0020FC$_H$	—				
002100$_H$	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002104$_H$	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108$_H$	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
00210C$_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110$_H$	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114$_H$	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118$_H$	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C$_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120$_H$	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124$_H$	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128$_H$	—	—	—	—	
00212C$_H$	—	—	—	—	
002130$_H$, 002134$_H$	Reserved (IF1 data mirror)				CAN1 (64msb)
002138$_H$	—	—	—	—	
00213C$_H$	—	—	—	—	
002140$_H$	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144$_H$	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148$_H$	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C$_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				RAM/ diagnosis Backup RAM
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W ------00 00001100		RAM/ diagnosis Backup RAM
003044_H	TSRCRA [R/W] B,H,W 0-------	—	—	TKCCRA [R/W] B,H,W 00----00	
003048_H to $0030FC_H$	—				Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		BUS diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114_H	—	—	BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
$00311C_H$	—	—	—	—	
003120_H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128_H to $003FFC_H$	—				Reserved
004000_H to $005FFC_H$	Backup-RAM				Backup RAM area

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
32-bit ICU5 (fetching/measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
- -	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3 , SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

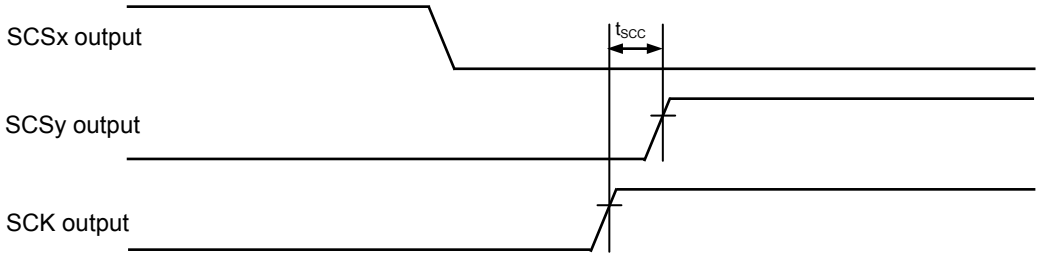
Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.

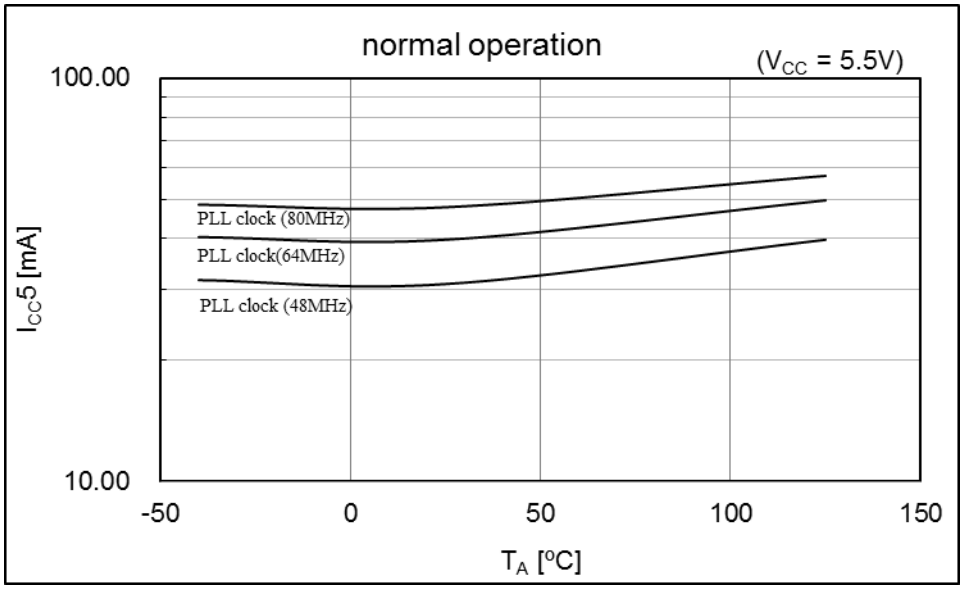


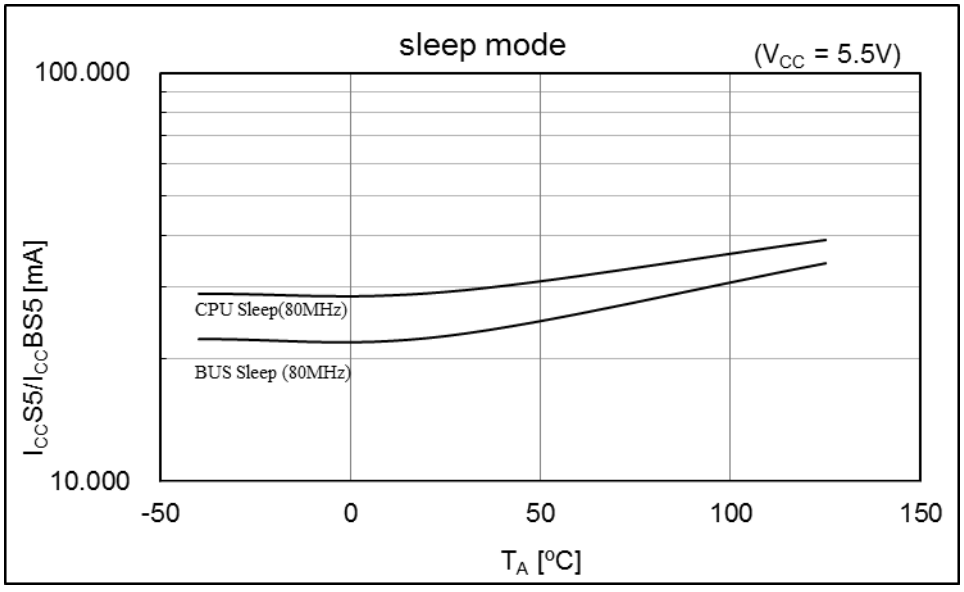
When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

12. EXAMPLE CHARACTERISTICS

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

MB91F526





Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526FWBPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FYBPMC			OFF	
MB91F526FJBPMC		OFF	ON	
MB91F526FLBPMC			OFF	
MB91F525FWBPMC		ON	ON	
MB91F525FYBPMC			OFF	
MB91F525FJBPMC		OFF	ON	
MB91F525FLBPMC			OFF	
MB91F524FWBPMC		ON	ON	
MB91F524FYBPMC			OFF	
MB91F524FJBPMC		OFF	ON	
MB91F524FLBPMC			OFF	
MB91F523FWBPMC		ON	ON	
MB91F523FYBPMC			OFF	
MB91F523FJBPMC		OFF	ON	
MB91F523FLBPMC			OFF	
MB91F522FWBPMC		ON	ON	
MB91F522FYBPMC			OFF	
MB91F522FJBPMC		OFF	ON	
MB91F522FLBPMC			OFF	
MB91F526FSBPMC	None	ON	ON	
MB91F526FUBPMC			OFF	
MB91F526FHBPMC		OFF	ON	
MB91F526FKBPMC			OFF	
MB91F525FSBPMC		ON	ON	
MB91F525FUBPMC			OFF	
MB91F525FHBPMC		OFF	ON	
MB91F525FKBPMC			OFF	
MB91F524FSBPMC		ON	ON	
MB91F524FUBPMC			OFF	
MB91F524FHBPMC		OFF	ON	
MB91F524FKBPMC			OFF	
MB91F523FSBPMC		ON	ON	
MB91F523FUBPMC			OFF	
MB91F523FHBPMC		OFF	ON	
MB91F523FKBPMC			OFF	
MB91F522FSBPMC		ON	ON	
MB91F522FUBPMC			OFF	
MB91F522FHBPMC		OFF	ON	
MB91F522FKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526JWCPMC	Yes	ON	ON	LQM・120 pin, Plastic
MB91F526JYCPMC			OFF	
MB91F526JJCPMC		OFF	ON	
MB91F526JLCPMC			OFF	
MB91F525JWCPMC		ON	ON	
MB91F525JYCPMC			OFF	
MB91F525JJCPMC		OFF	ON	
MB91F525JLCPMC			OFF	
MB91F524JWCPMC		ON	ON	
MB91F524JYCPMC			OFF	
MB91F524JJCPMC		OFF	ON	
MB91F524JLCPMC			OFF	
MB91F523JWCPMC		ON	ON	
MB91F523JYCPMC			OFF	
MB91F523JJCPMC		OFF	ON	
MB91F523JLCPMC			OFF	
MB91F522JWCPMC		ON	ON	
MB91F522JYCPMC			OFF	
MB91F522JJCPMC		OFF	ON	
MB91F522JLCPMC			OFF	
MB91F526JSCPMC	None	ON	ON	
MB91F526JUCPMC			OFF	
MB91F526JHCPMC		OFF	ON	
MB91F526JKCPMC			OFF	
MB91F525JSCPMC		ON	ON	
MB91F525JUCPMC			OFF	
MB91F525JHCPMC		OFF	ON	
MB91F525JKCPMC			OFF	
MB91F524JSCPMC		ON	ON	
MB91F524JUCPMC			OFF	
MB91F524JHCPMC		OFF	ON	
MB91F524JKCPMC			OFF	
MB91F523JSCPMC		ON	ON	
MB91F523JUCPMC			OFF	
MB91F523JHCPMC		OFF	ON	
MB91F523JKCPMC			OFF	
MB91F522JSCPMC		ON	ON	
MB91F522JUCPMC			OFF	
MB91F522JHCPMC		OFF	ON	
MB91F522JKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526BWEPMC1	Yes	ON	ON	LQE・64 pin, Plastic
MB91F526BJEPMC1		OFF	ON	
MB91F525BWEPMC1		ON	ON	
MB91F525BJEPMC1		OFF	ON	
MB91F524BWEPMC1		ON	ON	
MB91F524BJEPMC1		OFF	ON	
MB91F523BWEPMC1		ON	ON	
MB91F523BJEPMC1		OFF	ON	
MB91F522BWEPMC1		ON	ON	
MB91F522BJEPMC1		OFF	ON	
MB91F526BSEPMC1	None	ON	ON	
MB91F526BHEPMC1		OFF	ON	
MB91F525BSEPMC1		ON	ON	
MB91F525BHEPMC1		OFF	ON	
MB91F524BSEPMC1		ON	ON	
MB91F524BHEPMC1		OFF	ON	
MB91F523BSEPMC1		ON	ON	
MB91F523BHEPMC1		OFF	ON	
MB91F522BSEPMC1		ON	ON	
MB91F522BHEPMC1		OFF	ON	

*: For details of the package, see "■ PACKAGE DIMENSIONS ".

19. Major Changes

Spansion Publication Number: MB91F526L_DS705-00011

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
3	■FEATURES	Corrected the following description. 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input ↓ 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
33 to 36	■I/O CIRCUIT TYPE	Corrected the following description to "Type F, G, I, J, K, M". Schmitt input → CMOS hysteresis input Corrected the following description to "Type D, E". I^2C Schmitt input → I^2C hysteresis input
44 to 49	■BLOCK DIAGRAM	Corrected the following description. ●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B ●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D ●MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F ●MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J ●MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K ●MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L
138	■ELECTRICAL CHARACTERISTICS 2. Recommended operating conditions	Added the following description. *1 : When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset
139,140	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of "ICCT5 When using sub clock 32kHz TA=+25°C ". Max 1420μA → Max 2000μA
139	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of "Power supply voltage range". (TA:-40°C to +105°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V) ↓ (T_A:-40°C to +105°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)
140,141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of "Power supply voltage range". (T_A:-40°C to +125°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V) ↓ (T_A:-40°C to +125°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)
141	■ELECTRICAL CHARACTERISTICS 3.DC characteristics	Corrected the value of " Pull-up resistance R_{UP1}". Vcc=3.3V±0.3V Min 49 Max 140 →Min 45 Max 140

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>34, 35</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">113</td><td rowspan="4">133</td><td rowspan="4">161</td><td>P002</td></tr>
<tr><td>D18</td></tr>
<tr><td>SCK1_0</td></tr>
<tr><td>TIOB0_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">76</td><td rowspan="5">96</td><td rowspan="5">114</td><td rowspan="5">134</td><td rowspan="5">162</td><td>P003</td></tr>
<tr><td>D19</td></tr>
<tr><td>SIN2_0</td></tr>
<tr><td>TIOB1_1</td></tr>
<tr><td>INT3_0</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">135</td><td rowspan="3">163</td><td>P004</td></tr>
<tr><td>D20</td></tr>
<tr><td>SOT2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">164</td><td>P164</td></tr>
<tr><td>PPG32_1</td></tr>
<tr><td rowspan="6">61</td><td rowspan="6">77</td><td rowspan="6">97</td><td rowspan="6">115</td><td rowspan="6">136</td><td rowspan="6">165</td><td>P005</td></tr>
<tr><td>D21</td></tr>
<tr><td>SCK2_0</td></tr>
<tr><td>ADTG0_1</td></tr>
<tr><td>INT7_1</td></tr>
<tr><td>(RX2(64))</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">166</td><td>P165</td></tr>
<tr><td>PPG33_1</td></tr>
<tr><td rowspan="6">62</td><td rowspan="6">78</td><td rowspan="6">98</td><td rowspan="6">116</td><td rowspan="6">137</td><td rowspan="6">167</td><td>P006</td></tr>
<tr><td>D22</td></tr>
<tr><td>SCS2_0</td></tr>
<tr><td>ADTG1_1</td></tr>
<tr><td>INT2_1</td></tr>
<tr><td>(TX2(64))</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">117</td><td rowspan="2">138</td><td rowspan="2">168</td><td>P007</td></tr>
<tr><td>D23</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">169</td><td>P166</td></tr>
<tr><td>PPG34_1</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">118</td><td rowspan="2">139</td><td rowspan="2">170</td><td>P010</td></tr>
<tr><td>D24</td></tr>
<tr><td rowspan="6">63</td><td rowspan="6">79</td><td rowspan="6">99</td><td rowspan="6">119</td><td rowspan="6">140</td><td rowspan="6">171</td><td>P011</td></tr>
<tr><td>WOT</td></tr>
<tr><td>D25</td></tr>
<tr><td>SOT2_1</td></tr>
<tr><td>TIOA0_0</td></tr>
<tr><td>INT3_1</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>131</td><td>■Interrupt Vector Table</td><td>"42" is deleted as shown below from the interrupt factor in Interrupt vector 120pin.

(Error)
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/42/43
16-bit free-run timer 2 (0 detection) / (compare clear)</td><td>41</td><td>29</td><td>ICR 25</td><td>358 H</td><td>000F FF58 H</td><td>25 *3</td></tr>
</table>

(Correct)
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/43
16-bit free-run timer 2 (0 detection) / (compare clear)</td><td>41</td><td>29</td><td>ICR 25</td><td>358 H</td><td>000F FF58 H</td><td>25 *3</td></tr>
</table>
</td></tr>
<tr><td>133</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 120pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0
Base timer 1 IRQ1
–
–</td><td>61</td><td>3D</td><td>ICR 45</td><td>308 H</td><td>000F FF08 H</td><td>45 *5</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0
Base timer 1 IRQ1
–
–</td><td>61</td><td>3D</td><td>ICR 45</td><td>308 H</td><td>000F FF08 H</td><td>45</td></tr>
</table>
</td></tr>
<tr><td>133</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 120pins.

(Error)
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>