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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526dsbpmc-gte2

Product lineup comparison 144 pins

	MB91F522K	MB91F523K	MB91F524K	MB91F525K	MB91F526K
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	Yes				
DMA Transfer	16ch				
16-bit Base Timer	2ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×44ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×32ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch*1				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	120 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V *2				
Package	LQS144, LQN144				

*1: Only channel 3 and channel 4 support the I^2C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	40	46	54	68	P070	-	A	General-purpose I/O port
						ICU0_2	-		Input capture ch.0 input (2)
26	33	41	47	55	69	P071	-	G	General-purpose I/O port
						SCK4_2	-		Multi-function serial ch.4 clock I/O (2)
						AN35	-		ADC analog 35 input
						ICU1_2	-		Input capture ch.1 input (2)
						MONCLK	-		Clock monitor output pin
27	34	42	48	56	70	P072	-	G	General-purpose I/O port
						SIN4_0	-		Multi-function serial ch.4 serial data input (0)
						AN34	-		ADC analog 34 input
						ICU2_2	-		Input capture ch.2 input (2)
						INT5_0	-		INT5 External interrupt input (0)
-	35 *3	43 *4	49	57	71	P073	-	D	General-purpose I/O port
						SOT4_0/ SDA4 *3, *4	-		Multi-function serial ch.4 serial data output (0)/I^{2}C bus serial data I/O
						AN33	-		ADC analog 33 input
						ICU3_2	-		Input capture ch.3 input (2)
-	-	-	-	-	72	P186	-	A	General-purpose I/O port
						PPG46_0	-		PPG ch.46 output (0)
-	-	-	-	-	73	P187	-	A	General-purpose I/O port
						PPG47_0	-		PPG ch.47 output (0)
-	-	-	50	58	74	P074	-	E	General-purpose I/O port
						SCK4_0/ SCL4	-		Multi-function serial ch.4 clock I/O (0)/ I^{2}C bus serial clock I/O
-	-	-	51	59	75	P075	-	F	General-purpose I/O port
						SIN3_0	-		Multi-function serial ch.3 serial data input (0)
						INT4_0	-		INT4 External interrupt input (0)
-	-	-	52	60	76	P076	-	E	General-purpose I/O port
						SOT3_0/ SDA3	-		Multi-function serial ch.3 serial data output (0)/I^{2}C bus serial data I/O
-	-	-	53	61	77	P077	-	E	General-purpose I/O port
						SCK3_0/ SCL3	-		Multi-function serial ch.3 clock I/O (0)/ I^{2}C bus serial clock I/O
-	-	44	54	62	78	P152	-	A	General-purpose I/O port
						SCS53_0	-		Serial chip select 53 output (0)
28	36	45	55	63	79	P153	-	G	General-purpose I/O port
						SCK5_0/ SCL5	-		Multi-function serial ch.5 clock I/O (0)/ I^{2}C bus serial clock I/O
						AN32	-		ADC analog 32 input
						FRCK1_1	-		Free-run timer 1 clock input (1)
						INT4_1	-		INT4 External interrupt input (1)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	80	96	115	141	P130	-	F	General-purpose I/O port
						SCK0_0	-		Multi-function serial ch.0 clock I/O (0)
-	-	-	-	-	142	P162	-	A	General-purpose I/O port
						TRG5_2	-		PPG trigger 5 input (2)
-	-	-	-	-	143	P163	-	A	General-purpose I/O port
						TRG6_2	-		PPG trigger 6 input (2)
51	65	81	97	116	144	MD0	-	K	Mode pin 0
52	66	82	98	117	145	MD1	-	K	Mode pin 1
53	67	83	99	118	146	X0	-	N	Main clock oscillation input
54	68	84	100	119	147	X1	-	N	Main clock oscillation output
56	70	86	102	121	149	P135	-	A	General-purpose I/O port
						DTTI_0	-		Waveform generator ch.0-ch.5 input pin (0)
						X1A	-	O	Sub clock oscillation output
57	71	87	103	122	150	P136	-	A	General-purpose I/O port
						X0A	-	O	Sub clock oscillation input
58	72	88	104	123	151	RSTX	N	M	External reset input
-	-	-	-	124	152	P131	-	A	General-purpose I/O port
						ADTG0_0	-		A/D converter external trigger input 0 (0)
-	-	-	105	125	153	P132	-	A	General-purpose I/O port
						SCS1_0	-		Serial chip select 1 I/O (0)
						ADTG1_0	-		A/D converter external trigger input 1 (0)
-	-	89	106	126	154	P133	-	A	General-purpose I/O port
						TX2(64)	-		CAN transmission data 2 output
-	-	90	107	127	155	P134	-	F	General-purpose I/O port
						RX2(64)	-		CAN reception data 2 input
						SCS1_1	-		Serial chip select 1 I/O (1)
						ICU7_0	-		Input capture ch.7 input (0)
						INT7_0	-		INT7 External interrupt input (0)
-	-	91	108	128	156	P144	-	F	General-purpose I/O port
						SCK1_1	-		Multi-function serial ch.1 clock I/O (1)
-	-	94 *1	111 *1	131	159	P000	-	F	General-purpose I/O port
						D16 *4, *5	-		External bus data bit16 I/O (0)
						SIN1_0	-		Multi-function serial ch.1 serial data input (0)
						TIOA0_1 *4	-		TIOA output of Base timer ch.0 (1)
						INT2_0	-		INT2 External interrupt input (0)
-	75 *1	95 *1	112 *1	132	160	P001	-	A	General-purpose I/O port
						D17 *3, *4, *5	-		External bus data bit17 I/O
						SOT1_0 *3	-		Multi-function serial ch.1 serial data output (0)
						TIOA1_1	-		TIOA I/O of Base timer ch.1 (1)

- Notes When Writing Data in a Register Having the Status Flag
  When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

  The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

  Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

  Note: These points can be ignored because the bit instructions are already taken the points into consideration.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000710_H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter
000714_H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720_H to $0007F8_H$	—	—	—	—	Reserved
$0007FC_H$	BMODR [R] B, H, W XXXXXXXX	—	—	—	Mode Register
000800_H to $00083C_H$	—	—	—	—	Reserved [S]
000840_H	FCTLR [R/W] H -0--1000 0--0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]
000844_H to 000854_H	—	—	—	—	Reserved [S]
000858_H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]
$00085C_H$ to $00087C_H$	—	—	—	—	Reserved [S]
000880_H	WRAR00 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000884_H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000894_H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CA0_H$	DCCR10 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000CA4_H$	DCSR10 [R/W] H 0------- -----000		DTCR10 [R/W] H 00000000 00000000		
$000CA8_H$	DSAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CAC_H$	DDAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CB0_H$	DCCR11 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CB4_H$	DCSR11 [R/W] H 0------- -----000		DTCR11 [R/W] H 00000000 00000000		
$000CB8_H$	DSAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CBC_H$	DDAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CC0_H$	DCCR12 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CC4_H$	DCSR12 [R/W] H 0------- -----000		DTCR12 [R/W] H 00000000 00000000		
$000CC8_H$	DSAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CCC_H$	DDAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CD0_H$	DCCR13 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CD4_H$	DCSR13 [R/W] H 0------- -----000		DTCR13 [R/W] H 00000000 00000000		
$000CD8_H$	DSAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CDC_H$	DDAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CE0_H$	DCCR14 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CE4_H$	DCSR14 [R/W] H 0------- -----000		DTCR14 [R/W] H 00000000 00000000		
$000CE8_H$	DSAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CEC_H$	DDAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000FD0_H$	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 32-bit ICU
$000FD4_H$	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FD8_H$	—	—	LSYNS1 [R/W] B,H,W 00000000	ICS45 [R/W] B,H,W 00000000	
$000FDC_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 32-bit ICU
$000FE0_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FE4_H$	—	—	—	ICS67 [R/W] B,H,W 00000000	
$000FE8_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU
$000FEC_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FF0_H$	—	—	—	ICS89 [R/W] B,H,W 00000000	
$000FF4_H$	MSCY8 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU Cycle measurement data register 89
$000FF8_H$	MSCY9 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FFC_H$	—	—	MSCH89 [R] B,H,W 00000000	MSCL89 [R/W] B,H,W ------00	Cycle and pulse width measurement control 89
001000_H	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Clock Control
001004_H to $00112C_H$	—	—	—	—	Reserved
001130_H	—	—	—	CRCCR [R/W] B,H,W -0000000	CRC calculation unit
001134_H	CRCINIT [R/W] B,H,W 11111111 11111111 11111111 11111111				
001138_H	CRCIN [R/W] B,H,W 00000000 00000000 00000000 00000000				
$00113C_H$	CRCR [R] B,H,W 11111111 11111111 11111111 11111111				
001140_H to $0011FC_H$	—	—	—	—	Reserved

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt vector
64 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*6
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*6
-	24	18	ICR08	$39C_H$	$000FFF9C_H$	-*6
-	25	19	ICR09	398_H	$000FFF98_H$	-*6
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

80 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*6
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*6
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

100 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*[1]
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31/40/41	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 6/7/16/17/26/27/36/37	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 8/9/18/19/28/29/38/39	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]

176 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

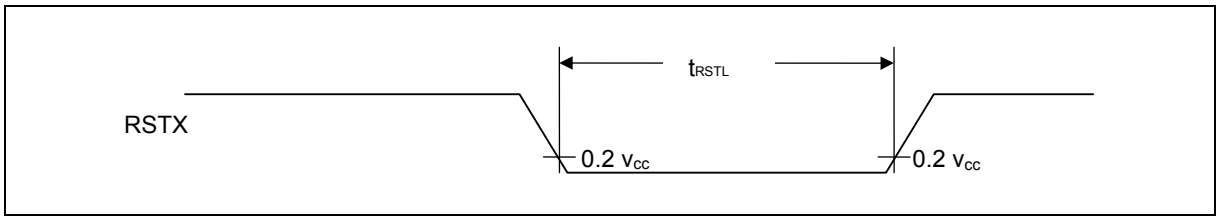
(2) Reset Input

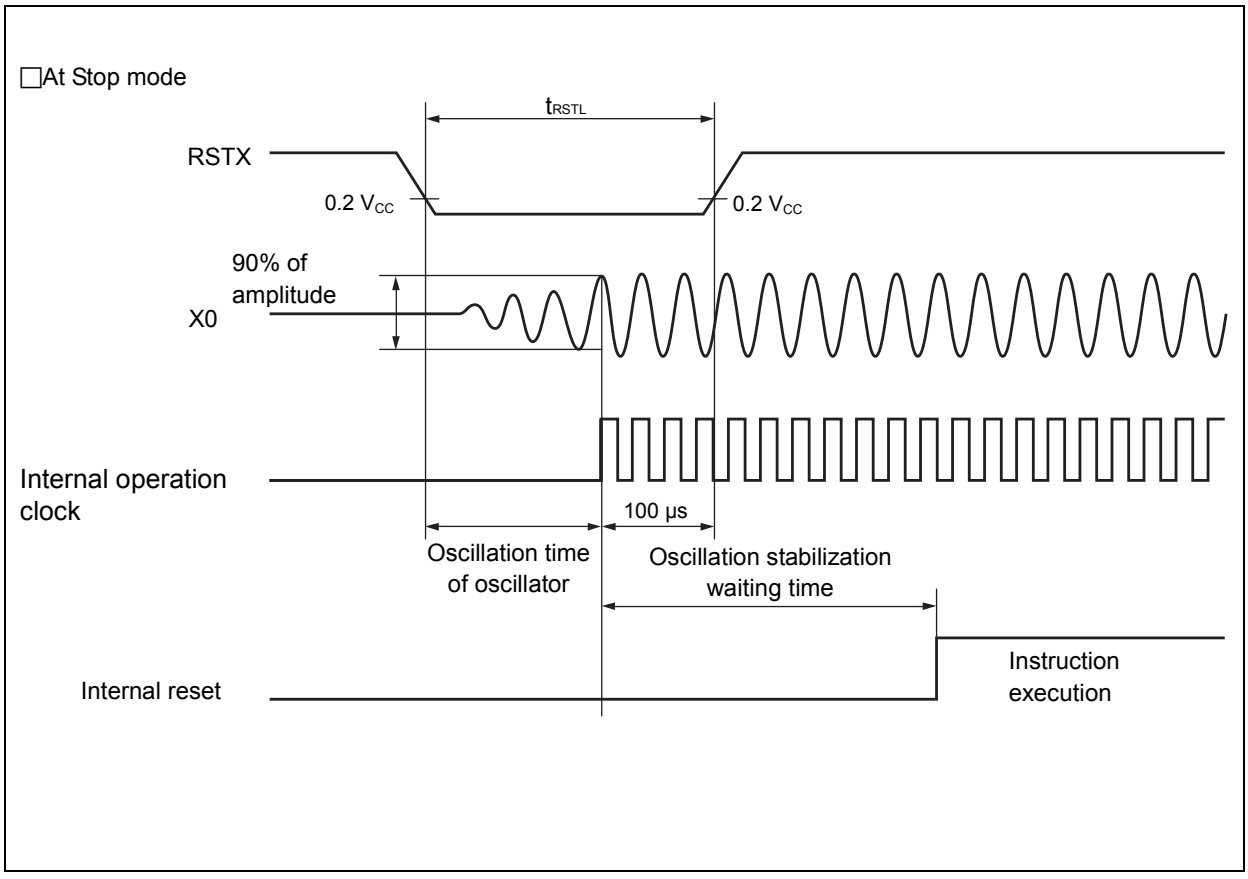
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator* +100	–	µs	At Stop mode At Power-on*2
				100	–	µs	At Watch mode
Width for reset input removal				1	–	µs	

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

*2: In case of using MB91F52xxxD or MB91F52xxxE and corresponding to note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.

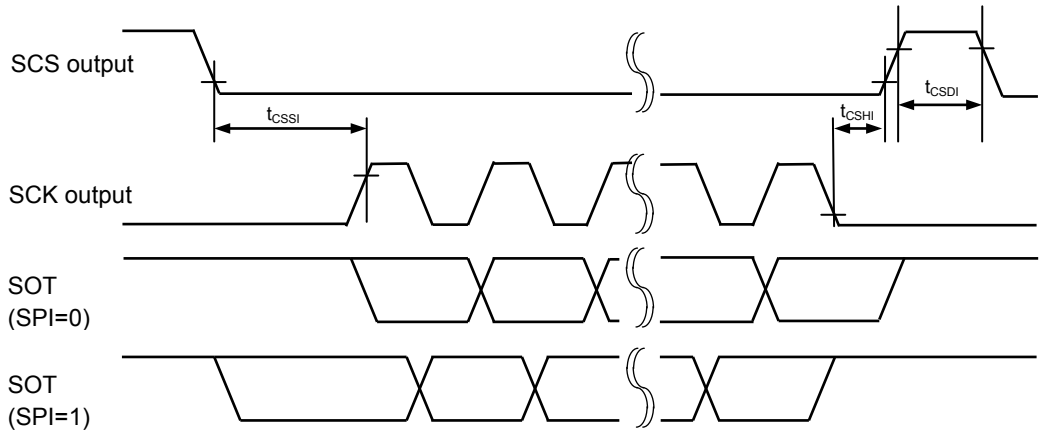




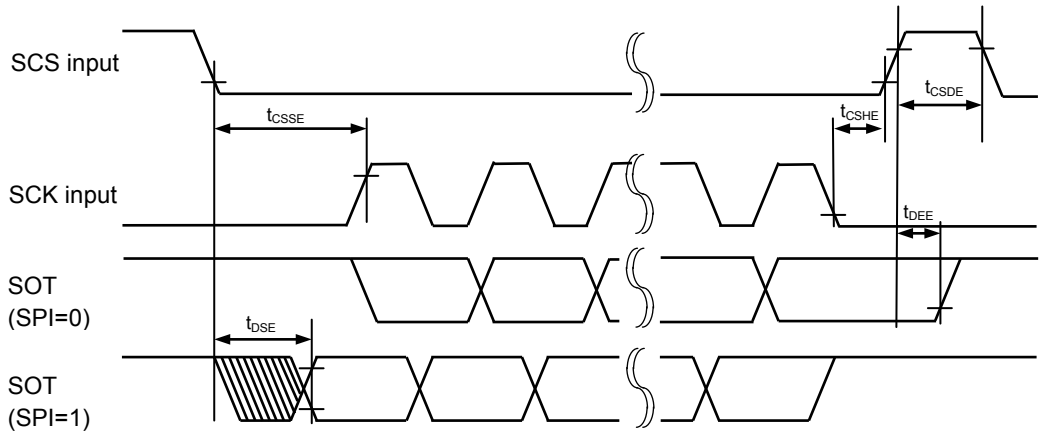
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2 , SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS↑→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↓ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock
*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock
*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3.

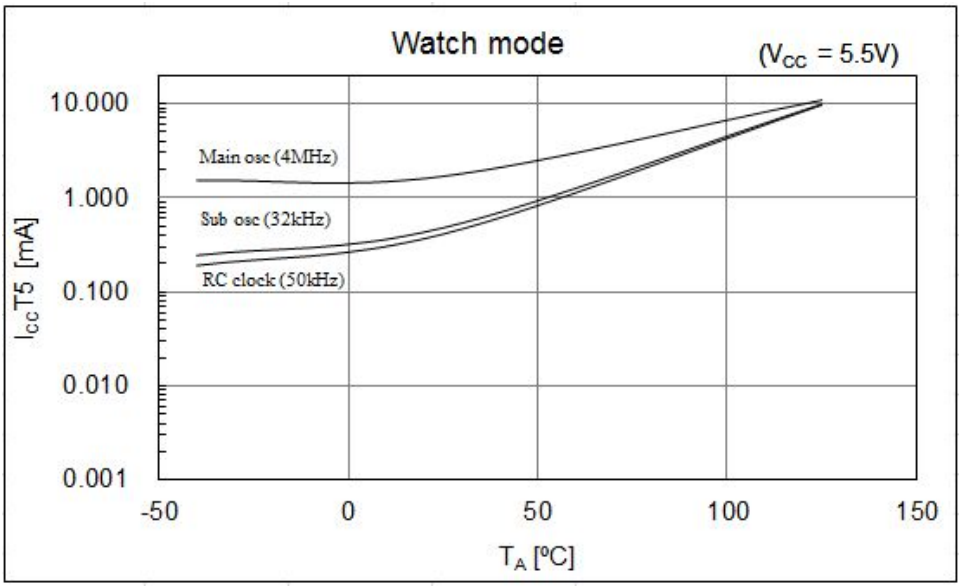


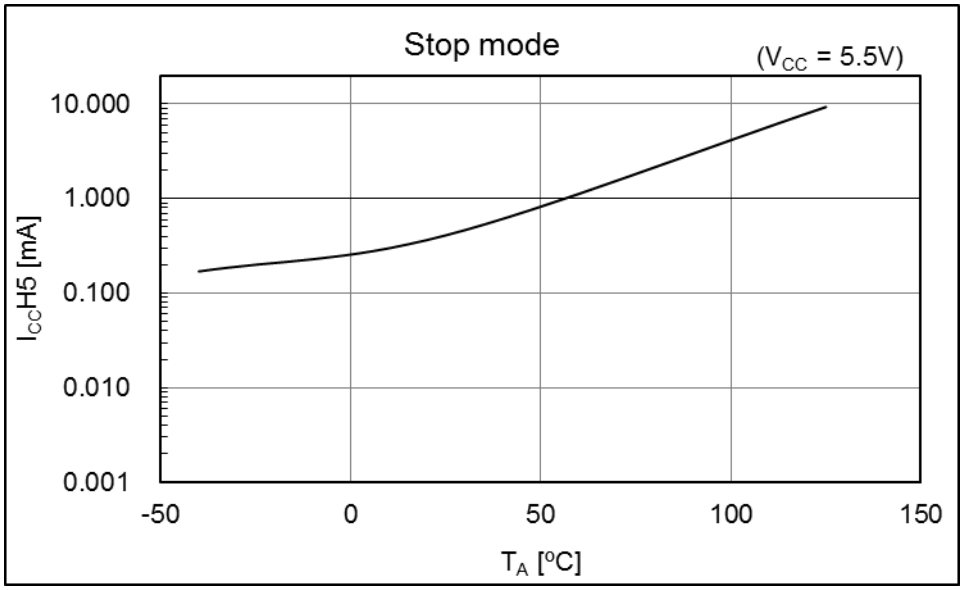
When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode



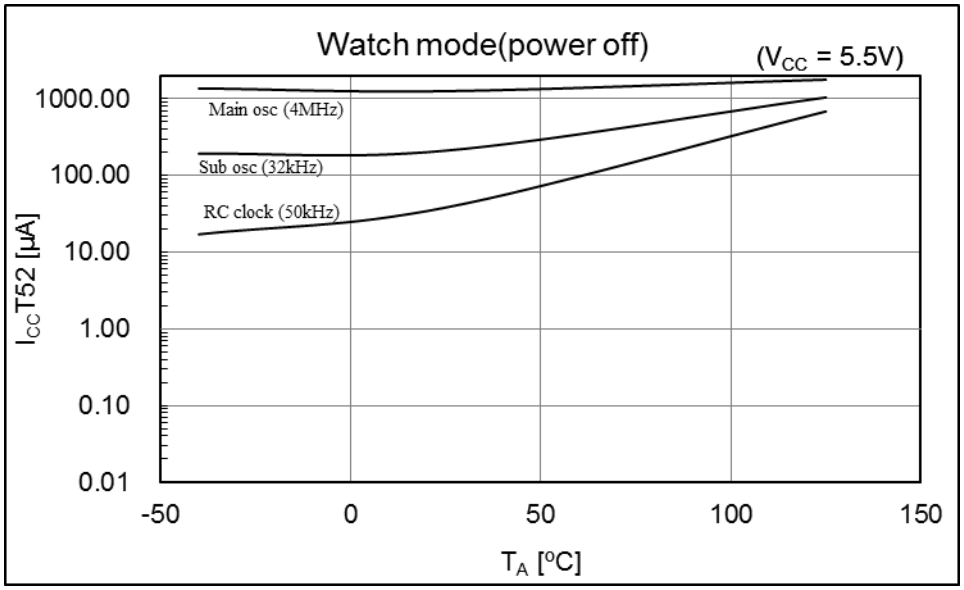
When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
External shift clock mode

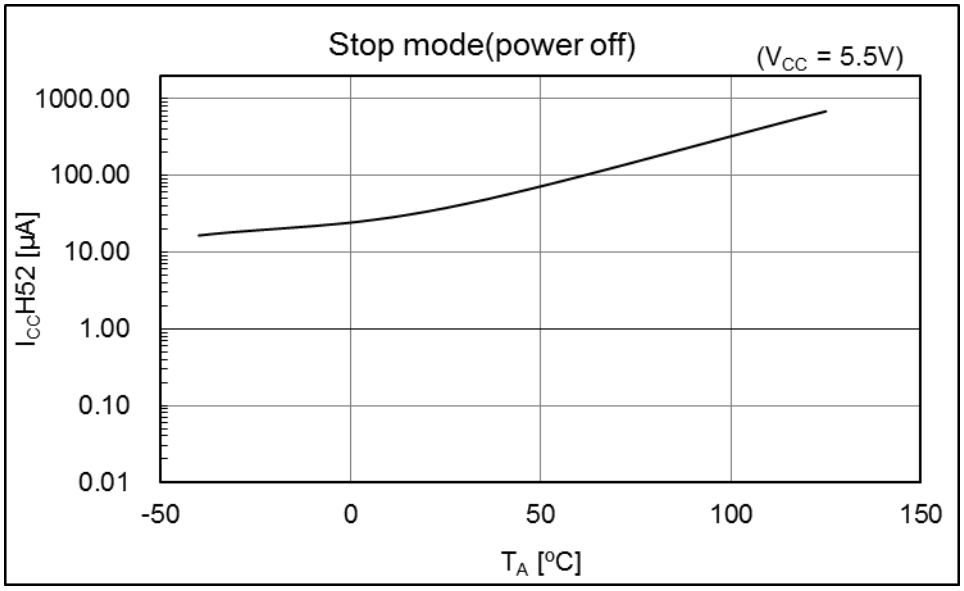
MB91F526


Watch mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC}T5 [mA]
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
-50
0
50
100
150
T_A [°C]


Stop mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC}H5 [mA]
-50
0
50
100
150
T_A [°C]

MB91F526


Watch mode(power off)
(V_{CC} = 5.5V)
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
1000.00
100.00
10.00
1.00
0.10
0.01
I_{CC}T52 [µA]
-50
0
50
100
150
T_A [°C]


Stop mode(power off)
(V_{CC} = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
I_{CC}H52 [µA]
-50
0
50
100
150
T_A [°C]

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWEPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FJEPMC		OFF	ON	
MB91F525FWEPMC		ON	ON	
MB91F525FJEPMC		OFF	ON	
MB91F524FWEPMC		ON	ON	
MB91F524FJEPMC		OFF	ON	
MB91F523FWEPMC		ON	ON	
MB91F523FJEPMC		OFF	ON	
MB91F522FWEPMC		ON	ON	
MB91F522FJEPMC		OFF	ON	
MB91F526FSEPMC	None	ON	ON	
MB91F526FHEPMC		OFF	ON	
MB91F525FSEPMC		ON	ON	
MB91F525FHEPMC		OFF	ON	
MB91F524FSEPMC		ON	ON	
MB91F524FHEPMC		OFF	ON	
MB91F523FSEPMC		ON	ON	
MB91F523FHEPMC		OFF	ON	
MB91F522FSEPMC		ON	ON	
MB91F522FHEPMC		OFF	ON	
MB91F526DWEPMC	Yes	ON	ON	LQH・80 pin, Plastic
MB91F526DJEPMC		OFF	ON	
MB91F525DWEPMC		ON	ON	
MB91F525DJEPMC		OFF	ON	
MB91F524DWEPMC		ON	ON	
MB91F524DJEPMC		OFF	ON	
MB91F523DWEPMC		ON	ON	
MB91F523DJEPMC		OFF	ON	
MB91F522DWEPMC		ON	ON	
MB91F522DJEPMC		OFF	ON	
MB91F526DSEPMC	None	ON	ON	
MB91F526DHEPMC		OFF	ON	
MB91F525DSEPMC		ON	ON	
MB91F525DHEPMC		OFF	ON	
MB91F524DSEPMC		ON	ON	
MB91F524DHEPMC		OFF	ON	
MB91F523DSEPMC		ON	ON	
MB91F523DHEPMC		OFF	ON	
MB91F522DSEPMC		ON	ON	
MB91F522DHEPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526BWEPMC1	Yes	ON	ON	LQE・64 pin, Plastic
MB91F526BJEPMC1		OFF	ON	
MB91F525BWEPMC1		ON	ON	
MB91F525BJEPMC1		OFF	ON	
MB91F524BWEPMC1		ON	ON	
MB91F524BJEPMC1		OFF	ON	
MB91F523BWEPMC1		ON	ON	
MB91F523BJEPMC1		OFF	ON	
MB91F522BWEPMC1		ON	ON	
MB91F522BJEPMC1		OFF	ON	
MB91F526BSEPMC1	None	ON	ON	
MB91F526BHEPMC1		OFF	ON	
MB91F525BSEPMC1		ON	ON	
MB91F525BHEPMC1		OFF	ON	
MB91F524BSEPMC1		ON	ON	
MB91F524BHEPMC1		OFF	ON	
MB91F523BSEPMC1		ON	ON	
MB91F523BHEPMC1		OFF	ON	
MB91F522BSEPMC1		ON	ON	
MB91F522BHEPMC1		OFF	ON	

*: For details of the package, see "■ PACKAGE DIMENSIONS ".

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>30</td><td>■PIN Description</td><td>
A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="4">-</td><td rowspan="4">48</td><td rowspan="4">59</td><td rowspan="4">69</td><td rowspan="4">85</td><td rowspan="4">104</td><td>P100</td></tr>
<tr><td>SCK7_0/ SCL7</td></tr>
<tr><td>AN12</td></tr>
<tr><td>PPG8_0</td></tr>
<tr><td colspan="6"></td><td></td></tr>
<tr><td rowspan="5">40</td><td rowspan="5">49</td><td rowspan="5">61</td><td rowspan="5">71</td><td rowspan="5">87</td><td rowspan="5">106</td><td>P102</td></tr>
<tr><td>SIN7_0</td></tr>
<tr><td>AN14</td></tr>
<tr><td>PPG10_0</td></tr>
<tr><td>INT10_0</td></tr>
<tr><td rowspan="4">41</td><td rowspan="4">50</td><td rowspan="4">62</td><td rowspan="4">72</td><td rowspan="4">88</td><td rowspan="4">107</td><td>P103</td></tr>
<tr><td>SCS73_0</td></tr>
<tr><td>AN15</td></tr>
<tr><td>PPG11_0</td></tr>
<tr><td rowspan="4">42</td><td rowspan="4">51</td><td rowspan="4">63</td><td rowspan="4">73</td><td rowspan="4">89</td><td rowspan="4">108</td><td>P104</td></tr>
<tr><td>SCS72_0</td></tr>
<tr><td>AN16</td></tr>
<tr><td>PPG12_0</td></tr>
<tr><td rowspan="4">43</td><td rowspan="4">52</td><td rowspan="4">64</td><td rowspan="4">74</td><td rowspan="4">90</td><td rowspan="4">109</td><td>P105</td></tr>
<tr><td>SCS71_0</td></tr>
<tr><td>AN17</td></tr>
<tr><td>PPG13_0</td></tr>
</table>
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="4">-</td><td rowspan="4">48*1</td><td rowspan="4">59</td><td rowspan="4">69</td><td rowspan="4">85</td><td rowspan="4">104</td><td>P100</td></tr>
<tr><td>SCK7_0/ SCL7*3</td></tr>
<tr><td>AN12</td></tr>
<tr><td>PPG8_0</td></tr>
<tr><td colspan="6"></td><td></td></tr>
<tr><td rowspan="5">40*1</td><td rowspan="5">49*1</td><td rowspan="5">61</td><td rowspan="5">71</td><td rowspan="5">87</td><td rowspan="5">106</td><td>P102</td></tr>
<tr><td>SIN7_0*2, *3</td></tr>
<tr><td>AN14</td></tr>
<tr><td>PPG10_0</td></tr>
<tr><td>INT10_0</td></tr>
<tr><td rowspan="4">41*1</td><td rowspan="4">50*1</td><td rowspan="4">62</td><td rowspan="4">72</td><td rowspan="4">88</td><td rowspan="4">107</td><td>P103</td></tr>
<tr><td>SCS73_0*2, *3</td></tr>
<tr><td>AN15</td></tr>
<tr><td>PPG11_0</td></tr>
<tr><td rowspan="4">42*1</td><td rowspan="4">51*1</td><td rowspan="4">63</td><td rowspan="4">73</td><td rowspan="4">89</td><td rowspan="4">108</td><td>P104</td></tr>
<tr><td>SCS72_0*2, *3</td></tr>
<tr><td>AN16</td></tr>
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<tr><td rowspan="4">43*1</td><td rowspan="4">52*1</td><td rowspan="4">64</td><td rowspan="4">74</td><td rowspan="4">90</td><td rowspan="4">109</td><td>P105</td></tr>
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<tr><td>AN17</td></tr>
<tr><td>PPG13_0</td></tr>
</table>
</td></tr>
</table>