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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526dwbpmc-gse1

Product lineup comparison 100 pins

	MB91F522F	MB91F523F	MB91F524F	MB91F525F	MB91F526F
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×34ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×21ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch[*1]				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	76 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V [*2]				
Package	LQI100				

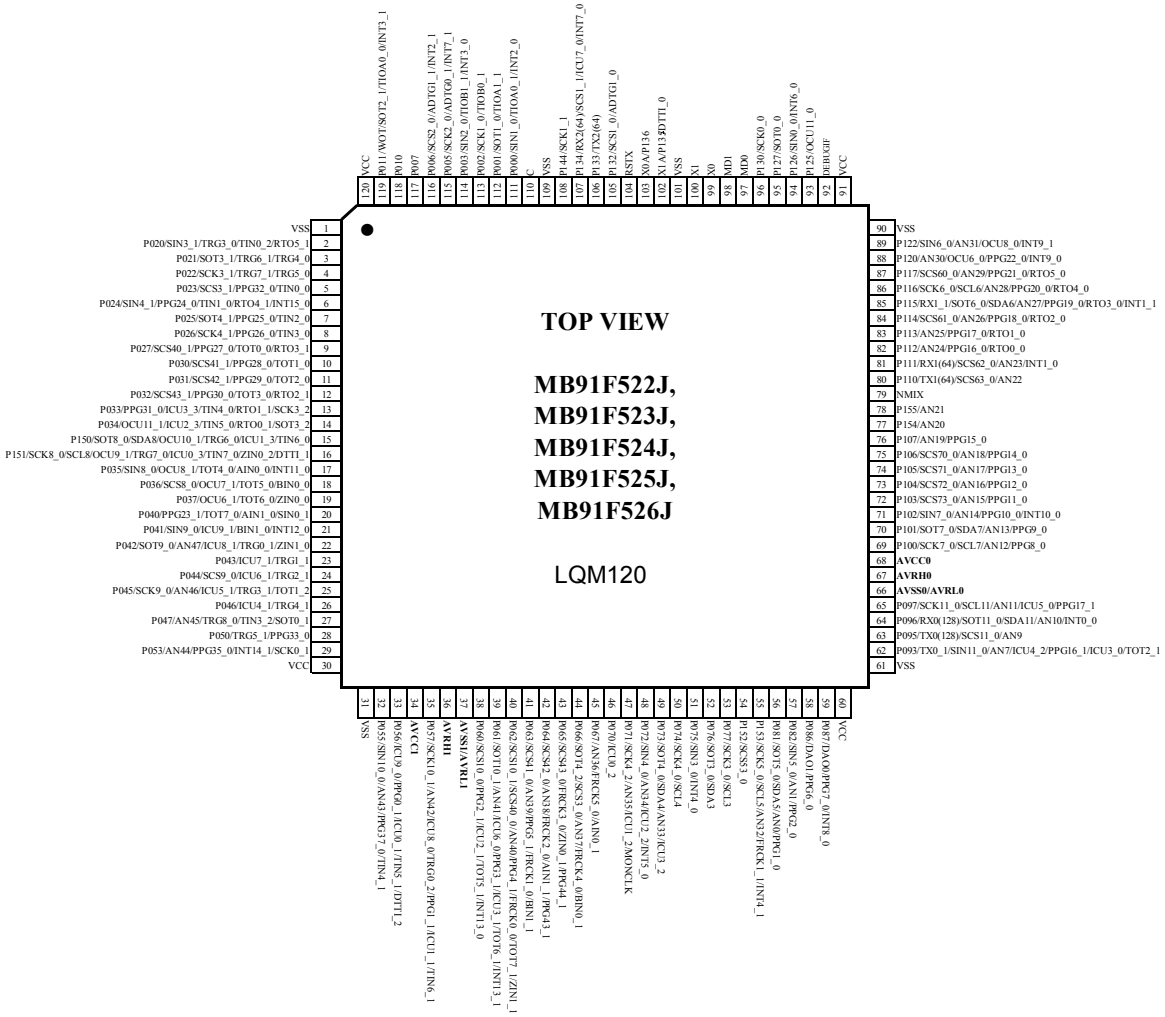
*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

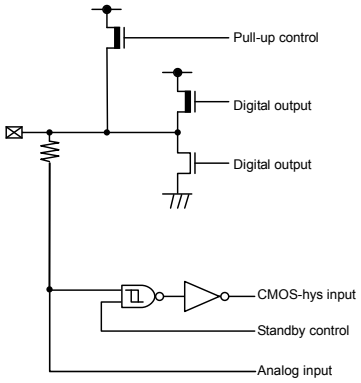
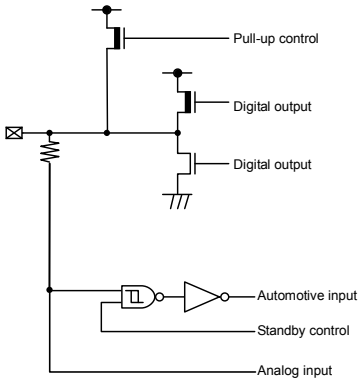
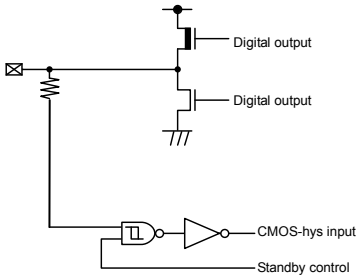
MB91F52xJ

MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J

(TOP VIEW)



* In a single clock product, pin 102 and pin 103 are the general-purpose ports.

Type	Circuit	Remarks
G		•Analog input, General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ • CMOS hysteresis input
H		•Analog input, General-purpose I/O port •Output 12mA •Pull-up resistor control 50kΩ •Automotive input
I		• General-purpose I/O port (5V tolerant) • Output 4mA • CMOS hysteresis input

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000400_H	ICSEL0 [R/W] B,H,W -----000	ICSEL1 [R/W] B,H,W -----000	ICSEL2 [R/W] B,H,W -------0	ICSEL3 [R/W] B,H,W -------0	DMA request generation and clear
000404_H	—	ICSEL5 [R/W] B,H,W -----000	ICSEL6 [R/W] B,H,W ----0000	ICSEL7 [R/W] B,H,W ----0000	
000408_H	ICSEL8 [R/W] B,H,W ------00	ICSEL9 [R/W] B,H,W ------00	ICSEL10 [R/W] B,H,W ------00	ICSEL11 [R/W] B,H,W -----000	
$00040C_H$	—	ICSEL13 [R/W] B,H,W ------00	ICSEL14 [R/W] B,H,W ------00	ICSEL15 [R/W] B,H,W ------00	
000410_H	ICSEL16 [R/W] B,H,W ----0000	ICSEL17 [R/W] B,H,W ------00	ICSEL18 [R/W] B,H,W ---00000	ICSEL19 [R/W] B,H,W -----000	
000414_H	ICSEL20 [R/W] B,H,W -----000	ICSEL21 [R/W] B,H,W ------00	ICSEL22 [R/W] B,H,W ------00	ICSEL23 [R/W] B,H,W ------00	
000418_H	IRPR0H [R] B,H,W 00------	IRPR0L [R] B,H,W 00------	IRPR1H [R] B,H,W 00------	IRPR1L [R] B,H,W 00------	Interrupt Request Batch Reading Register
$00041C_H$	—	—	IRPR3H [R] B,H,W 000000--	IRPR3L [R] B,H,W 000000--	
000420_H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 000-----	
000424_H	IRPR6H [R] B,H,W --00----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W -0-00---	IRPR7L [R] B,H,W ------00	
000428_H	IRPR8H [R] B,H,W --0-----	IRPR8L [R] B,H,W -00-----	IRPR9H [R] B,H,W -0------	IRPR9L [R] B,H,W -0------	
$00042C_H$	IRPR10H [R] B,H,W -0------	IRPR10L [R] B,H,W -0------	IRPR11H [R] B,H,W 0-------	IRPR11L [R] B,H,W 0-------	
000430_H	IRPR12H [R] B,H,W --0000--	IRPR12L [R] B,H,W ----00--	IRPR13H [R] B,H,W 00------	IRPR13L [R] B,H,W 00------	
000434_H	IRPR14H [R] B,H,W 00000000	IRPR14L [R] B,H,W 00000000	IRPR15H [R] B,H,W 000-----	IRPR15L [R] B,H,W 0000000-	
000438_H	ICSEL24 [R/W] B,H,W ------00	ICSEL25 [R/W] B,H,W ---00000	ICSEL26 [R/W] B,H,W -------0	ICSEL27 [R/W] B,H,W -------0	DMA request generation and clear
$00043C_H$	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0012D4$_H$	FRS6 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare
0012D8$_H$	FRS7 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
0012DC$_H$ to 0012FC$_H$	—	—	—	—	Reserved
001300$_H$	—				Reserved
001304$_H$	ADTSS0[R/W] B,H,W -------0	—	—	—	12-bit A/D converter 1/2 unit
001308$_H$	ADTSE0[R/W] B,H,W 00000000 00000000 00000000 00000000				
00130C$_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001310$_H$	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
001314$_H$	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
001318$_H$	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
00131C$_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
001320$_H$	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
001324$_H$	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001328$_H$	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		
00132C$_H$	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001330$_H$	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
001334$_H$	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001338$_H$	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
00133C$_H$	ADCOMP24/ADCOMPB24[R/W] H,W 00000000 00000000		ADCOMP25/ADCOMPB25[R/W] H,W 00000000 00000000		
001340$_H$	ADCOMP26/ADCOMPB26[R/W] H,W 00000000 00000000		ADCOMP27/ADCOMPB27[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001D70$_H$ to 001FFC$_H$	—	—	—	—	Reserved
002000$_H$	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0 [R/W] B,H,W -------- 00000000		CAN0 (128msb)
002004$_H$	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W -0100011 00000001		
002008$_H$	INTR0 [R] B,H,W 00000000 00000000		TESTR0 [R/W] B,H,W -------- X00000--		
00200C$_H$	BRPER0 [R/W] B,H,W -------- ----0000		—	—	
002010$_H$	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014$_H$	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018$_H$	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00201C$_H$	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002020$_H$	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
002024$_H$	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028$_H$	—	—	—	—	
00202C$_H$	—	—	—	—	
002030$_H$, 002034$_H$	Reserved(IF1 data mirror)				
002038$_H$	—	—	—	—	
00203C$_H$	—	—	—	—	
002040$_H$	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044$_H$	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048$_H$	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
00204C$_H$	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002050$_H$	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		

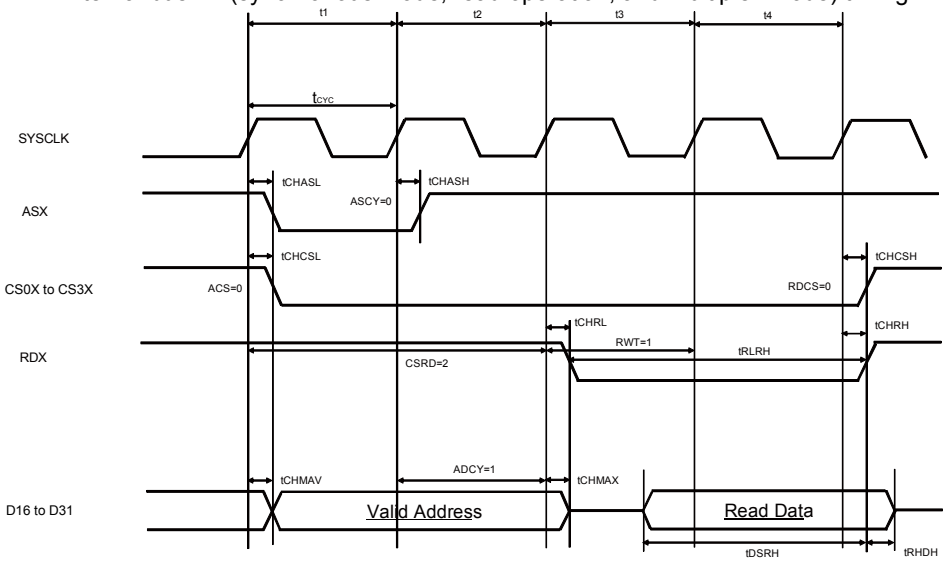
100 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

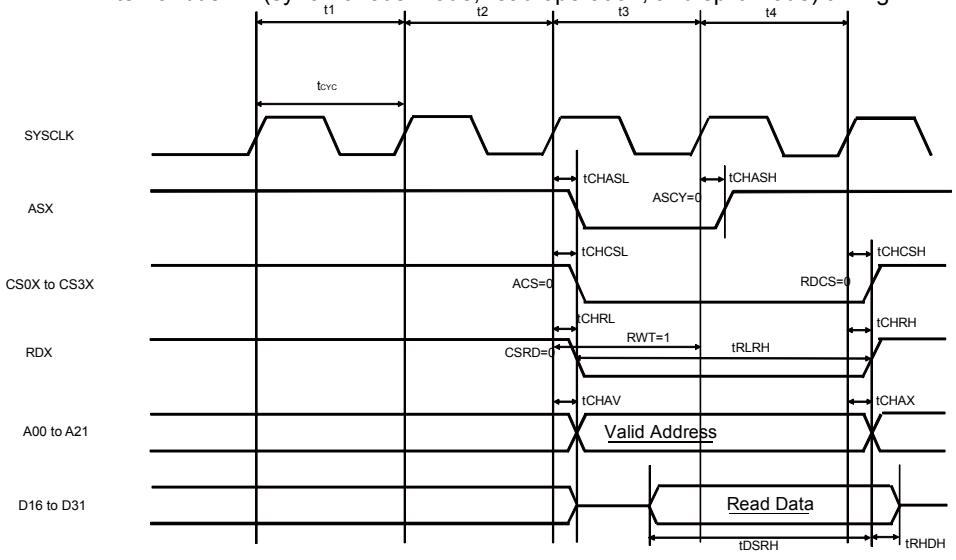
Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/7/9/10/11/12/13/14/15/16 17/18/19/22/23/26/27/28/29/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0/1/2 WG dead timer reload 0/1/2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1, *4
A/D converter 0/1/7/9/10/11/12/13/14/15/16/ 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit Free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching/measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0/1/2 WG dead timer reload 0/1/2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40

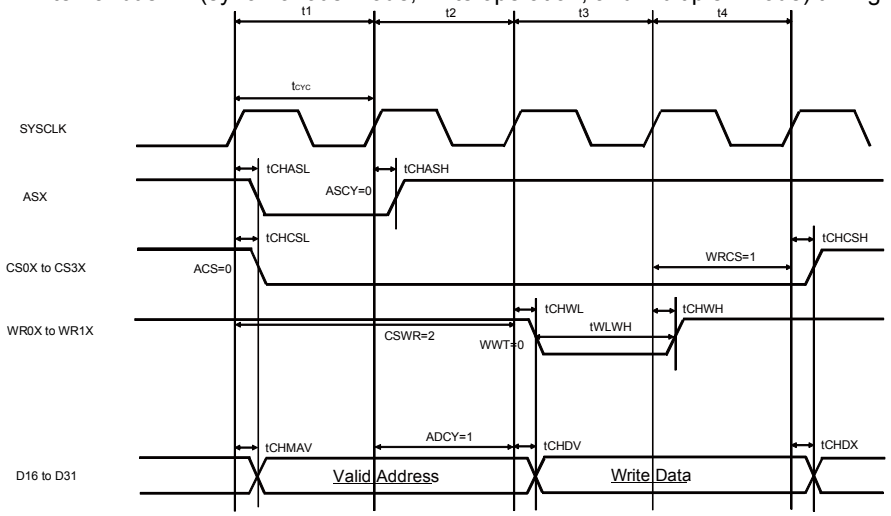
External bus I/F (synchronous mode, read operation, and multiplex mode) timing



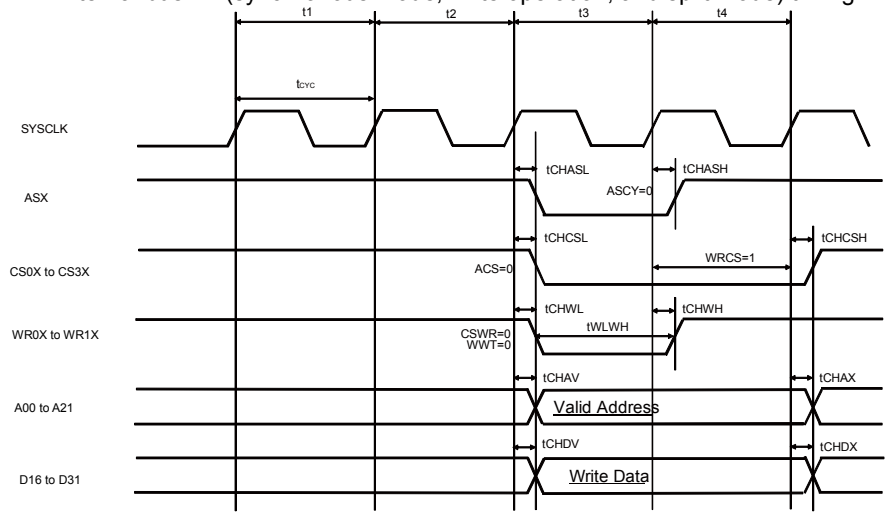
External bus I/F (synchronous mode, read operation, and split mode) timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing



15. Ordering Information MB91F52xxxD

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWDPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LJDPMC		OFF	ON	
MB91F525LWDPMC		ON	ON	
MB91F525LJDPMC		OFF	ON	
MB91F524LWDPMC		ON	ON	
MB91F524LJDPMC		OFF	ON	
MB91F523LWDPMC		ON	ON	
MB91F523LJDPMC		OFF	ON	
MB91F522LWDPMC		ON	ON	
MB91F522LJDPMC		OFF	ON	
MB91F526LSDPMC	None	ON	ON	
MB91F526LHDPMC		OFF	ON	
MB91F525LSDPMC		ON	ON	
MB91F525LHDPMC		OFF	ON	
MB91F524LSDPMC		ON	ON	
MB91F524LHDPMC		OFF	ON	
MB91F523LSDPMC		ON	ON	
MB91F523LHDPMC		OFF	ON	
MB91F522LSDPMC		ON	ON	
MB91F522LHDPMC		OFF	ON	
MB91F526KWDPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJDPMC		OFF	ON	
MB91F525KWDPMC		ON	ON	
MB91F525KJDPMC		OFF	ON	
MB91F524KWDPMC		ON	ON	
MB91F524KJDPMC		OFF	ON	
MB91F523KWDPMC		ON	ON	
MB91F523KJDPMC		OFF	ON	
MB91F522KWDPMC		ON	ON	
MB91F522KJDPMC		OFF	ON	
MB91F526KSDPMC	None	ON	ON	
MB91F526KHDPMC		OFF	ON	
MB91F525KSDPMC		ON	ON	
MB91F525KHDPMC		OFF	ON	
MB91F524KSDPMC		ON	ON	
MB91F524KHDPMC		OFF	ON	
MB91F523KSDPMC		ON	ON	
MB91F523KHDPMC		OFF	ON	
MB91F522KSDPMC		ON	ON	
MB91F522KHDPMC		OFF	ON	

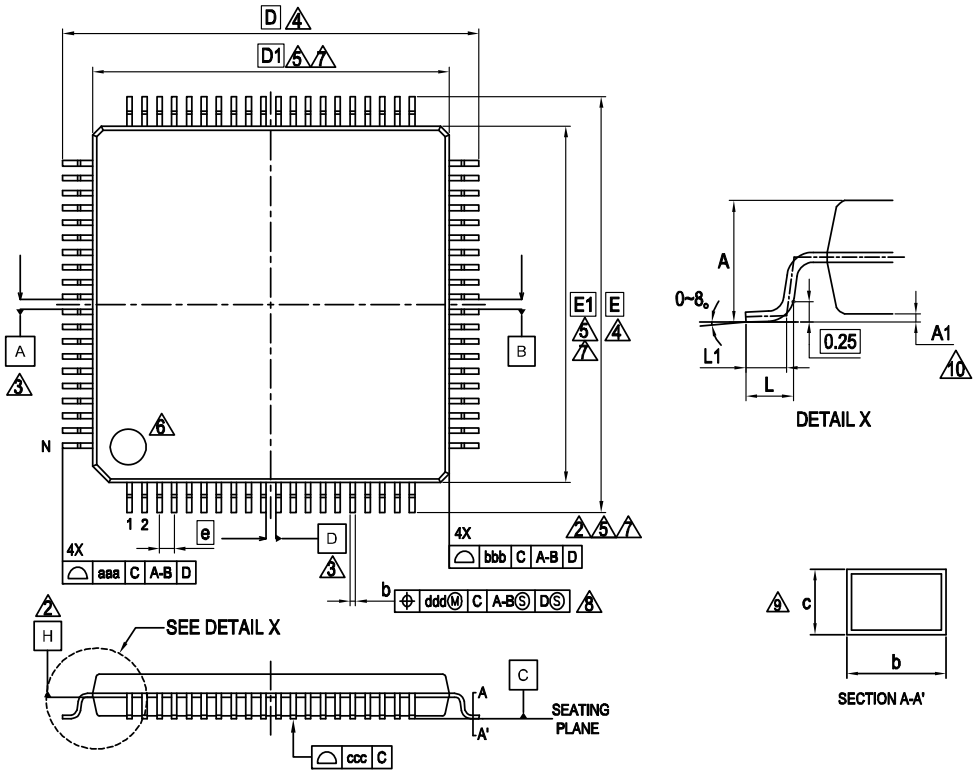
Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526KWDPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KJDPMC1		OFF	ON	
MB91F525KWDPMC1		ON	ON	
MB91F525KJDPMC1		OFF	ON	
MB91F524KWDPMC1		ON	ON	
MB91F524KJDPMC1		OFF	ON	
MB91F523KWDPMC1		ON	ON	
MB91F523KJDPMC1		OFF	ON	
MB91F522KWDPMC1		ON	ON	
MB91F522KJDPMC1		OFF	ON	
MB91F526KSDPMC1	None	ON	ON	
MB91F526KHDPMC1		OFF	ON	
MB91F525KSDPMC1		ON	ON	
MB91F525KHDPMC1		OFF	ON	
MB91F524KSDPMC1		ON	ON	
MB91F524KHDPMC1		OFF	ON	
MB91F523KSDPMC1		ON	ON	
MB91F523KHDPMC1		OFF	ON	
MB91F522KSDPMC1		ON	ON	
MB91F522KHDPMC1		OFF	ON	
MB91F526JWDPMC	Yes	ON	ON	LQM・120 pin, Plastic
MB91F526JJDPMC		OFF	ON	
MB91F525JWDPMC		ON	ON	
MB91F525JJDPMC		OFF	ON	
MB91F524JWDPMC		ON	ON	
MB91F524JJDPMC		OFF	ON	
MB91F523JWDPMC		ON	ON	
MB91F523JJDPMC		OFF	ON	
MB91F522JWDPMC		ON	ON	
MB91F522JJDPMC		OFF	ON	
MB91F526JSDPMC	None	ON	ON	
MB91F526JHDPMC		OFF	ON	
MB91F525JSDPMC		ON	ON	
MB91F525JHDPMC		OFF	ON	
MB91F524JSDPMC		ON	ON	
MB91F524JHDPMC		OFF	ON	
MB91F523JSDPMC		ON	ON	
MB91F523JHDPMC		OFF	ON	
MB91F522JSDPMC		ON	ON	
MB91F522JHDPMC		OFF	ON	

16. Ordering Information MB91F52xxxE

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWEPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LJEPMC		OFF	ON	
MB91F525LWEPMC		ON	ON	
MB91F525LJEPMC		OFF	ON	
MB91F524LWEPMC		ON	ON	
MB91F524LJEPMC		OFF	ON	
MB91F523LWEPMC		ON	ON	
MB91F523LJEPMC		OFF	ON	
MB91F522LWEPMC		ON	ON	
MB91F522LJEPMC		OFF	ON	
MB91F526LSEPMC	None	ON	ON	
MB91F526LHEPMC		OFF	ON	
MB91F525LSEPMC		ON	ON	
MB91F525LHEPMC		OFF	ON	
MB91F524LSEPMC		ON	ON	
MB91F524LHEPMC		OFF	ON	
MB91F523LSEPMC		ON	ON	
MB91F523LHEPMC		OFF	ON	
MB91F522LSEPMC		ON	ON	
MB91F522LHEPMC		OFF	ON	
MB91F526KWEPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJEPMC		OFF	ON	
MB91F525KWEPMC		ON	ON	
MB91F525KJEPMC		OFF	ON	
MB91F524KWEPMC		ON	ON	
MB91F524KJEPMC		OFF	ON	
MB91F523KWEPMC		ON	ON	
MB91F523KJEPMC		OFF	ON	
MB91F522KWEPMC		ON	ON	
MB91F522KJEPMC		OFF	ON	
MB91F526KSEPMC	None	ON	ON	
MB91F526KHEPMC		OFF	ON	
MB91F525KSEPMC		ON	ON	
MB91F525KHEPMC		OFF	ON	
MB91F524KSEPMC		ON	ON	
MB91F524KHEPMC		OFF	ON	
MB91F523KSEPMC		ON	ON	
MB91F523KHEPMC		OFF	ON	
MB91F522KSEPMC		ON	ON	
MB91F522KHEPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526FWEPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FJEPMC		OFF	ON	
MB91F525FWEPMC		ON	ON	
MB91F525FJEPMC		OFF	ON	
MB91F524FWEPMC		ON	ON	
MB91F524FJEPMC		OFF	ON	
MB91F523FWEPMC		ON	ON	
MB91F523FJEPMC		OFF	ON	
MB91F522FWEPMC		ON	ON	
MB91F522FJEPMC		OFF	ON	
MB91F526FSEPMC	None	ON	ON	
MB91F526FHEPMC		OFF	ON	
MB91F525FSEPMC		ON	ON	
MB91F525FHEPMC		OFF	ON	
MB91F524FSEPMC		ON	ON	
MB91F524FHEPMC		OFF	ON	
MB91F523FSEPMC		ON	ON	
MB91F523FHEPMC		OFF	ON	
MB91F522FSEPMC		ON	ON	
MB91F522FHEPMC		OFF	ON	
MB91F526DWEPMC	Yes	ON	ON	LQH・80 pin, Plastic
MB91F526DJEPMC		OFF	ON	
MB91F525DWEPMC		ON	ON	
MB91F525DJEPMC		OFF	ON	
MB91F524DWEPMC		ON	ON	
MB91F524DJEPMC		OFF	ON	
MB91F523DWEPMC		ON	ON	
MB91F523DJEPMC		OFF	ON	
MB91F522DWEPMC		ON	ON	
MB91F522DJEPMC		OFF	ON	
MB91F526DSEPMC	None	ON	ON	
MB91F526DHEPMC		OFF	ON	
MB91F525DSEPMC		ON	ON	
MB91F525DHEPMC		OFF	ON	
MB91F524DSEPMC		ON	ON	
MB91F524DHEPMC		OFF	ON	
MB91F523DSEPMC		ON	ON	
MB91F523DHEPMC		OFF	ON	
MB91F522DSEPMC		ON	ON	
MB91F522DHEPMC		OFF	ON	

LQH080 , 80 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQH080		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.15	0.20	0.25
c	0.09	——	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	80		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Page	Section	Change Results
23, 24	■PIN Description	(Continued) (Correct)

Pin no.						Pin Name
64	80	100	120	144	176	
15 *1	18 *1	23 *1	27 *1	30	37	P047
						A17 *2, *3, *4, *5
						AN45
						TRG8_0
						TIN3_2
						SOT0_1
-	-	-	-	-	38	P177
						TRG11_0
-	-	-	28 *1	31	39	P050
						A18 *5
						TRG5_1
						PPG33_0
-	-	-	-	32	40	P051
						A19
						TRG9_0
-	-	-	-	33	41	P052
						A20
						PPG34_0
						INT14_0
16 *1	19 *1	24 *1	29 *1	34	42	P053
						A21 *2, *3, *4, *5
						AN44
						PPG35_0
						INT14_1
						SCK0_1
-	-	-	-	35	43	P054
						SYSCLK
						PPG36_0
17 *1	22 *1	27 *1	32 *1	38	46	P055
						CS2X *2, *3, *4, *5
						SIN10_0
						AN43
						PPG37_0
						TIN4_1
-	-	-	33 *1	39	49	P056
						CS3X *5
						ICU9_0
						PPG0_1
						ICU0_1
						TIN5_1
						DTTI_2

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>34, 35</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">113 *1</td><td rowspan="4">133</td><td rowspan="4">161</td><td>P002</td></tr>
<tr><td>D18 *5</td></tr>
<tr><td>SCK1_0</td></tr>
<tr><td>TIOB0_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">76 *1</td><td rowspan="5">96 *1</td><td rowspan="5">114 *1</td><td rowspan="5">134</td><td rowspan="5">162</td><td>P003</td></tr>
<tr><td>D19 *3, *4, *5</td></tr>
<tr><td>SIN2_0</td></tr>
<tr><td>TIOB1_1</td></tr>
<tr><td>INT3_0</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">135</td><td rowspan="3">163</td><td>P004</td></tr>
<tr><td>D20</td></tr>
<tr><td>SOT2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">164</td><td>P164</td></tr>
<tr><td>PPG32_1</td></tr>
<tr><td rowspan="7">61 *1</td><td rowspan="7">77 *1</td><td rowspan="7">97 *1</td><td rowspan="7">115 *1</td><td rowspan="7">136 *1</td><td rowspan="7">165 *1</td><td>P005</td></tr>
<tr><td>D21 *2, *3, *4, *5</td></tr>
<tr><td>SCK2_0 *2</td></tr>
<tr><td>ADTG0_1</td></tr>
<tr><td>INT7_1</td></tr>
<tr><td>RX2(64) *4, *5, *6, *7</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">166</td><td>P165</td></tr>
<tr><td>PPG33_1</td></tr>
<tr><td rowspan="7">62 *1</td><td rowspan="7">78 *1</td><td rowspan="7">98 *1</td><td rowspan="7">116 *1</td><td rowspan="7">137 *1</td><td rowspan="7">167 *1</td><td>P006</td></tr>
<tr><td>D22 *2, *3, *4, *5</td></tr>
<tr><td>SCS2_0 *2</td></tr>
<tr><td>ADTG1_1</td></tr>
<tr><td>INT2_1</td></tr>
<tr><td>TX2(64) *4, *5, *6, *7</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">117 *1</td><td rowspan="2">138</td><td rowspan="2">168</td><td>P007</td></tr>
<tr><td>D23 *5</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">169</td><td>P166</td></tr>
<tr><td>PPG34_1</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">118 *1</td><td rowspan="2">139</td><td rowspan="2">170</td><td>P010</td></tr>
<tr><td>D24 *5</td></tr>
<tr><td rowspan="7">63 *1</td><td rowspan="7">79 *1</td><td rowspan="7">99 *1</td><td rowspan="7">119 *1</td><td rowspan="7">140</td><td rowspan="7">171</td><td>P011</td></tr>
<tr><td>WOT</td></tr>
<tr><td>D25 *2, *3, *4, *5</td></tr>
<tr><td>SOT2_1 *2</td></tr>
<tr><td>TIOA0_0 *2, *3, *4</td></tr>
<tr><td>INT3_1</td></tr>
</table></td></tr>
</table>

Page	Section	Change Results
Rev *C		
2	Features Peripheral Functions	The following sentence modified in I2C as following: (Error) < I2C > 2 channels ch.3 , ch.4 Standard mode/high-speed mode supported. Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported (Correct) < I2C > 2 channels ch.3 , ch.4 Standard mode/fast mode supported. Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported
5,6,7,8,9 ,10	1. Product Lineup	The following *2 added as follows: (Error) Power supply | 2.7 V to 5.5 V (Correct) Power supply | 2.7 V to 5.5 V *2
5,6,7,8,9 ,10	1. Product Lineup	The following sentence added as follows: (Correct) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
8, 9, 10,	1. Product Lineup	The following sentence modified in the bottom of Product lineup comparison table as following: (Error) *1: Only channel 3 and channel 4 support the I2C (high-speed mode/standard mode). (Correct) *1: Only channel 3 and channel 4 support the I2C (fast mode/standard mode).
11	1. Product Lineup	Added silicon version E

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				(1) 12-bit A/D Converter Electrical Characteristics: Added the value of "Total error". Total error value Min – Typ – Max ±12 LSB Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB Added the following description. Parameter : Power supply current I_A AVCC*3 *3: The power supply current described only current value on A/D converter. The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter. Electrical Characteristics 7.D/A Converter: Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter. Electrical Characteristics 6.Flash memory: Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing Tj<+105°C" Electrical Characteristics 7.D/A Converter: Corrected the following description. Parameter : Power supply current Symbol IA Pin name AV_{CC} Symbol IAH Pin name AV_{CC} ↓ Symbol IA Pin name AVCC Symbol IAH Pin name AVCC Example Characteristics Corrected the following description. Watch mode Ordering Information Corrected the following description. • ORDERING INFORMATION ↓ • ORDERING INFORMATION MB91F52xxxB[*1]