What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

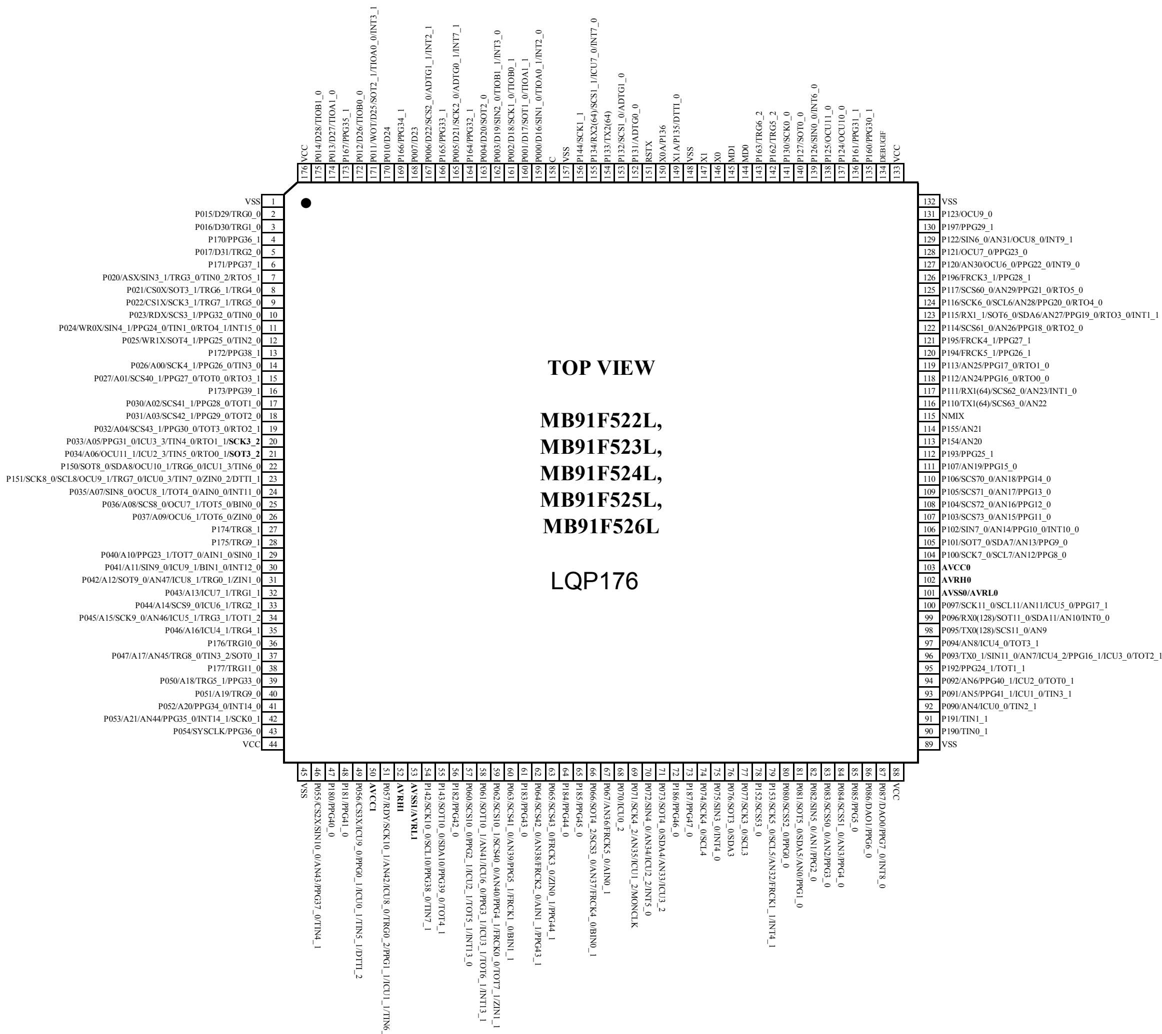
Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526dwbpmc-gse2

- D/A converter (R-2R type)
  - 8-bit resolution : 2ch
- External interrupt input: 8 channels × 2 units total 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max.12 channels
  - 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
    < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detection functions provided
  - DMA transfer support
    <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detection function is provided
  - DMA transfer support
  - Serial chip select SPI function
    <LIN (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - LIN protocol revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support
  - Hard assist function
    < I^2C >
  - 2 channels ch.3 , ch.4 Standard mode/fast mode supported.
  - 6 channels ch.5 to ch.8, ch.10, ch.11 Standard mode supported.
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (CAN) : 3 channels
  - Transfer speed : Up to 1Mbps
  - 128-transmission/reception message buffering : 1 channel (ch.0),
    64-transmission/reception message buffering : 2 channels (ch.1 and ch.2)
- PPG: 16-bit × Max. 48 channels
  - LED drive output 4 channels 11ch to 14ch
  - Reload timer : 16-bit × Max.8 channels
  - Free-run timer :
    16-bit × 3 channels
    32-bit × Max 3 channels
- Input capture :
  16-bit × 4 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Output compare :
  16-bit × 6 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Waveform generator : 6 channels
- Up/Down counter
  - 8/16-bit Up/Down counter × 2 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main or sub oscillation frequency can be selected for the operation clock
- Calibration: Real-time clock (RTC) of the subclock drive
  - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (by damaged quartz, etc.) of suboscillation (32kHz) (dual clock products) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
  - Initial value ON/OFF can be selected by the part number.
- Base timer : Max.2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascade mode
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog (possible to set the valid range for counter clearing)
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
  - The interrupt existence from two or more peripherals can be read by a series of register.
- I/O relocation
  - Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode

MB91F52xL

MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L

(TOP VIEW)



* In a single clock product, pin 149 and pin 150 are the general-purpose ports.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	73	87	103	125	P117	-	B	General-purpose I/O port
						SCS60_0	-		Serial chip select 60 I/O (0)
						AN29	-		ADC analog 29 input
						PPG21_0	-		PPG ch.21 output (0)
						RTO5_0	-		Waveform generator ch.5 output pin (0)
-	-	-	-	-	126	P196	-	A	General-purpose I/O port
						FRCK3_1	-		Free-run timer 3 clock input (1)
						PPG28_1	-		PPG ch.28 output (1)
-	-	-	88	104	127	P120	-	B	General-purpose I/O port
						AN30	-		ADC analog 30 input
						OCU6_0	-		Output compare ch.6 output (0)
						PPG22_0	-		PPG ch.22 output (0)
						INT9_0	-		INT9 External interrupt input (0)
-	-	-	-	105	128	P121	-	A	General-purpose I/O port
						OCU7_0	-		Output compare ch.7 output (0)
						PPG23_0	-		PPG ch.23 output (0)
48	59	74	89	106	129	P122	-	J	General-purpose I/O port
						SIN6_0	-		Multi-function serial ch.6 serial data input (0)
						AN31	-		ADC analog 31 input
						OCU8_0	-		Output compare ch.8 output (0)
						INT9_1	-		INT9 External interrupt input (1)
-	-	-	-	-	130	P197	-	A	General-purpose I/O port
						PPG29_1	-		PPG ch.29 output (1)
-	-	-	-	107	131	P123	-	A	General-purpose I/O port
						OCU9_0	-		Output compare ch.9 output (0)
49	62	77	92	110	134	DEBUGIF	-	L	MDI I/O for debugger (OCD)
-	-	-	-	-	135	P160	-	A	General-purpose I/O port
						PPG30_1	-		PPG ch.30 output (1)
-	-	-	-	-	136	P161	-	A	General-purpose I/O port
						PPG31_1	-		PPG ch.31 output (1)
-	-	-	-	111	137	P124	-	A	General-purpose I/O port
						OCU10_0	-		Output compare ch.10 output (0)
-	-	-	93	112	138	P125	-	A	General-purpose I/O port
						OCU11_0	-		Output compare ch.11 output (0)
50	63	78	94	113	139	P126	-	F	General-purpose I/O port
						SIN0_0	-		Multi-function serial ch.0 serial data input (0)
						INT6_0	-		INT6 External interrupt input (0)
-	64	79	95	114	140	P127	-	A	General-purpose I/O port
						SOT0_0	-		Multi-function serial ch.0 serial data output (0)

6. Handling Devices

This section explains the latch-up prevention and pin processing.

- For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC, AVRH) and analog input must not be exceed the digital power supply (VCC) when the power supply to the analog system is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC) and analog power supplies (AVCC, AVRH) simultaneously. Or, turn on the digital power supply (VCC), and then turn on analog power supplies (AVCC, AVRH).

- Treatment of unused pins

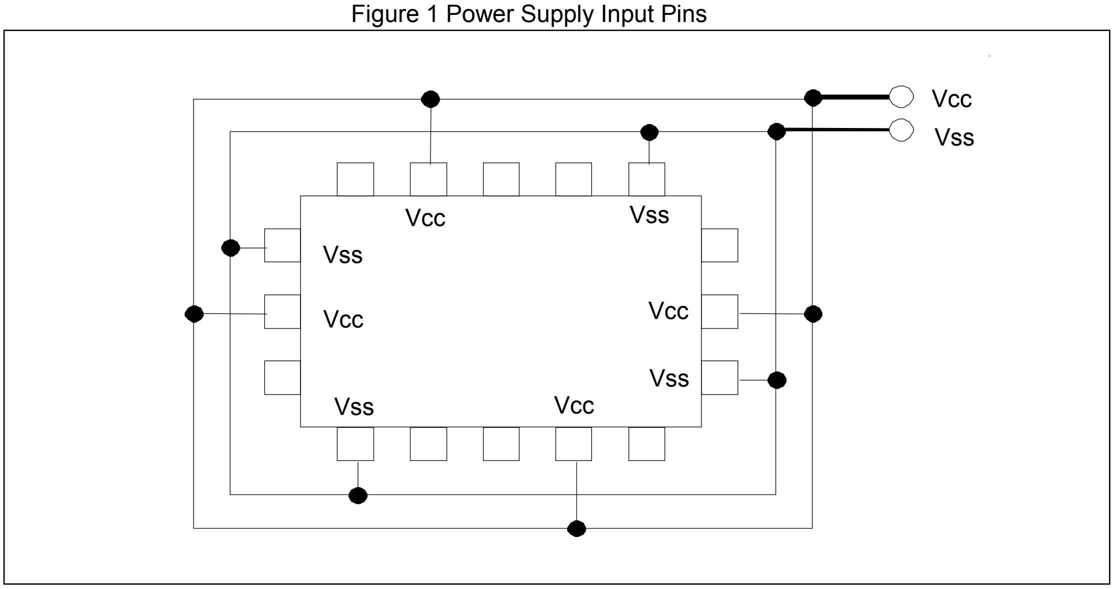
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2kΩ resistor to each of the unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

- Power supply pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1 Power Supply Input Pins



The power supply pins should be connected to VCC and VSS pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000074_H	—	FRS9 [R/W] B,H,W --00--00 --00--00 --00--00			Free-run timer selection register 9
000078_H	—	—	—	OCLS67 [R/W] B,H,W ----0000	OCU67 Output level control register
$00007C_H$	—	—	—	OCLS89 [R/W] B,H,W ----0000	OCU89 Output level control register
000080_H	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] H -000--00 -000-000		Base Timer 0
000084_H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	—	—	
000088_H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	—	—	—	—	Reserved
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00 -000-000		Base Timer 1
000094_H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base Timer 0,1
$0000A0_H$ to $0000FC_H$	—	—	—	—	Reserved
000100_H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1
000104_H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108_H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2
$00010C_H$	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000		
000110_H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3
000114_H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000		
000118_H	MSCY4 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 Cycle measurement data register 45
$00011C_H$	MSCY5 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00147C$_H$	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000		12-bit A/D converter 2/2 unit
001480$_H$	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		
001484$_H$	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000		
001488$_H$	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000		
00148C$_H$	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000		
001490$_H$	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000		
001494$_H$	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000		
001498$_H$ to 0014B4$_H$	—	—	—	—	Reserved
0014B8$_H$	ADTCS32[R/W] B,H,W 00000000 0010----		ADTCS33[R/W] B,H,W 00000000 0010----		12-bit A/D converter 2/2 unit
0014BC$_H$	ADTCS34[R/W] B,H,W 00000000 0010----		ADTCS35[R/W] B,H,W 00000000 0010----		
0014C0$_H$	ADTCS36[R/W] B,H,W 00000000 0010----		ADTCS37[R/W] B,H,W 00000000 0010----		
0014C4$_H$	ADTCS38[R/W] B,H,W 00000000 0010----		ADTCS39[R/W] B,H,W 00000000 0010----		
0014C8$_H$	ADTCS40[R/W] B,H,W 00000000 0010----		ADTCS41[R/W] B,H,W 00000000 0010----		
0014CC$_H$	ADTCS42[R/W] B,H,W 00000000 0010----		ADTCS43[R/W] B,H,W 00000000 0010----		
0014D0$_H$	ADTCS44[R/W] B,H,W 00000000 0010----		ADTCS45[R/W] B,H,W 00000000 0010----		
0014D4$_H$	ADTCS46[R/W] B,H,W 00000000 0010----		ADTCS47[R/W] B,H,W 00000000 0010----		
0014D8$_H$ to 0014F4$_H$	—	—	—	—	Reserved
0014F8$_H$	ADTCD32[R] B,H,W 10--0000 00000000		ADTCD33[R] B,H,W 10--0000 00000000		12-bit A/D converter 2/2 unit
0014FC$_H$	ADTCD34[R] B,H,W 10--0000 00000000		ADTCD35[R] B,H,W 10--0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001804$_H$	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001808$_H$	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
00180C$_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810$_H$	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814$_H$	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818$_H$	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00181C$_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820$_H$	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824$_H$	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828$_H$	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
00182C$_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830$_H$	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834$_H$	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838$_H$	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
00183C$_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0018F0$_H$	— /(SCSTR310)/ (LAMSR10) [R/W] B,H,W -------- *3	— /(SCSTR210)/ (LAMCR10) [R/W] B,H,W -------- *3	— /(SCSTR110)/ (SFLR110)[R/W] B,H,W -------- *3	— /(SCSTR010)/ (SFLR010)[R/W] B,H,W -------- *3	Multi-UART10 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018F4$_H$	—	— /(SCSFR210) [R/W] B,H,W -------- *3	— /(SCSFR110) [R/W] B,H,W -------- *3	— /(SCSFR010) [R/W] B,H,W -------- *3	
0018F8$_H$	—/(TBYTE310)/ (LAMESR10) [R/W] B,H,W -------- *3	—/(TBYTE210)/ (LAMERT10) [R/W] B,H,W -------- *3	—/(TBYTE110)/ (LAMIER10) [R/W] B,H,W -------- *3	TBYTE010/(LAMRID10)/(LAMTID10) [R/W] B,H,W 00000000	
0018FC$_H$	BGR10[R/W] H, W 00000000 00000000		— /(ISMK10)[R/W] B,H,W -------- *2	— /(ISBA10)[R/W] B,H,W -------- *2	
001900$_H$	FCR110[R/W] B,H,W ---00100	FCR010[R/W] B,H,W -0000000	FBYTE10[R/W] B,H,W 00000000 00000000		
001904$_H$	FTICR10[R/W] B,H,W 00000000 00000000		—	—	
001908$_H$	SCR11/(IBCR11) [R/W] B,H,W 0--00000	SMR11[R/W] B,H,W 000-00-0	SSR11[R/W] B,H,W 0-000011	ESCR11/(IBSR11) [R/W] B,H,W 00000000	Multi-UART11 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00190C$_H$	— /(RDR111/(TDR111))[R/W] B,H,W -------- -------- *3		RDR011/(TDR011)[R/W] B,H,W -------0 00000000 *1		
001910$_H$	SACSR11[R/W] B,H,W 0----000 00000000		STMR11[R] B,H,W 00000000 00000000		
001914$_H$	STMCR11[R/W] B,H,W 00000000 00000000		— /(SCSCR11/SFUR11)[R/W] B,H,W -------- -------- *3 *4		
001918$_H$	— /(SCSTR311)/ (LAMSR11) [R/W] B,H,W -------- *3	— /(SCSTR211)/ (LAMCR11) [R/W] B,H,W -------- *3	— /(SCSTR111)/ (SFLR111)[R/W] B,H,W -------- *3	— /(SCSTR011)/ (SFLR011)[R/W] B,H,W -------- *3	
00191C$_H$	—	— /(SCSFR211) [R/W] B,H,W -------- *3	— /(SCSFR111) [R/W] B,H,W -------- *3	— /(SCSFR011) [R/W] B,H,W -------- *3	
001920$_H$	—/(TBYTE311)/ (LAMESR11) [R/W] B,H,W -------- *3	—/(TBYTE211)/ (LAMERT11) [R/W] B,H,W -------- *3	—/(TBYTE111)/ (LAMIER11) [R/W] B,H,W -------- *3	TBYTE011/(LAMRID11)/(LAMTID11) [R/W] B,H,W 00000000	
001924$_H$	BGR11[R/W] H, W 00000000 00000000		— /(ISMK11)[R/W] B,H,W -------- *2	— /(ISBA11)[R/W] B,H,W -------- *2	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B24H	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PTMR11 [R] H,W 11111111 11111111		PPG11
001B28H	PCN211 [R/W] B,H,W --000000 -----110		PSDR11 [R/W] H,W 00000000 00000000		
001B2CH	PTPC11 [R/W] H,W 00000000 00000000		—	—	
001B30H	PCN12 [R/W] B,H,W 00000000 000000-0		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
001B34H	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PTMR12 [R] H,W 11111111 11111111		
001B38H	PCN212 [R/W] B,H,W --000000 -----110		PSDR12 [R/W] H,W 00000000 00000000		
001B3CH	PTPC12 [R/W] H,W 00000000 00000000		—	—	
001B40H	PCN13 [R/W] B,H,W 00000000 000000-0		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
001B44H	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PTMR13 [R] H,W 11111111 11111111		
001B48H	PCN213 [R/W] B,H,W --000000 -----110		PSDR13 [R/W] H,W 00000000 00000000		
001B4CH	PTPC13 [R/W] H,W 00000000 00000000		—	—	
001B50H	PCN14 [R/W] B,H,W 00000000 000000-0		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
001B54H	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PTMR14 [R] H,W 11111111 11111111		
001B58H	PCN214 [R/W] B,H,W --000000 -----110		PSDR14 [R/W] H,W 00000000 00000000		
001B5CH	PTPC14 [R/W] H,W 00000000 00000000		—	—	
001B60H	PCN15 [R/W] B,H,W 00000000 000000-0		PCSR15 [W] H,W XXXXXXXX XXXXXXXX		PPG15
001B64H	PDUT15 [W] H,W XXXXXXXX XXXXXXXX		PTMR15 [R] H,W 11111111 11111111		
001B68H	PCN215 [R/W] B,H,W --000000 -----110		PSDR15 [R/W] H,W 00000000 00000000		
001B6CH	PTPC15 [R/W] H,W 00000000 00000000		—	—	
001B70H	PCN16 [R/W] B,H,W 00000000 000000-0		PCSR16 [W] H,W XXXXXXXX XXXXXXXX		PPG16
001B74H	PDUT16 [W] H,W XXXXXXXX XXXXXXXX		PTMR16 [R] H,W 11111111 11111111		

80 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*6
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*6
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390$_H$	000FFF90$_H$	11
Multi-function serial interface ch.4 (reception completed) Multi-function serial interface ch.4 (status)	28	1C	ICR12	38C$_H$	000FFF8C$_H$	12[*1]
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388$_H$	000FFF88$_H$	13
Multi-function serial interface ch.5 (reception completed) Multi-function serial interface ch.5 (status)	30	1E	ICR14	384$_H$	000FFF84$_H$	14[*1]
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380$_H$	000FFF80$_H$	15
Multi-function serial interface ch.6 (reception completed) Multi-function serial interface ch.6 (status)	32	20	ICR16	37C$_H$	000FFF7C$_H$	16[*1]
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378$_H$	000FFF78$_H$	17
CAN0	34	22	ICR18	374$_H$	000FFF74$_H$	-
CAN1 RAM diagnosis end RAM initialization completion Error generation during RAM diagnosis Backup RAM diagnosis end Backup RAM initialization completion Error generation during Backup RAM diagnosis	35	23	ICR19	370$_H$	000FFF70$_H$	-
CAN2 Up/down counter 0 Up/down counter 1	36	24	ICR20	36C$_H$	000FFF6C$_H$	-
Real time clock	37	25	ICR21	368$_H$	000FFF68$_H$	-
Multi-function serial interface ch.7 (reception completed) Multi-function serial interface ch.7 (status)	38	26	ICR22	364$_H$	000FFF64$_H$	22[*1]
16-bit Free-running timer 0 (0 detection) / (compare clear) Multi-function serial interface ch.7 (transmission completed)	39	27	ICR23	360$_H$	000FFF60$_H$	23
PPG 1/10/11/20/21/30/31 16-bit Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	35C$_H$	000FFF5C$_H$	24[*3]
PPG 2/3/12/13/23/32/43 16-bit Free-run timer 2 (0 detection) / (compare clear)	41	29	ICR25	358$_H$	000FFF58$_H$	25[*3]
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354$_H$	000FFF54$_H$	26[*3]
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350$_H$	000FFF50$_H$	27[*3]
PPG 8/9/18/19/28/29	44	2C	ICR28	34C$_H$	000FFF4C$_H$	28[*3]

(3-2) [MB9152xxxE]

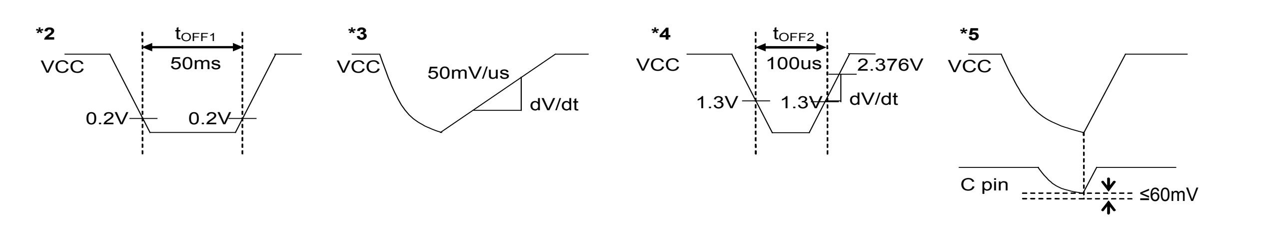
(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Power off time	t_{OFF1}	V_{CC}	Vcc ≤ 0.2V	50	–	–	ms	*2
	t_{OFF2}	V_{CC}	Vcc ≤ 1.3V	100	–	–	µs	*4
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2V to 2.376V (t_{OFF1} $<$ 50ms)	–	–	50	mV/µs	*3
	dV/dt	V_{CC}	VCC: 1.3V to 2.376V (t_{OFF2} ≥ 100µs)	–	–	1000	mV/µs	*4
C pin voltage at Power-on	–	C	–	–	–	60	mV	*5
Maximum ramp rate guaranteed to not generate power-on reset	|dV/dt|	Vcc	VCC: Between 2.4V and 4.5V	–	–	50	mV/µs	*6

*1: The specified level detection time applies only for power ramp rate of 1000mV/µs or less.
*2: Vcc must be held below 0.2V for a minimum period of t_{OFF1}.
*3: Power-on can detect by satisfying power ramp rate when t_{OFF1} is not satisfied.
*4: Vcc must be held below 1.3V for a minimum period of t_{OFF2}.
Power ramp rate must be 1000mV/µs or less from 1.3V to 2.376V.
Power-on can detect by satisfying power ramp rate and power off time.
*5: C-pin voltage is below 60 mV when VCC is turned on again.
*6: This specification is specified the power supply fluctuation after power on detection. When VCC voltage is between 2.4V and 4.5V, the power supply fluctuation is below 50mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.

Note: When using MB91F52xxxE, either *2 or *3 or *4 or *5 must be satisfied. When neither *2 nor *3 nor *4 nor *5 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate, C pin voltage at Power-on



(4-1-2) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=1, SCR:SPI=0

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

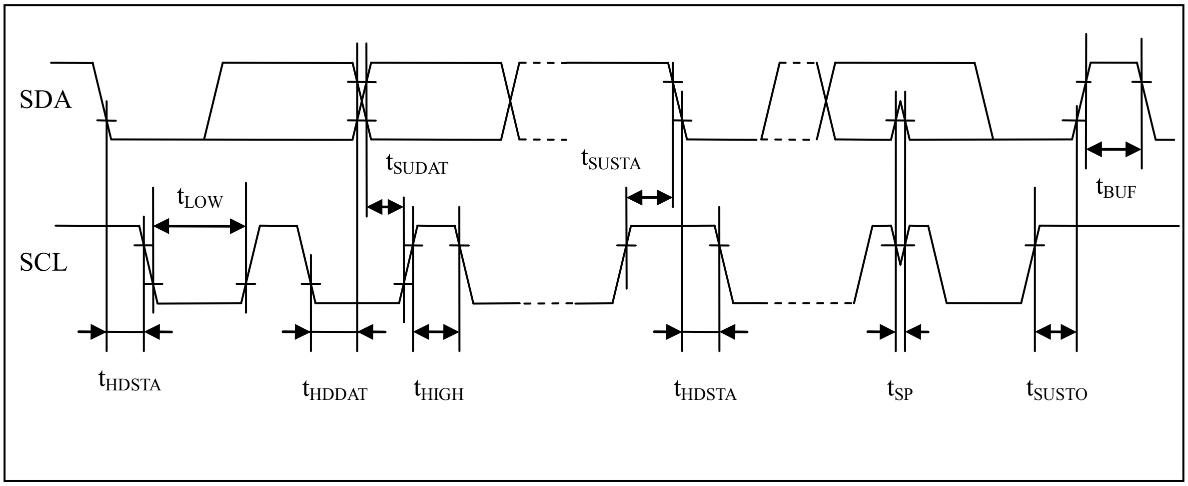
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-30	30	ns	
		SCK3 , SCK4 SOT3 , SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11		34	-	ns	
		SCK3 , SCK4 SIN3, SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK11 SIN0 to SIN11		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11		-	33	ns	
		SCK3 , SCK4 SOT3 , SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK11 SIN0 to SIN11		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK11		-	5	ns	
SCK rise time	t_R	SCK0 to SCK11		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

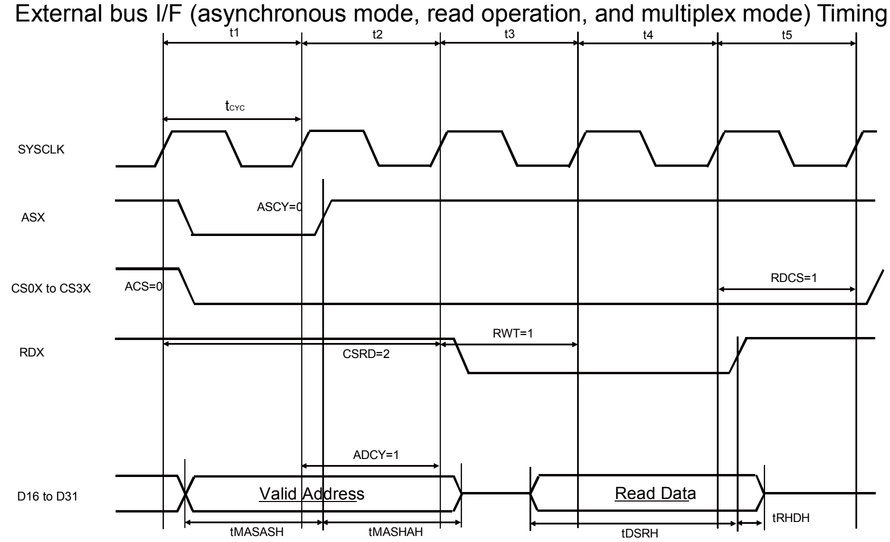
"$t_{SUDAT} \geq 250$ ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I^2C.

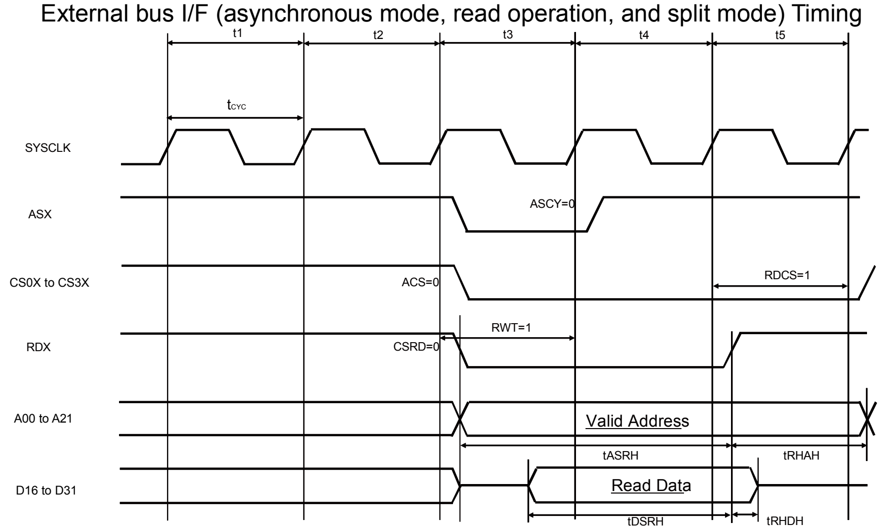
• I^2C timing



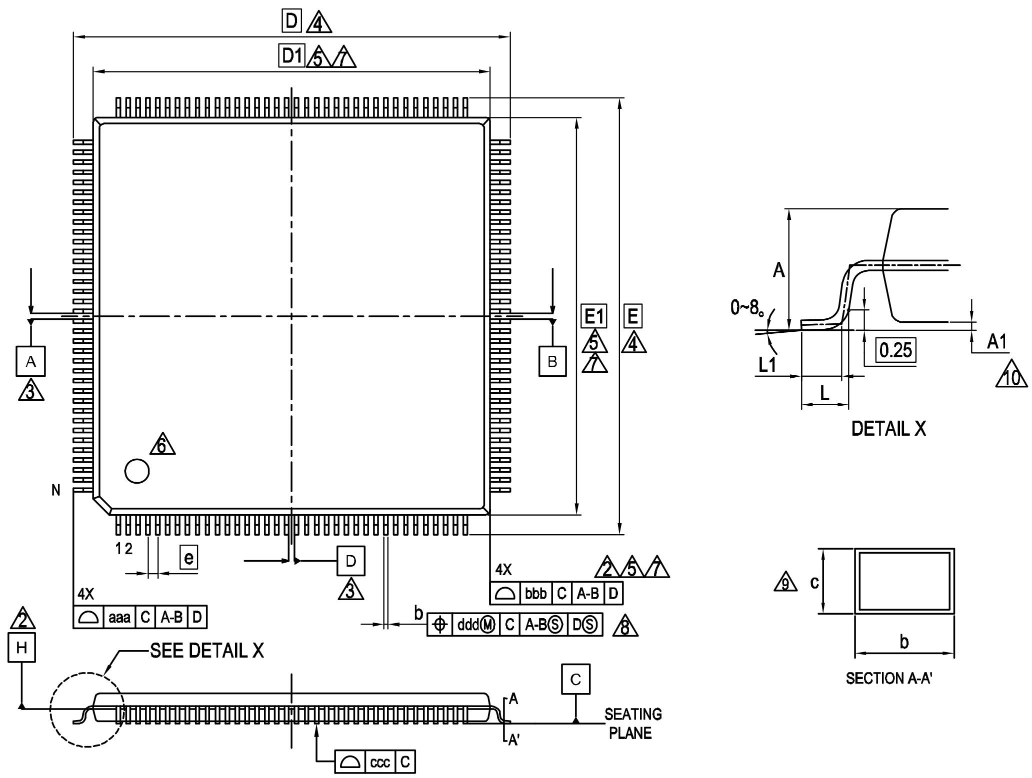
External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



External bus I/F (asynchronous mode, read operation, and split mode) Timing



LQS144 , 144 Lead Plastic Low Profile Quad Flat Package



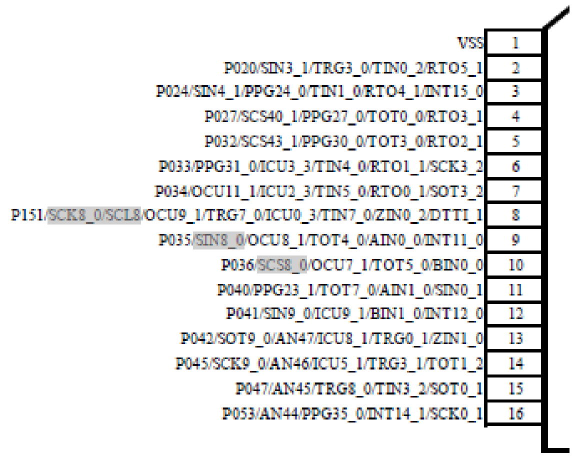
PACKAGE	LQS144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05/0.06	—	0.15/0.26
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC.		
D1	20.00 BSC.		
e	0.50 BSC		
E	22.00 BSC.		
E1	20.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>13</td><td>■Pin Assignment MB91F52xB</td><td>
Signals indicated by the shading below deleted in Figure.
- Left side



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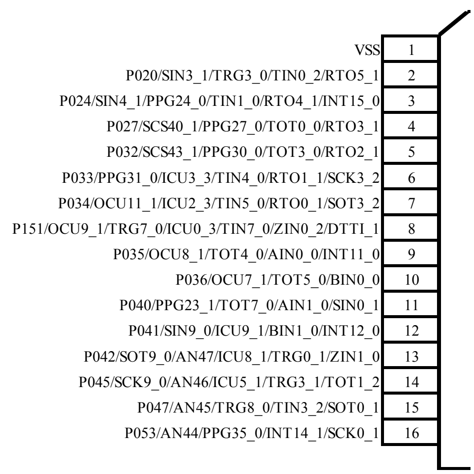

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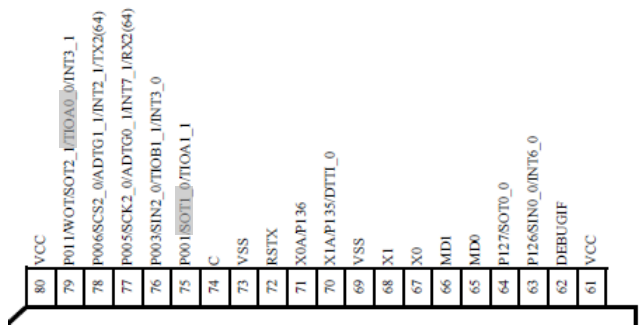
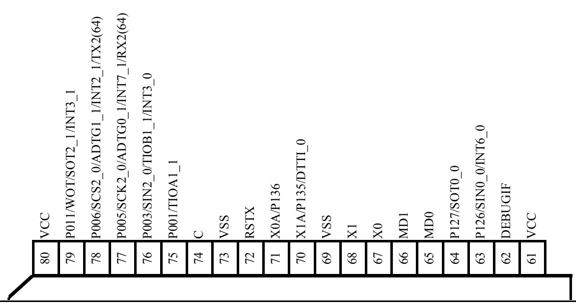
Page	Section	Change Results
14	■Pin Assignment MB91F52xD	- Top  ↓ 
14	■Pin Assignment MB91F52xD	The following note added on the bottom left of Figure. * In a single clock product, pin 71 and pin 72 are the general-purpose ports.

Page	Section	Change Results
23, 24	■PIN Description	A List of "Pin Description" modified. (Error)

Pin no.						Pin Name
64	80	100	120	144	176	
15	18	23	27	30	37	P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1
-	-	-	-	-	38	P177 TRG11_0
-	-	-	28	31	39	P050 A18 TRG5_1 PPG33_0
-	-	-	-	32	40	P051 A19 TRG9_0
-	-	-	-	33	41	P052 A20 PPG34_0 INT14_0
16	19	24	29	34	42	P053 A21 AN44 PPG35_0 INT14_1 SCK0_1
-	-	-	-	35	43	P054 SYSCLK PPG36_0
17	22	27	32	38	46	P055 CS2X SIN10_0 AN43 PPG37_0 TIN4_1
-	-	-	33	39	49	P056 CS3X ICU9_0 PPG0_1 ICU0_1 TIN5_1 DTTI_2

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Value: Min -30 Max 30 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min -30 Max 30 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min -300 Max 300 (4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time t_{IVSHI} (4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time t_{IVSLI} Corrected the following description. Pin name: SCK0 to SCK11 SIN0 to SIN11 Value: Min 34 Max - ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11 Value: Min 34 Max - Pin name: SCK3,SCK4,SIN3,SIN4 Value: Min 300 Max – (4-1-1),(4-1-4)SCK↓⇒SOT delay time t_{SLOVE} (4-1-2),(4-1-3)SCK↑⇒SOT delay time t_{SHOVE} Corrected the following description. Pin name: SCK0 to SCK11 SOT0 to SOT11 Value: Min - Max 33 ↓ Pin name: SCK0 to SCK2,SCK5 to SCK11 SOT0 to SOT2,SOT5 to SOT11 Value: Min - Max 33 Pin name: SCK3,SCK4 SOT3,SOT4 Value: Min - Max 300 (4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time t_F Corrected the following description. Pin name: SCK0 to SCK2,SCK5 to SCK11 Value: Min - Max 5 Pin name: SCK3,SCK4 Value: Min - Max 250 ↓ Pin name: SCK0 to SCK11 Value: Min - Max 5 (4-1-5)SCS↓⇒SCK↓ setup time t_{CSSI} (4-1-6)SCS↓⇒SCK↑ setup time t_{CSSI} (4-1-7)SCS↑⇒SCK↓ setup time t_{CSSI} (4-1-8)SCS↑⇒SCK↑ setup time t_{CSSI} Corrected the following description. Pin name: SCK1 to SCK11 SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSSU}+0 Max t_{CSSU}+50 ↓ Pin name: SCK1,SCK2,SCK5 to SCK11 SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 Value: Min t_{CSSU}-50 Max t_{CSSU}+0 Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43 Value: Min t_{CSSU}-50 Max t_{CSSU}+300