# Infineon Technologies - MB91F526DWBPMC-GTE1 Datasheet

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## What is "Embedded - Microcontrollers"?

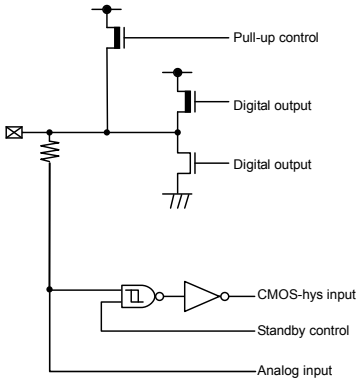
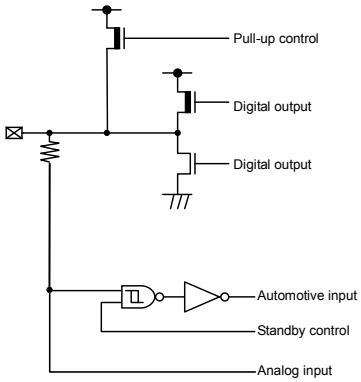
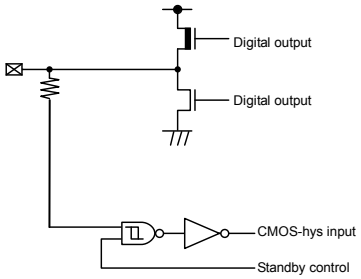
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | FR81S |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, CSIO, I²C, LINbus, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 56 |
| Program Memory Size | 1.0625MB (1.0625M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 136K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 32x12b; D/A 1x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526dwbpmc-gte1 |

| Pin no. | | | | | | Pin Name | Polarity | I/O circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 5 *1 | 7 *1 | 9 *1 | 12 *1 | 15 | 19 | P032 | - | A | General-purpose I/O port |
| | | | | | | A04 *2, *3, *4, *5 | - | | External bus/Address bit4 output (0) |
| | | | | | | SCS43_1 | - | | Serial chip select 43 output (1) |
| | | | | | | PPG30_0 | - | | PPG ch.30 output (0) |
| | | | | | | TOT3_0 | - | | Reload timer ch.3 output (0) |
| | | | | | | RTO2_1 | - | | Waveform generator ch.2 output pin (1) |
| 6 *1 | 8 *1 | 10 *1 | 13 *1 | 16 | 20 | P033 | - | A | General-purpose I/O port |
| | | | | | | A05 *2, *3, *4, *5 | - | | External bus/Address bit5 output (0) |
| | | | | | | PPG31_0 | - | | PPG ch.31 output (0) |
| | | | | | | ICU3_3 | - | | Input capture ch.3 input (3) |
| | | | | | | TIN4_0 | - | | Reload timer ch.4 event input (0) |
| | | | | | | RTO1_1 | - | | Waveform generator ch.1 output pin (1) |
| | | | | | | SCK3_2 | - | | Multi-function serial ch.3 clock I/O (2) |
| 7 *1 | 9 *1 | 11 *1 | 14 *1 | 17 | 21 | P034 | - | A | General-purpose I/O port |
| | | | | | | A06 *2, *3, *4, *5 | - | | External bus/Address bit6 output (0) |
| | | | | | | OCU11_1 | - | | Output compare ch.11 output (1) |
| | | | | | | ICU2_3 | - | | Input capture ch.2 input (3) |
| | | | | | | TIN5_0 | - | | Reload timer ch.5 event input (0) |
| | | | | | | RTO0_1 | - | | Waveform generator ch.0 output pin (1) |
| | | | | | | SOT3_2 | - | | Multi-function serial ch.3 serial data output (2) |
| - | - | 12 | 15 | 18 | 22 | P150 | - | F | General-purpose I/O port |
| | | | | | | SOT8_0/ SDA8 | - | | Multi-function serial ch.8 serial data output (0)/ $I^2C$ bus serial data I/O |
| | | | | | | OCU10_1 | - | | Output compare ch.10 output (1) |
| | | | | | | TRG6_0 | - | | PPG trigger 6 input (0) |
| | | | | | | ICU1_3 | - | | Input capture ch.1 input (3) |
| | | | | | | TIN6_0 | - | | Reload timer ch.6 event input (0) |
| 8 *1 | 10 *1 | 13 | 16 | 19 | 23 | P151 | - | F | General-purpose I/O port |
| | | | | | | SCK8_0/ SCL8 *2, *3 | - | | Multi-function serial ch.8 clock I/O (0)/ $I^2C$ bus serial clock I/O |
| | | | | | | OCU9_1 | - | | Output compare ch.9 output (1) |
| | | | | | | TRG7_0 | - | | PPG trigger 7 input (0) |
| | | | | | | ICU0_3 | - | | Input capture ch.0 input (3) |
| | | | | | | TIN7_0 | - | | Reload timer ch.7 event input (0) |
| | | | | | | ZIN0_2 | - | | U/D counter ch.0 ZIN input (2) |
| | | | | | | DTTI_1 | - | | Waveform generator ch.1 input pin (1) |

| Pin no. | | | | | | Pin Name | Polarity | I/O circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | - | - | 64 | 80 | P080 | - | A | General-purpose I/O port |
| | | | | | | SCS52_0 | - | | Serial chip select 52 output (0) |
| | | | | | | PPG0_0 | - | | PPG ch.0 output (0) |
| 29 | 37 | 46 | 56 | 65 | 81 | P081 | - | G | General-purpose I/O port |
| | | | | | | SOT5_0/ SDA5 | - | | Multi-function serial ch.5 serial data output (0)/I$^2$C bus serial data I/O |
| | | | | | | AN0 | - | | ADC analog 0 input |
| | | | | | | PPG1_0 | - | | PPG ch.1 output (0) |
| 30 | 38 | 47 | 57 | 66 | 82 | P082 | - | G | General-purpose I/O port |
| | | | | | | SIN5_0 | - | | Multi-function serial ch.5 serial data input (0) |
| | | | | | | AN1 | - | | ADC analog 1 input |
| | | | | | | PPG2_0 | - | | PPG ch.2 output (0) |
| - | - | - | - | 67 | 83 | P083 | - | B | General-purpose I/O port |
| | | | | | | SCS50_0 | - | | Serial chip select 50 I/O (0) |
| | | | | | | AN2 | - | | ADC analog 2 input |
| | | | | | | PPG3_0 | - | | PPG ch.3 output (0) |
| - | - | - | - | 68 | 84 | P084 | - | B | General-purpose I/O port |
| | | | | | | SCS51_0 | - | | Serial chip select 51 output (0) |
| | | | | | | AN3 | - | | ADC analog 3 input |
| | | | | | | PPG4_0 | - | | PPG ch.4 output (0) |
| - | - | - | - | 69 | 85 | P085 | - | A | General-purpose I/O port |
| | | | | | | PPG5_0 | - | | PPG ch.5 output (0) |
| - | - | 48 | 58 | 70 | 86 | P086 | - | C | General-purpose I/O port |
| | | | | | | DAO1 | - | | DAC analog 1 output |
| | | | | | | PPG6_0 | - | | PPG ch.6 output (0) |
| 31 | 39 | 49 | 59 | 71 | 87 | P087 | - | C | General-purpose I/O port |
| | | | | | | DAO0 | - | | DAC analog 0 output |
| | | | | | | PPG7_0 | - | | PPG ch.7 output (0) |
| | | | | | | INT8_0 | - | | INT8 External interrupt input (0) |
| - | - | - | - | - | 90 | P190 | - | A | General-purpose I/O port |
| | | | | | | TIN0_1 | - | | Reload timer ch.0 event input (1) |
| - | - | - | - | - | 91 | P191 | - | A | General-purpose I/O port |
| | | | | | | TIN1_1 | - | | Reload timer ch.1 event input (1) |
| - | - | - | - | 74 | 92 | P090 | - | B | General-purpose I/O port |
| | | | | | | AN4 | - | | ADC analog 4 input |
| | | | | | | ICU0_0 | - | | Input capture ch.0 input (0) |
| | | | | | | TIN2_1 | - | | Reload timer ch.2 event input (1) |
| - | - | - | - | 75 | 93 | P091 | - | B | General-purpose I/O port |
| | | | | | | AN5 | - | | ADC analog 5 input |
| | | | | | | PPG41_1 | - | | PPG ch.41 output (1) |
| | | | | | | ICU1_0 | - | | Input capture ch.1 input (0) |
| | | | | | | TIN3_1 | - | | Reload timer ch.3 event input (1) |

| Type | Circuit | Remarks |
|---|---|---|
| G |  | •Analog input, General-purpose I/O port<br>•Output 4mA<br>•Pull-up resistor control 50kΩ<br>• CMOS hysteresis input |
| H |  | •Analog input, General-purpose I/O port<br>•Output 12mA<br>•Pull-up resistor control 50kΩ<br>•Automotive input |
| I |  | • General-purpose I/O port (5V tolerant)<br>• Output 4mA<br>• CMOS hysteresis input |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000BF8_H$ | — | — | MBR [R/W] B,H,W<br>00------ XXXXXXXX | | OCDU |
| $000BFC_H$ | — | — | UER [W] B,H,W<br>-------- -------X | | |
| $000C00_H$ | DCCR0 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | DMA Controller [S] |
| $000C04_H$ | DCSR0 [R/W] H<br>0------- -----000 | | DTCR0 [R/W] H<br>00000000 00000000 | | |
| $000C08_H$ | DSAR0 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C0C_H$ | DDAR0 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C10_H$ | DCCR1 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C14_H$ | DCSR1 [R/W] H<br>0------- -----000 | | DTCR1 [R/W] H<br>00000000 00000000 | | |
| $000C18_H$ | DSAR1 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C1C_H$ | DDAR1 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C20_H$ | DCCR2 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C24_H$ | DCSR2 [R/W] H<br>0------- -----000 | | DTCR2 [R/W] H<br>00000000 00000000 | | |
| $000C28_H$ | DSAR2 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C2C_H$ | DDAR2 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C30_H$ | DCCR3 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C34_H$ | DCSR3 [R/W] H<br>0------- -----000 | | DTCR3 [R/W] H<br>00000000 00000000 | | |
| $000C38_H$ | DSAR3 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C3C_H$ | DDAR3 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000C40_H$ | DCCR4 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| $000C44_H$ | DCSR4 [R/W] H<br>0------- -----000 | | DTCR4 [R/W] H<br>00000000 00000000 | | |
| $000C48_H$ | DSAR4 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000CF0_H$ | DCCR15 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | DMA Controller [S] |
| $000CF4_H$ | DCSR15 [R/W] H<br>0------- -----000 | | DTCR15 [R/W] H<br>00000000 00000000 | | |
| $000CF8_H$ | DSAR15 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000CFC_H$ | DDAR15 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| $000D00_H$ to $000DF0_H$ | — | — | — | — | Reserved [S] |
| $000DF4_H$ | — | — | DNMIR [R/W] B<br>0------0 | DILVR [R/W] B<br>---11111 | DMA Controller [S] |
| $000DF8_H$ | DMACR[R/W] W<br>0------- -------- 0------- -------- | | | | |
| $000DFC_H$ | — | — | — | — | Reserved [S] |
| $000E00_H$ | DDR00 [R/W] B,H,W<br>00000000 | DDR01 [R/W] B,H,W<br>00000000 | DDR02 [R/W] B,H,W<br>00000000 | DDR03 [R/W] B,H,W<br>00000000 | Data Direction Register |
| $000E04_H$ | DDR04 [R/W] B,H,W<br>00000000 | DDR05 [R/W] B,H,W<br>00000000 | DDR06 [R/W] B,H,W<br>00000000 | DDR07 [R/W] B,H,W<br>00000000 | |
| $000E08_H$ | DDR08 [R/W] B,H,W<br>00000000 | DDR09 [R/W] B,H,W<br>00000000 | DDR10 [R/W] B,H,W<br>00000000 | DDR11 [R/W] B,H,W<br>00000000 | Data Direction Register |
| $000E0C_H$ | DDR12 [R/W] B,H,W<br>00000000 | DDR13 [R/W] B,H,W<br>-0000000 | DDR14 [R/W] B,H,W<br>---000-- | DDR15 [R/W] B,H,W<br>--000000 | |
| $000E10_H$ | — | — | — | — | |
| $000E14_H$ | — | — | — | — | |
| $000E18_H$ | DDR16 [R/W] B,H,W<br>00000000 | DDR17 [R/W] B,H,W<br>00000000 | DDR18 [R/W] B,H,W<br>00000000 | DDR19 [R/W] B,H,W<br>00000000 | |
| $000E1C_H$ | — | — | — | — | Reserved |
| $000E20_H$ | PFR00 [R/W] B,H,W<br>00000000 | PFR01 [R/W] B,H,W<br>00000000 | PFR02 [R/W] B,H,W<br>00000000 | PFR03 [R/W] B,H,W<br>00000000 | Port Function Register |
| $000E24_H$ | PFR04 [R/W] B,H,W<br>00000000 | PFR05 [R/W] B,H,W<br>00000000 | PFR06 [R/W] B,H,W<br>00000000 | PFR07 [R/W] B,H,W<br>00000000 | |
| $000E28_H$ | PFR08 [R/W] B,H,W<br>00000000 | PFR09 [R/W] B,H,W<br>00000000 | PFR10 [R/W] B,H,W<br>00000000 | PFR11 [R/W] B,H,W<br>00000000 | |
| $000E2C_H$ | PFR12 [R/W] B,H,W<br>00000000 | PFR13 [R/W] B,H,W<br>-0000000 | PFR14 [R/W] B,H,W<br>---000-- | PFR15 [R/W] B,H,W<br>--000000 | |
| $000E30_H$ | — | — | — | — | |
| $000E34_H$ | — | — | — | — | |
| $000E38_H$ | PFR16 [R/W] B,H,W<br>00000000 | PFR17 [R/W] B,H,W<br>00000000 | PFR18 [R/W] B,H,W<br>00000000 | PFR19 [R/W] B,H,W<br>00000000 | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001D70$_H$ to 001FFC$_H$ | — | — | — | — | Reserved |
| 002000$_H$ | CTRLR0 [R/W] B,H,W<br>-------- 000-0001 | | STATR0 [R/W] B,H,W<br>-------- 00000000 | | CAN0 (128msb) |
| 002004$_H$ | ERRCNT0 [R] B,H,W<br>00000000 00000000 | | BTR0 [R/W] B,H,W<br>-0100011 00000001 | | |
| 002008$_H$ | INTR0 [R] B,H,W<br>00000000 00000000 | | TESTR0 [R/W] B,H,W<br>-------- X00000-- | | |
| 00200C$_H$ | BRPER0 [R/W] B,H,W<br>-------- ----0000 | | — | — | |
| 002010$_H$ | IF1CREQ0 [R/W] B,H,W<br>0------- 00000001 | | IF1CMSK0 [R/W] B,H,W<br>-------- 00000000 | | |
| 002014$_H$ | IF1MSK20 [R/W] B,H,W<br>11-11111 11111111 | | IF1MSK10 [R/W] B,H,W<br>11111111 11111111 | | |
| 002018$_H$ | IF1ARB20 [R/W] B,H,W<br>00000000 00000000 | | IF1ARB10 [R/W] B,H,W<br>00000000 00000000 | | |
| 00201C$_H$ | IF1MCTR0 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002020$_H$ | IF1DTA10 [R/W] B,H,W<br>00000000 00000000 | | IF1DTA20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002024$_H$ | IF1DTB10 [R/W] B,H,W<br>00000000 00000000 | | IF1DTB20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002028$_H$ | — | — | — | — | |
| 00202C$_H$ | — | — | — | — | |
| 002030$_H$, 002034$_H$ | Reserved(IF1 data mirror) | | | | |
| 002038$_H$ | — | — | — | — | |
| 00203C$_H$ | — | — | — | — | |
| 002040$_H$ | IF2CREQ0 [R/W] B,H,W<br>0------- 00000001 | | IF2CMSK0 [R/W] B,H,W<br>-------- 00000000 | | |
| 002044$_H$ | IF2MSK20 [R/W] B,H,W<br>11-11111 11111111 | | IF2MSK10 [R/W] B,H,W<br>11111111 11111111 | | |
| 002048$_H$ | IF2ARB20 [R/W] B,H,W<br>00000000 00000000 | | IF2ARB10 [R/W] B,H,W<br>00000000 00000000 | | |
| 00204C$_H$ | IF2MCTR0 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002050$_H$ | IF2DTA10 [R/W] B,H,W<br>00000000 00000000 | | IF2DTA20 [R/W] B,H,W<br>00000000 00000000 | | |

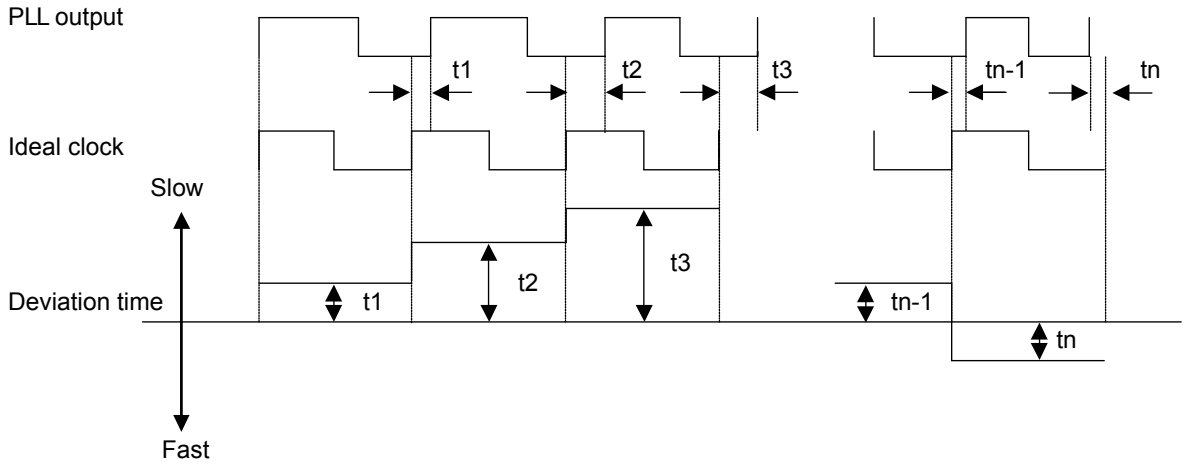
| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $002054_H$ | IF2DTB10 [R/W] B,H,W<br>00000000 00000000 | | IF2DTB20 [R/W] B,H,W<br>00000000 00000000 | | CAN0<br>(128msb) |
| $002058_H$ | — | — | — | — | |
| $00205C_H$ | — | — | — | — | |
| $002060_H$, $002064_H$ | Reserved(IF2 data mirror) | | | | |
| $002068_H$ to $00207C_H$ | — | | | | |
| $002080_H$ | TREQR20 [R] B,H,W<br>00000000 00000000 | | TREQR10 [R] B,H,W<br>00000000 00000000 | | |
| $002084_H$ | TREQR40 [R] B,H,W<br>00000000 00000000 | | TREQR30 [R] B,H,W<br>00000000 00000000 | | |
| $002088_H$ | TREQR60 [R] B,H,W<br>00000000 00000000 | | TREQR50 [R] B,H,W<br>00000000 00000000 | | |
| $00208C_H$ | TREQR80 [R] B,H,W<br>00000000 00000000 | | TREQR70 [R] B,H,W<br>00000000 00000000 | | |
| $002090_H$ | NEWDT20 [R] B,H,W<br>00000000 00000000 | | NEWDT10 [R] B,H,W<br>00000000 00000000 | | |
| $002094_H$ | NEWDT40 [R] B,H,W<br>00000000 00000000 | | NEWDT30 [R] B,H,W<br>00000000 00000000 | | |
| $002098_H$ | NEWDT60 [R] B,H,W<br>00000000 00000000 | | NEWDT50 [R] B,H,W<br>00000000 00000000 | | |
| $00209C_H$ | NEWDT80 [R] B,H,W<br>00000000 00000000 | | NEWDT70 [R] B,H,W<br>00000000 00000000 | | |
| $0020A0_H$ | INTPND20 [R] B,H,W<br>00000000 00000000 | | INTPND10 [R] B,H,W<br>00000000 00000000 | | |
| $0020A4_H$ | INTPND40 [R] B,H,W<br>00000000 00000000 | | INTPND30 [R] B,H,W<br>00000000 00000000 | | |
| $0020A8_H$ | INTPND60 [R] B,H,W<br>00000000 00000000 | | INTPND50 [R] B,H,W<br>00000000 00000000 | | |
| $0020AC_H$ | INTPND80 [R] B,H,W<br>00000000 00000000 | | INTPND70 [R] B,H,W<br>00000000 00000000 | | |
| $0020B0_H$ | MSGVAL20 [R] B,H,W<br>00000000 00000000 | | MSGVAL10 [R] B,H,W<br>00000000 00000000 | | |
| $0020B4_H$ | MSGVAL40 [R] B,H,W<br>00000000 00000000 | | MSGVAL30 [R] B,H,W<br>00000000 00000000 | | |
| $0020B8_H$ | MSGVAL60 [R] B,H,W<br>00000000 00000000 | | MSGVAL50 [R] B,H,W<br>00000000 00000000 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $002300_H$ | DFCTLR [R/W] B,H,W<br>-0------ -------- | | — | DFSTR [R/W] B,H,W<br>-----001 | WorkFlash |
| $002304_H$ | — | — | — | — | |
| $002308_H$ | FLIFCTLR [R/W]<br>B,H,W<br>---0--00 | — | FLIFFER1 [R/W]<br>B,H,W<br>-------- | FLIFFER2 [R/W]<br>B,H,W<br>-------- | Flash /<br>WorkFlash |
| $00230C_H$<br>to<br>$0023FC_H$ | — | | | | Reserved |
| $002400_H$ | SEEARX [R] B,H,W<br>-0000000 00000000 | | DEEARX [R] B,H,W<br>-0000000 00000000 | | XBS RAM<br>ECC control |
| $002404_H$ | EECSRX [R/W]<br>B,H,W<br>----00-- | — | EFEARX [R/W] B,H,W<br>-0000000 00000000 | | |
| $002408_H$ | — | EFECRX [R/W] B,H,W<br>-------0 00000000 00000000 | | | |
| $00240C_H$<br>to<br>$002FFC_H$ | — | | | | Reserved |
| $003000_H$ | SEEARA [R] B,H,W<br>-----000 00000000 | | DEEARA [R] B,H,W<br>-----000 00000000 | | Backup RAM<br>ECC control |
| $003004_H$ | EECSRA [R/W]<br>B,H,W<br>----00-- | — | EFEARA [R/W] B,H,W<br>-----000 00000000 | | |
| $003008_H$ | — | EFECRA [R/W] B,H,W<br>-------0 00000000 00000000 | | | |
| $00300C_H$ | TEAR0X[R] B,H,W<br>000----- -------- -0000000 00000000 | | | | RAM/ diagnosis<br>XBS RAM |
| $003010_H$ | TEAR1X[R] B,H,W<br>000----- -------- -0000000 00000000 | | | | |
| $003014_H$ | TEAR2X[R] B,H,W<br>000----- -------- -0000000 00000000 | | | | |
| $003018_H$ | TAEARX [R/W] B,H,W<br>-1111111 11111111 | | TASARX [R/W] B,H,W<br>-0000000 00000000 | | |
| $00301C_H$ | TFECRX [R/W]<br>B,H,W<br>----0000 | TICRX [R/W]<br>B,H,W<br>----0000 | TTCRX [R/W] B,H,W<br>------00 00001100 | | |
| $003020_H$ | TSRCRX [W]<br>B,H,W<br>0------- | — | — | TKCCRX [R/W]<br>B,H,W<br>00----00 | |
| $003024_H$<br>to<br>$00302C_H$ | — | | | | Reserved |

| Interrupt factor | Interrupt number | | Interrupt level | Offset | Default address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexadecimal | | | | |
| Multi-function serial interface ch.8 (reception completed)<br>Multi-function serial interface ch.8 (status)<br>16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | 45 | 2D | ICR29 | $348_H$ | $000FFF48_H$ | 29*1 |
| Main timer<br>Sub timer<br>PLL timer<br>Multi-function serial interface ch.8 (transmission completed)<br>16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | 46 | 2E | ICR30 | $344_H$ | $000FFF44_H$ | 30 |
| Clock calibration unit (sub oscillation)<br>Multi-function serial interface ch.9 (reception completed)<br>Multi-function serial interface ch.9 (status) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1, *4 |
| A/D converter 0/1/7/9/10/11/12/13/14/15/16 17/18/19/22/23/26/27/28/29/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit (CR oscillation)<br>Multi-function serial interface ch.9 (transmission completed)<br>16-bit OCU 0 (match) / 16-bit OCU 1 (match) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| 32-bit Free-run timer 4<br>16-bit OCU 2 (match) / 16-bit OCU 3 (match) | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 32-bit Free-run timer 3/5<br>16-bit OCU 4 (match) / 16-bit OCU 5 (match) | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35*5 |
| 32-bit ICU6 (fetching/measurement)<br>Multi-function serial interface ch.10 (reception completed)<br>Multi-function serial interface ch.10 (status) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| 32-bit ICU7 (fetching/measurement)<br>Multi-function serial interface ch.10 (transmission completed) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| 32-bit ICU8 (fetching/measurement)<br>Multi-function serial interface ch.11 (reception completed)<br>Multi-function serial interface ch.11 (status) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| 32-bit ICU9 (fetching/measurement)<br>WG dead timer underflow 0/1/2<br>WG dead timer reload 0/1/2<br>WG DTTI 0 | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| 32-bit ICU4 (fetching/measurement)<br>Multi-function serial interface ch.11 (transmission completed) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |

• CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

($T_A$: -40°C to +125°C, $V_{CC}$= $AV_{CC}$=5.0V ± 10%/$V_{CC}$=$AV_{CC}$=3.3V±0.3V, $V_{SS}$=$AV_{SS}$=0.0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK11 | - | $4t_{CPP}$ | - | ns | Internal shift clock mode output pin : $C_L$=50pF |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | -30 | 30 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | -300 | 300 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11 | | 34 | - | ns | |
| | | SCK3 , SCK4 SIN3 , SIN4 | | 300 | - | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK11 SIN0 to SIN11 | | 0 | - | ns | |
| Serial clock "H"pulse width | $t_{SHSL}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | External shift clock mode output pin: $C_L$=50pF |
| Serial clock "L" pulse width | $t_{SLSH}$ | | | $2t_{CPP}$-10 | - | ns | |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | - | 33 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | - | 300 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCK0 to SCK11 SIN0 to SIN11 | | 10 | - | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | | | 20 | - | ns | |
| SCK fall time | $t_F$ | SCK0 to SCK11 | | - | 5 | ns | |
| SCK rise time | $t_R$ | SCK0 to SCK11 | | - | 5 | ns | |

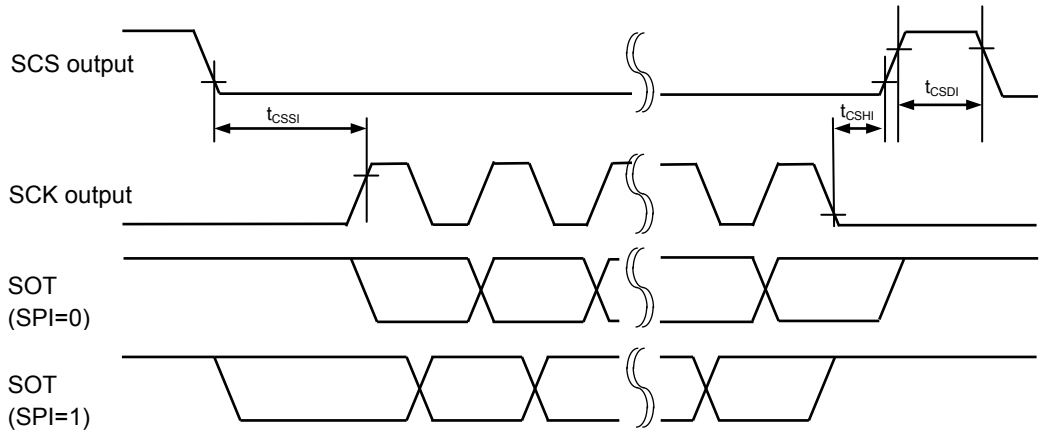
**Notes:**

AC characteristic in CLK synchronized mode.

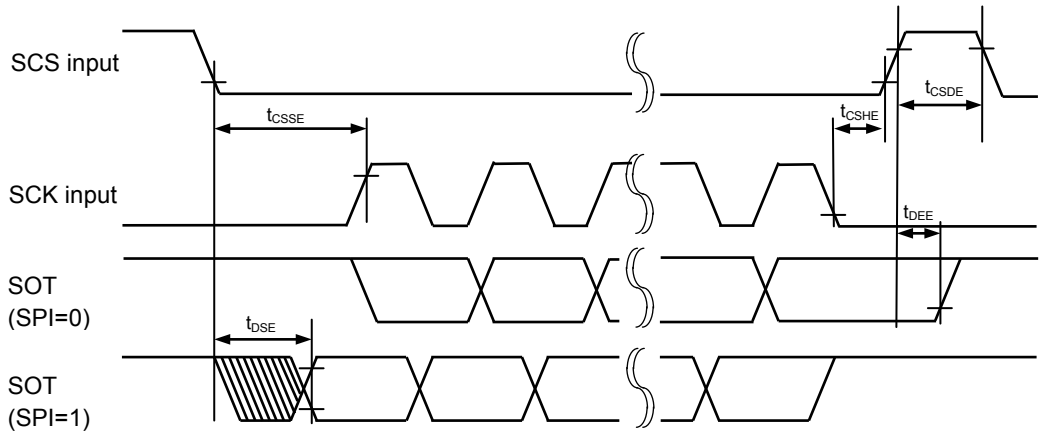
$C_L$ is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.



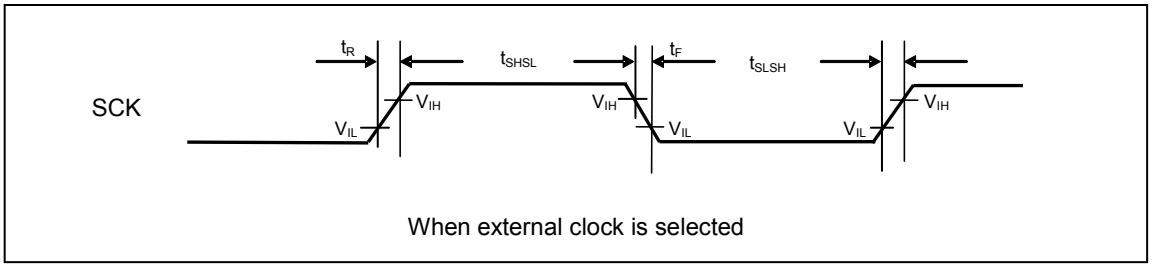

When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode




When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
External shift clock mode

(4-3) LIN Interface (v2.1)( Asynchronous Serial Interface for LIN (v2.1)) timing
Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1
($T_A$:-40°C to +125°C, $V_{CC}$=$AV_{CC}$=5.0V±10%/$V_{CC}$=$AV_{CC}$=3.3V±0.3V, $V_{SS}$=$AV_{SS}$=0.0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | output pin: $C_L$=50pF |
| Serial clock "H"pulse width | $t_{SHSL}$ | | | $t_{CPP}$+10 | - | ns | |
| SCK fall time | $t_F$ | | | - | 5 | ns | |
| SCK rise time | $t_R$ | | | - | 5 | ns | |

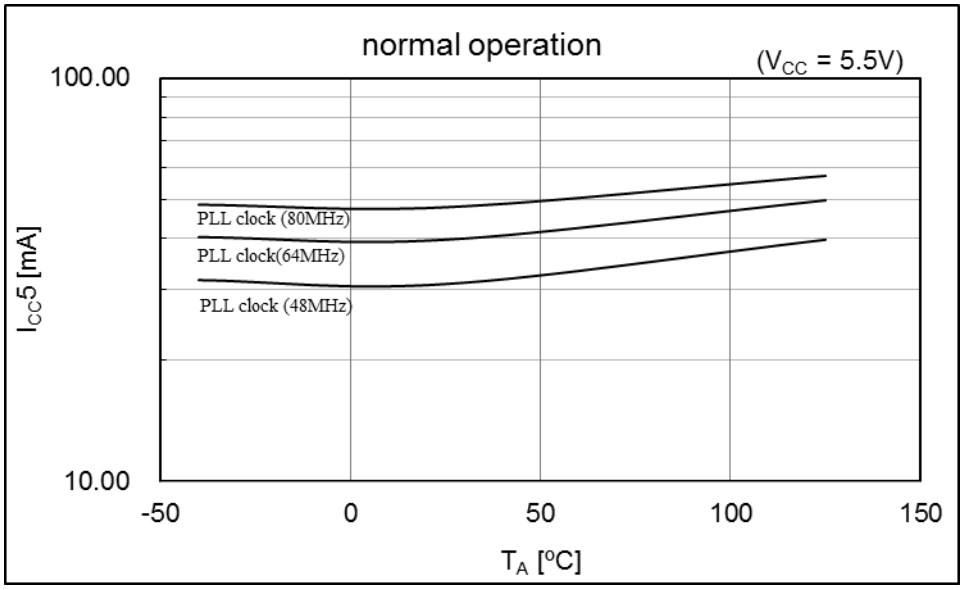


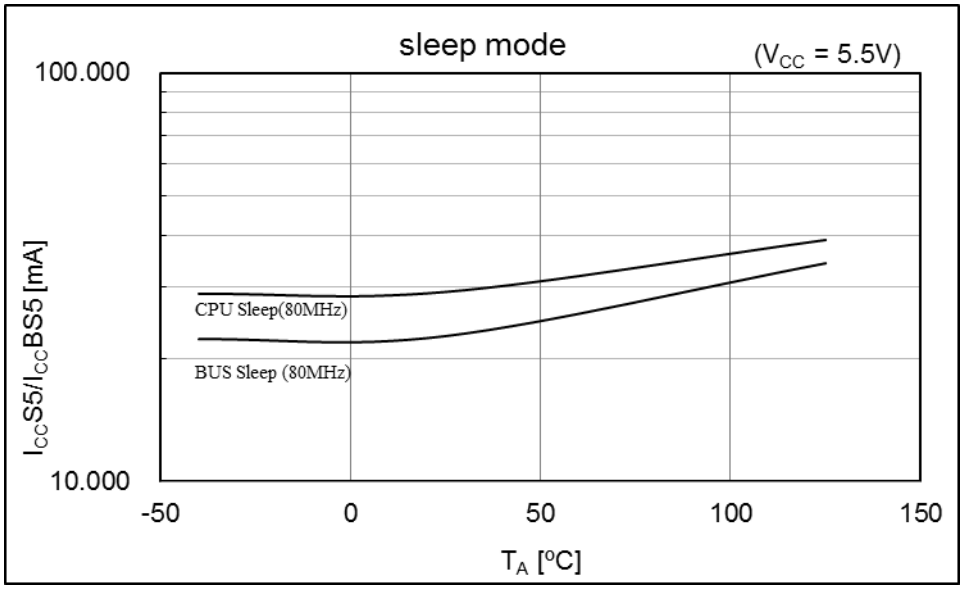

When external clock is selected

## 12. EXAMPLE CHARACTERISTICS

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

MB91F526



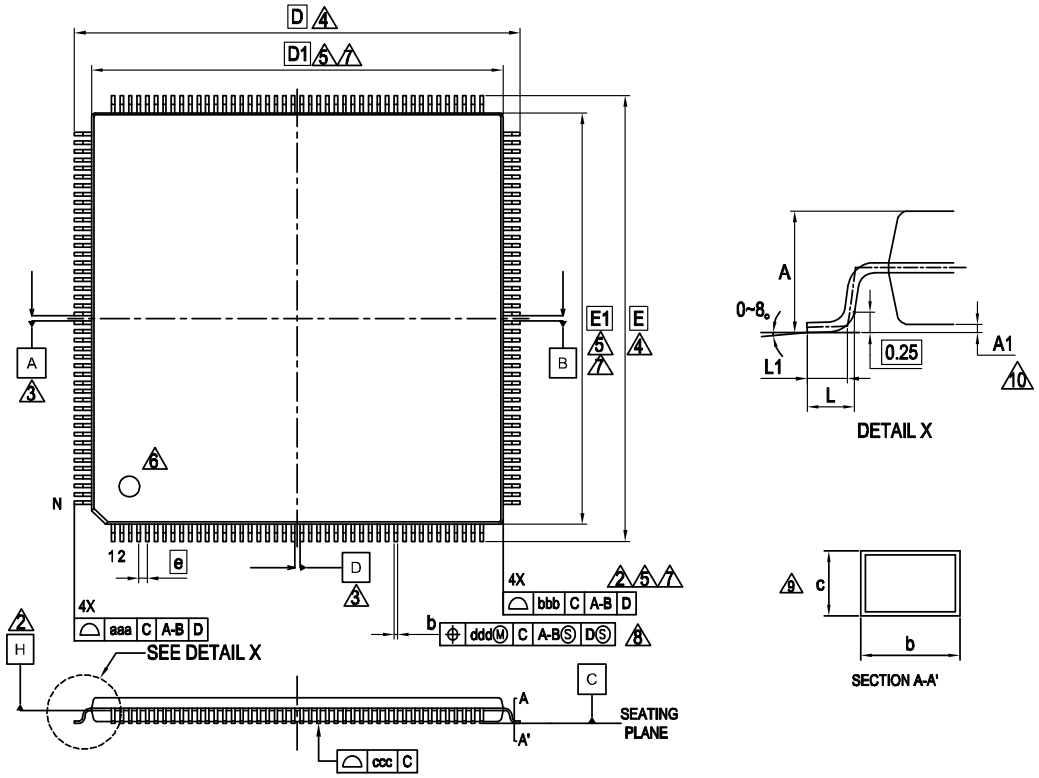



## 15. Ordering Information MB91F52xxxD

| Part number | Sub clock | CSV Initial value | LVD Initial value | Package* |
|---|---|---|---|---|
| MB91F526LWDPMC | Yes | ON | ON | LQP・176 pin, Plastic |
| MB91F526LJDPMC | | OFF | ON | |
| MB91F525LWDPMC | | ON | ON | |
| MB91F525LJDPMC | | OFF | ON | |
| MB91F524LWDPMC | | ON | ON | |
| MB91F524LJDPMC | | OFF | ON | |
| MB91F523LWDPMC | | ON | ON | |
| MB91F523LJDPMC | | OFF | ON | |
| MB91F522LWDPMC | | ON | ON | |
| MB91F522LJDPMC | | OFF | ON | |
| MB91F526LSDPMC | None | ON | ON | |
| MB91F526LHDPMC | | OFF | ON | |
| MB91F525LSDPMC | | ON | ON | |
| MB91F525LHDPMC | | OFF | ON | |
| MB91F524LSDPMC | | ON | ON | |
| MB91F524LHDPMC | | OFF | ON | |
| MB91F523LSDPMC | | ON | ON | |
| MB91F523LHDPMC | | OFF | ON | |
| MB91F522LSDPMC | | ON | ON | |
| MB91F522LHDPMC | | OFF | ON | |
| MB91F526KWDPMC | Yes | ON | ON | LQS・144 pin, (Lead pitch 0.5mm) Plastic |
| MB91F526KJDPMC | | OFF | ON | |
| MB91F525KWDPMC | | ON | ON | |
| MB91F525KJDPMC | | OFF | ON | |
| MB91F524KWDPMC | | ON | ON | |
| MB91F524KJDPMC | | OFF | ON | |
| MB91F523KWDPMC | | ON | ON | |
| MB91F523KJDPMC | | OFF | ON | |
| MB91F522KWDPMC | | ON | ON | |
| MB91F522KJDPMC | | OFF | ON | |
| MB91F526KSDPMC | None | ON | ON | |
| MB91F526KHDPMC | | OFF | ON | |
| MB91F525KSDPMC | | ON | ON | |
| MB91F525KHDPMC | | OFF | ON | |
| MB91F524KSDPMC | | ON | ON | |
| MB91F524KHDPMC | | OFF | ON | |
| MB91F523KSDPMC | | ON | ON | |
| MB91F523KHDPMC | | OFF | ON | |
| MB91F522KSDPMC | | ON | ON | |
| MB91F522KHDPMC | | OFF | ON | |

| Part number | Sub clock | CSV Initial value | LVD Initial value | Package* |
|---|---|---|---|---|
| MB91F526KWDPMC1 | Yes | ON | ON | LQN・144 pin, (Lead pitch 0.4mm) Plastic |
| MB91F526KJDPMC1 | | OFF | ON | |
| MB91F525KWDPMC1 | | ON | ON | |
| MB91F525KJDPMC1 | | OFF | ON | |
| MB91F524KWDPMC1 | | ON | ON | |
| MB91F524KJDPMC1 | | OFF | ON | |
| MB91F523KWDPMC1 | | ON | ON | |
| MB91F523KJDPMC1 | | OFF | ON | |
| MB91F522KWDPMC1 | | ON | ON | |
| MB91F522KJDPMC1 | | OFF | ON | |
| MB91F526KSDPMC1 | None | ON | ON | |
| MB91F526KHDPMC1 | | OFF | ON | |
| MB91F525KSDPMC1 | | ON | ON | |
| MB91F525KHDPMC1 | | OFF | ON | |
| MB91F524KSDPMC1 | | ON | ON | |
| MB91F524KHDPMC1 | | OFF | ON | |
| MB91F523KSDPMC1 | | ON | ON | |
| MB91F523KHDPMC1 | | OFF | ON | |
| MB91F522KSDPMC1 | | ON | ON | |
| MB91F522KHDPMC1 | | OFF | ON | |
| MB91F526JWDPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| MB91F526JJDPMC | | OFF | ON | |
| MB91F525JWDPMC | | ON | ON | |
| MB91F525JJDPMC | | OFF | ON | |
| MB91F524JWDPMC | | ON | ON | |
| MB91F524JJDPMC | | OFF | ON | |
| MB91F523JWDPMC | | ON | ON | |
| MB91F523JJDPMC | | OFF | ON | |
| MB91F522JWDPMC | | ON | ON | |
| MB91F522JJDPMC | | OFF | ON | |
| MB91F526JSDPMC | None | ON | ON | |
| MB91F526JHDPMC | | OFF | ON | |
| MB91F525JSDPMC | | ON | ON | |
| MB91F525JHDPMC | | OFF | ON | |
| MB91F524JSDPMC | | ON | ON | |
| MB91F524JHDPMC | | OFF | ON | |
| MB91F523JSDPMC | | ON | ON | |
| MB91F523JHDPMC | | OFF | ON | |
| MB91F522JSDPMC | | ON | ON | |
| MB91F522JHDPMC | | OFF | ON | |

## LQP176 , 176 Lead Plastic Low Profile Quad Flat Package




| PACKAGE | LQP176 | | |
|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 26.00 BSC. | | |
| D1 | 24.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 26.00 BSC. | | |
| E1 | 24.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| aaa | — | — | 0.20 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.08 |
| N | 176 | | |

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>20</td><td>■PIN Description</td><td>A List of "Pin Description" modified.<br><br>(Error)
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<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
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<tr><td>WR1X</td></tr>
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<tr><td>PPG25_0</td></tr>
<tr><td>TIN2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">13</td><td>P172</td></tr>
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<tr><td>A05</td></tr>
<tr><td>PPG31_0</td></tr>
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<tr><td>TIN4_0</td></tr>
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<tr><td>ICU4_2</td></tr>
<tr><td>PPG16_1</td></tr>
<tr><td>ICU3_0</td></tr>
<tr><td>TOT2_1*2, *3</td></tr>
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</td></tr>
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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | Package<br>↓<br>Package*2<br>Added the following description.<br>*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.<br>Corrected the following description.<br>For details of the package, see "■ PACKAGE DIMENSIONS ".<br>↓<br>*2: For details of the package, see "■ PACKAGE DIMENSIONS ".<br>Added the following description.<br>• ORDERING INFORMATION MB91F52xxxC<br>Company name and layout design change |
| *A | 4999456 | JHMU | 11/13/2015 | Updated to Cypress template.<br>Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in “Absolute Maximum Ratings” of “ELECTRICAL CHARACTERISTICS”.<br>*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.<br>*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.<br>Added Errata section. |
| *B | 5112138 | KUME | 01/28/2016 | Fixed some clerical errors.<br>For details, please see the chapter 18. Major Changes. |
| *C | 5196285 | KUME | 04/28/2016 | For details, please see the chapter 19. Major Changes. |
| *D | 5318862 | KUME | 06/23/2016 | For details, please see the chapter 19. Major Changes. |