





Welcome to **E-XFL.COM** 

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

- · ·	
Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526fsbpmc-gse2



Product lineup comparison 80 pins

Product lineup comparison 80 pins	1	T	T	T	1	
	MB91F522D	MB91F523D	MB91F524D	MB91F525D	MB91F526D	
System Clock	On chip PLL Clock multiple method					
Minimum instruction execution time	12.5ns (80MHz)					
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB	
Flash Capacity (Data)			64KB			
RAM Capacity	(48+8	3)KB	(64+8)KB	(96+8)KB	(128+8)KB	
External BUS I/F (22address/16data/4cs)			None			
DMA Transfer			16ch			
16-bit Base Timer			1ch			
Free-run Timer		161	oit×3ch, 32bit×2	2ch		
Input capture			oit×4ch, 32bit×5			
Output Compare			bit×6ch, 32bit×4			
16-bit Reload Timer		101	7ch	FOIT		
PPG			16bit×27ch			
Up/down Counter			2ch			
Clock Supervisor			Yes			
External Interrupt			8ch×2units			
A/D converter		12bit×16ch	(1unit), 12bit×1	16ch (1unit)		
D/A converter (8bit)			1ch			
Multi-Function Serial Interface			9ch*1			
CAN		64ms	g×2ch/128msg	x1ch		
Hardware Watchdog Timer		O IIIIc	Yes	1011		
CRC Formation			Yes			
Low-voltage detection reset			Yes			
Flash Security			Yes			
ECC Flash/WorkFlash			Yes			
ECC RAM			Yes			
Memory Protection Function (MPU)			Yes			
Floating point arithmetic (FPU)			Yes			
Real Time Clock (RTC)			Yes			
General-purpose port (#GPIOs)			56 ports			
SSCG			Yes			
Sub clock			Yes			
CR oscillator			Yes			
NMI request function			Yes			
OCD (On Chip Debug)			Yes			
TPU (Timing Protection Unit)			Yes			
Key code register			Yes			
Waveform generator			6ch			
Operation guaranteed temperature (T <sub>A</sub> )		-	40°C to +125°C			
Power supply			2.7V to 5.5V *2			
Package			LQH080			

<sup>\*1:</sup> Only channel 5, channel 6 and channel 11 support the I<sup>2</sup>C (standard mode).

<sup>\*2:</sup> The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.



Pin no.		Pin Name Polarity		I/O circuit	Function* <sup>9</sup>				
64	80	100	120	144	176	Name		types*8	
						P057	-		General-purpose I/O port
						RDY *2, *3, *4, *5	-		External bus/Ready input (0)
						SCK10_1	-		Multi-function serial ch.10 clock I/O (1)
19	24	*4	*4			AN42	-	_	ADC analog 42 input
*1	*1	29 *1	35 *1	41	51	ICU8_0	-	G	Input capture ch.8 input (0)
						TRG0_2	-		PPG trigger 0 input (2)
						PPG1_1	-		PPG ch.1 output (1)
						ICU1_1	-		Input capture ch.1 input (1)
						TIN6_1	-		Reload timer ch.6 event input (1)
						P142	-		General-purpose I/O port
						SCK10_0			Multi-function serial ch.10 clock I/O (0)/
-	-	-	-	44	54	/ SCL10	-	F	I <sup>2</sup> C bus serial clock I/O
						PPG38_0	-		PPG ch.38 output (0)
						TIN7_1	-		Reload timer ch.7 event input (1)
						P143	-		General-purpose I/O port
						SOT10_0			Multi-function serial ch.10 serial data output
-	-	-	-	45	55	/SDA10	-	F	(0)/ I <sup>2</sup> C bus serial data I/O
						PPG39_0	-		PPG ch.39 output (0)
						TOT4_1	-		Reload timer ch.4 output (1)
		_		_	56	P182	-	Α	General-purpose I/O port
				_	30	PPG42_0	-		PPG ch.42 output (0)
						P060	-		General-purpose I/O port
						SCS10_0	-		Serial chip select 10 I/O (0)
		32	38	46	57	PPG2_1	-	Α	PPG ch.2 output (1)
-	_	32	38	8 46	37	ICU2_1	-	^	Input capture ch.2 input (1)
						TOT5_1	-		Reload timer ch.5 output (1)
						INT13_0	-		INT13 External interrupt input (0)
						P061	-		General-purpose I/O port
						SOT10 1	_		Multi-function serial ch.10
						_			serial data output (1)
						AN41	-		ADC analog 41 input
22	27	33	39	47	58	ICU6_0	-	В	Input capture ch.6 input (0)
						PPG3_1	-		PPG ch.3 output (1)
						ICU3_1	-		Input capture ch.3 input (1)
						TOT6_1	-		Reload timer ch.6 output (1)
						INT13_1	-		INT13 External interrupt input (1)



Polarity   Circuit types*8	et 10 I/O (1) et 40 I/O (0) input t (1) 0 clock input (0) .7 output (1) 1 ZIN input (1) e I/O port et 41 output (0) input
SCS10_1   Serial chip select   ADC analog 40   PPG ch.4 output   Free-run timer 0   Reload timer ch.   U/D counter ch.   U/D counter ch.   Serial chip select   U/D counter ch.   Serial chip select   Serial chip select	et 10 I/O (1) et 40 I/O (0) input t (1) 0 clock input (0) .7 output (1) 1 ZIN input (1) e I/O port et 41 output (0) input
SCS40_0   Serial chip select	ct 40 I/O (0) input t (1) 0 clock input (0) .7 output (1) 1 ZIN input (1) e I/O port ct 41 output (0) input
23 28 34 40 48 59 AN40 - PPG4_1 - PPG ch.4 output Free-run timer 0  TOT7_1 - Reload timer ch.  ZIN1_1 - U/D counter ch.  P063 - SCS41_0 - Serial chip select  AN39 - PPG ch.5 output  B ADC analog 40 PPG ch.4 output Free-run timer 0 Reload timer ch.  General-purpose Scrial chip select AN39 - PPG5_1 - B PPG ch.5 output	input t (1) clock input (0) r output (1) 1 ZIN input (1) e I/O port ct 41 output (0) input
23   28   34   40   48   59     PPG4_1   -     FRCK0_0   -     Free-run timer 0     Reload timer ch.	t (1) 0 clock input (0) .7 output (1) 1 ZIN input (1) e I/O port ct 41 output (0) input
PPG4_1 - PPG ch.4 outpu FRCK0_0 - Reload timer ch  TOT7_1 - U/D counter ch.  V/D counter ch.  P063 - General-purpose SCS41_0 - Serial chip select AN39 - ADC analog 39 PPG ch.5 outpu	1 clock input (0) 1.7 output (1) 1 ZIN input (1) 1 I/O port 1 tt 41 output (0) 1 input
TOT7_1 - Reload timer ch.  ZIN1_1 - U/D counter ch.  P063 - General-purpose SCS41_0 - Serial chip select AN39 - ADC analog 39 PPG ch.5 output	.7 output (1) 1 ZIN input (1) e I/O port ct 41 output (0) input
ZIN1_1 - U/D counter ch.  P063 - General-purpose SCS41_0 - AN39 - ADC analog 39 PPG ch.5 output	1 ZIN input (1) e I/O port ct 41 output (0) input
P063 - General-purpose SCS41_0 - Serial chip select AN39 - B PPG ch.5 output	e I/O port ct 41 output (0) input
SCS41_0 - Serial chip selection   AN39 - ADC analog 39 PPG5_1 - B  Serial chip selection   ADC analog 39 PPG ch.5 output	ct 41 output (0) input
- 29 35 41 49 60 AN39 - B ADC analog 39 PPG ch.5 output	input
- 29 35 41 49 60 PPG5_1 - B PPG ch.5 outpu	•
PPG5_1 - PPG ch.5 outpu	
FRCK1_0 - Free-run timer 1	t (1)
	clock input (0)
BIN1_1 - U/D counter ch.	1 BIN input (1)
P183 - General-purpose	e I/O port
61 PPG43_0 - A PPG ch.43 outp	ut (0)
P064 - General-purpose	e I/O port
SCS42_0 - Serial chip select	ct 42 output (0)
ADC analog 38	input
24   30   36   42   50   62   FRCK2_0   -   B   Free-run timer 2	clock input (0)
AIN1_1 - U/D counter ch.	1 AIN input (1)
PPG43_1 - PPG ch.43 outp	ut (1)
P065 - General-purpose	e I/O port
SCS43_0 - Serial chip select	ct 43 output (0)
37 43 51 63 FRCK3_0 - A Free-run timer 3	clock input (0)
ZIN0_1 - U/D counter ch.0	0 ZIN input (1)
PPG44_1 - PPG ch.44 outp	ut (1)
P184 - General-purpose	e I/O port
64 PPG44_0 - A PPG ch.44 outp	ut (0)
P185 - General-purpose	e I/O port
65 PPG45_0 - A PPG ch.45 outp	ut (0)
P066 - General-purpose	e I/O port
SOT4_2 - Multi-function se serial data outs	
25 31 38 44 52 66 <u>SCS3_0 - B Serial chip selectors</u> AN37 - ADC analog 37	` '
FRCK4_0 - Free-run timer 4	•
BINO_1 - U/D counter ch.	. , ,
P067 - General-purpose	, , ,
AN36 - ADC analog 36	
- 32 39 45 53 67 FRCK5_0 - B Free-run timer 5	•
AINO_1 - U/D counter ch.	



## 9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map

Address	Address offset value/ register name						
Addiess	+0	+1	+2	+3	Block		
000090 <sub>H</sub>	BT1TM	IR[R] H	BT1TMCR[	•			
	00000000	0000000	00000000	00000000			
000094 н	-	BT1STC[R/W] B 00000000	-	-	Dana timan 4		
000000	BT1PCSR/BT1	IPRLL[R /W] H	BT1PDU T/BT1PRL	H/BT1DTBF[R/W] H	Base timer 1		
000098 н	00000000	00000000	00000000	00000000			
000000	BTSEL[R/W] B		BTSSSR[W] B,H				
00009С <sub>н</sub>	000 0	=					
0000A0 <sub>H</sub>	ADERH [R	W]B, H, W	ADERL [R/	W]B, H, W			
0000A0 H	00000000	00000000	00000000				
0000A4 <sub>н</sub>	ADCS1 [R/W] B, H,W	ADCS0 [R/W] B, H,W	ADCR1 [R] B, H,W	ADCR0 [R] B, H,W	A/D converter		
0000A4 H	00000000	00000000	XX	XXXXX XXX	A B converter		
0000А8 н	ADCT1 [R/W] B, H,W	ADCT0 [R/W] B, H,W	ADSCH [R/W] B, H,W	ADECH [R/W] B, H,W			
0000А0 Н	00010000	00101100	00000	00000			
				Data access attribution B: Byte H: Half-word W: Word (Note)The access attribution is disabled.			

The initial register value after reset indicates as follows:

- · "1": Initial value "1"
- · "0": Initial value "0"
- · "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- · "\*": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.



A 1.1		<b>6</b> 11				
Address	+0	+1	+2	+3	Block	
0001F8 <sub>H</sub>	TMRLRAI XXXXXXXX	Dalaad Timaa C				
0001FC <sub>н</sub>	TMRLRB0 XXXXXXXX	Reload Timer 6				
000200 <sub>H</sub> to 000238 <sub>H</sub>	_	_	_			
00023С <sub>н</sub>	DACR0 [R/W] B,H,W 0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W	DADR1 [R/W] B,H,W XXXXXXXX	DA Converter	
000240 <sub>H</sub>			[R/W] W 11111111 11111111			
000244н		TCDT3 00000000 00000000	[R/W] W 00000000 00000000		Free-run Timer 3 32-bit FRT	
000248н	TCCSH3 [R/W] B,H,W 000	TCCSL3 [R/W] B,H,W -1-00000	_	_	02 BRT KT	
00024Сн						
000250н		Free-run Timer 4 32-bit FRT				
000254н	TCCSH4 [R/W] B,H,W 000	TCCSL4 [R/W] B,H,W -1-00000	_	_		
000258 <sub>Н</sub> to 0002C0 <sub>Н</sub>	_	_	_	_	Reserved	
0002C4 <sub>H</sub> to 0002FC <sub>H</sub>	_	_	_	_	Reserved	
000300 <sub>H</sub> to 00030C <sub>H</sub>	_	_	_	_	Reserved	
000310 <sub>H</sub>	_	_	MPUCR 000000-0			
000314 <sub>H</sub>	_	_	_	_		
000318 <sub>H</sub>		_	_		MPU [S]	
00031С <sub>н</sub>	_	(Only CPU core can access this area)				
000320н	XX		R [R] W XXXXXXXX XXXXX	XX	arou)	
000324н	_	_	DPVSR 0	= =		



Addusses		Disak			
Address -	+0	+1	+2	+3	- Block
000E94 <sub>H</sub>	— EPFR56 [R/W] B,H,W	— EPFR57 [R/W] B,H,W	— EPFR58 [R/W] B,H,W	— EPFR59 [R/W] B,H,W	-
	0-0 EPFR60 [R/W]	00-0 EPFR61 [R/W]	00-0 EPFR62 [R/W]	00-0 EPFR63 [R/W]	Extended Port Function Register
000E9C <sub>H</sub>	B,H,W 00-0	B,H,W 00-	B,H,W 00-	B,H,W 0000-	
000EA0 <sub>H</sub> to 000EBC <sub>H</sub>			Reserved		
000EC0 <sub>н</sub>	PPER00 [R/W] B,H,W 00000000	PPER01 [R/W] B,H,W 00000000	PPER02 [R/W] B,H,W 00000000	PPER03 [R/W] B,H,W 00000000	
000EC4 <sub>н</sub>	PPER04 [R/W] B,H,W 00000000	PPER05 [R/W] B,H,W 00000000	PPER06 [R/W] B,H,W 00000000	PPER07 [R/W] B,H,W 00000000	
000EС8 <sub>Н</sub>	B <sub>H</sub> B,H,W B,H,W 00000000 00000000	00000000	PPER10 [R/W] B,H,W 00000000	PPER11 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
000ECC <sub>H</sub>	PPER12 [R/W] B,H,W 00000000	PPER13 [R/W] B,H,W -0000000	PPER14 [R/W] B,H,W 000	PPER15 [R/W] B,H,W 000000	Litable Register
000ED0 <sub>H</sub>	_	_	_	_	
000ED4 <sub>н</sub>	_	_	_	_	
000ED8 <sub>н</sub>	PPER16 [R/W] B,H,W 00000000	PPER17 [R/W] B,H,W 00000000	PPER18 [R/W] B,H,W 00000000	PPER19 [R/W] B,H,W 00000000	
000EDC <sub>H</sub> to 000F3C <sub>H</sub>	_	_	_	_	Reserved
000F40 <sub>Н</sub>	PORTEN [R/W] B,H,W 0	-	_	_	Port Enable Register
000F44 <sub>н</sub>	KEYCDR 00000000		ı	_	KeyCodeRegister
000F48 <sub>H</sub> to 000F64 <sub>H</sub>	_	_	_	_	Reserved
000F68 <sub>H</sub>	XX	MSCY6	[R] H,W XXXXXXXX XXXXXX	xx	Input Capture 6,7 Cycle
000F6C <sub>н</sub>	XX	xx	measurement data register 67		



A al al as a s		Disale			
Address	+0	+1	+2	+3	Block
000F70 <sub>Н</sub>	RCRH0 [W] H,W XXXXXXX	RCRL0 [W] B,H,W XXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/Down
000F74 <sub>H</sub>	CCR0 [R/W] B,H 000000000 -0001000		_	CSR0 [R/W] B 00000000	Counter 0
000F78 <sub>H</sub> to 000F7C <sub>H</sub>	<del>-</del>	_	_	_	Reserved
000F80н	RCRH1 [W] H,W XXXXXXXX	RCRL1 [W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/Down
000F84 <sub>н</sub>		R/W] B,H ) -0001000	_	CSR1 [R/W] B 00000000	Counter 1
000F88 <sub>н</sub>	_			Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45	
000F8С <sub>н</sub>	_	MSCH67 [R — B,H,W 00000000		MSCL67 [R/W] B,H,W 00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67
000F90 <sub>н</sub>		OCCP10 00000000 00000000			Output Compare
000F94 <sub>н</sub>		OCCP11 00000000 00000000			32-bit OCU
000F98 <sub>н</sub>	_	_	OCSH1011 [R/W] B,H,W 000	OCSL1011 [R/W] B,H,W 000000	Output Compare 10,11 32-bit OCU
000F9Сн	_	_	_	OCLS1011 [R/W] B,H,W 0000	OCU1011 Output level control register
000FA0 <sub>н</sub>		CPCLR5 111111111 11111111			
000FA4 <sub>Н</sub>		TCDT5 [ 00000000 00000000			Free-run Timer 5 32-bit FRT
000FA8н	TCCSH5 [R/W]B,H,W 000	TCCSL5 [R/W]B,H,W -1-00000	_	_	
000FAC <sub>H</sub> to 000FCC <sub>H</sub>	_	_	_	_	Reserved



A -1 -1		Address offset val	ue / Register name		Disals			
Address	+0	Block						
000FD0 <sub>н</sub>	XX	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX						
000FD4 <sub>н</sub>	XX	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX						
000FD8 <sub>H</sub>	_	_	LSYNS1 [R/W] B,H,W 00000000	ICS45 [R/W] B,H,W 00000000	32-bit ICU			
000FDC <sub>н</sub>	XX	IPCP6 XXXXXX XXXXXXX	S [R] W XXXXXXXX XXXXX	ΧΧ				
000FE0 <sub>H</sub>	XX	IPCP7 XXXXXX XXXXXXX	' [R] W XXXXXXXX XXXXX	XXX	Input Capture 6,7			
000FE4 <sub>н</sub>	l	_	_	ICS67 [R/W] B,H,W 00000000	32-bit ICU			
000FE8 <sub>H</sub>	XX	IPCP8	R] W XXXXXXXX XXXXX	XXX				
000FEC <sub>H</sub>	XX	IPCP9	R] W XXXXXXXX XXXXX	XXX	Input Capture 8,9 32-bit ICU			
000FF0 <sub>н</sub>	_	ICS89 [R/W] B,H,W 00000000						
000FF4 <sub>н</sub>	XX	Input Capture 8,9						
000FF8 <sub>н</sub>	xx	MSCY9 XXXXXX XXXXXXX	[R] H,W XXXXXXXX XXXXXX	XXX	32-bit ICU Cycle measurement data register 89			
000FFC <sub>н</sub>	_	_	MSCH89 [R] B,H,W 00000000	MSCL89 [R/W] B,H,W 00	Cycle and pulse width measurement control 89			
001000н	SACR [R/W] B,H,W	PICD [R/W] B,H,W0011	_	_	Clock Control			
001004 <sub>H</sub> to 00112С <sub>H</sub>	_	_	_	_	Reserved			
001130 <sub>н</sub>	_	_	_	CRCCR [R/W] B,H,W -0000000				
001134 <sub>н</sub>		CRCINIT [F 11111111 11111111			CRC calculation			
001138 <sub>н</sub>		-	/W] B,H,W 00000000 00000000		unit			
00113С <sub>н</sub>			R] B,H,W 11111111 11111111					
001140 <sub>H</sub> to 0011FC <sub>H</sub>	_	_	_	_	Reserved			



<b>A</b> 1.1		Dii			
Address	+0	+1	+2	+3	Block
001750н	SCR0/(IBCR0)[R/W] B,H,W 000000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W ] B,H,W 00000000	
001754н	— /(RDR10/(TDR	- /(RDR10/(TDR10))[R/W] B,H,W		Multi-UART0	
001758н	SACSR0[R 0000 (	=	-	R] B,H,W 00000000	*1: Byte access is possible only for
00175Сн	STMCR0[R 00000000		— /(SCSCR0/SF	UR0)[R/W] B,H,W	access to lower 8 bits.
001760н	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W	— /(SCSTR10) /(SFLR10) [R/W] B,H,W	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W	*2: Reserved because I <sup>2</sup> C mode is not set immediately after
001764 <sub>н</sub>	_	— /(SCSFR20) [R/W] B,H,W *3	— /(SCSFR10) [R/W] B,H,W *3	— /(SCSFR00) [R/W] B,H,W	reset.  *3: Reserved because CSIO
001768 <sub>Н</sub>	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W	TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000	mode is not set immediately after reset.  *4: Reserved
00176Сн	BGR0[R/ 00000000	-	— /(ISMK0) [R/W] B,H,W	— /(ISBA0) [R/W] B,H,W	because LIN2.1 mode is not set immediately after
001770н	FCR10[R/W] B,H,W 00100	FCR00[R/W] B,H,W -0000000		R/W] B,H,W 00000000	reset.
001774н	FTICR0[R/ 00000000	- · · · · · · · · · · · · · · · · · · ·	-	_	
001778н	SCR1/(IBCR1) [R/W] B,H,W 000000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W ] B,H,W 00000000	Multi-UART1
00177Сн	— /(RDR11/(TDR 	11))[R/W] B,H,W *3		1)[R/W] B,H,W 0000000 <sup>*1</sup>	
001780н	SACSR1[R 0000 (		-	R] B,H,W 00000000	Multi-UART1
001784н	STMCR1[R 00000000	=	— /(SCSCR1/SF	UR1)[R/W] B,H,W *3 *4	*1: Byte access is possible only for access to lower 8
001788 <sub>н</sub>	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W *3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W	bits. *2: Reserved
00178С <sub>н</sub>	_	— /(SCSFR21)[R/W] B,H,W *3	— /(SCSFR11) [R/W] B,H,W	— /(SCSFR01) [R/W] B,H,W	because I <sup>2</sup> C mode is not set immediately after reset.



Address	+0	+1	+2 +3		Block	
001AD0 <sub>H</sub>	PCN6 [R/W 00000000 0	•		PCSR6 [W] H,W XXXXXXX XXXXXXX		
001AD4 <sub>Н</sub>	PDUT6 [M XXXXXXXX X	-	PTMR6 [R] H,W 11111111 11111111		DDCC	
001AD8 <sub>н</sub>	=	PCN206 [R/W] B,H,W PSDR6 [R/W] H,W000000110 00000000 00000000		PPG6		
001ADC <sub>н</sub>	PTPC6 [R/\ 00000000 00	-	ı	_		
001AE0 <sub>н</sub>	PCN7 [R/W 00000000 0	_		7 [W] H,W X XXXXXXX		
001AE4 <sub>н</sub>	PDUT7 [M XXXXXXXX X			7 [R] H,W 1 11111111	PPG7	
001AE8 <sub>н</sub>	PCN207 [R/V 000000 -	- · · · · ·	PSDR7 [R/W] H,W 00000000 00000000			
001AEC <sub>н</sub>	PTPC7 [R/\ 00000000 00	-	1	_		
001AF0 <sub>н</sub>	PCN8 [R/W 00000000 0	•	PCSR8 XXXXXXX			
001AF4 <sub>н</sub>	PDUT8 [W] H,W XXXXXXXX XXXXXXX		PTMR8 [R] H,W 11111111 11111111		PPG8	
001AF8 <sub>н</sub>	-	PCN208 [R/W] B,H,W PSDR8 [R/W] H,W000000110 00000000 00000000		PPGo		
001AFC <sub>н</sub>	PTPC8 [R/\ 00000000 00	-	_	_		
001В00н	PCN9 [R/W 00000000 0			P [W] H,W X XXXXXXX		
001B04 <sub>Н</sub>	NJ etudq XXXXXXXX	<u> </u>	PTMR9 [R] H,W 11111111 11111111		PPG9	
001B08 <sub>Н</sub>	PCN209 [R/V 000000 -	110		[R/W] H,W 0 00000000		
001B0С <sub>н</sub>	PTPC9 [R/\ 00000000 00	000000	_	_		
001B10 <sub>H</sub>	PCN10 [R/W 00000000 0	•		0 [W] H,W X XXXXXXX	DDC10	
001В14 <sub>Н</sub>	PDUT10 [V XXXXXXXX X	- ·	PTMR10 [R] H,W 11111111 11111111		PPG10	
001В18 <sub>Н</sub>	PCN210 [R/V 000000 -	-		[R/W] H,W 0 00000000	DDC40	
001B1C <sub>н</sub>	PTPC10 [R/ 00000000 00		_	_	PPG10	
001В20 <sub>Н</sub>	PCN11 [R/W 00000000 0	-		1 [W] H,W X XXXXXXX	PPG11	



	Interr	upt number	Interrupt		Default	
Interrupt factor	Decimal	Hexadecimal	level	Offset	address for TBR	RN
32-bit ICU5 (fetching/measurement)						
A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/ 47	57	39	ICR41	318 <sub>H</sub>	000FFF18 <sub>н</sub>	41
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314 <sub>H</sub>	000FFF14 <sub>н</sub>	42
32-bit OCU 8/9 (match)	59	3B	ICR43	310 <sub>H</sub>	000FFF10 <sub>н</sub>	43
-	60	3C	ICR44	30C <sub>H</sub>	000FFF0С <sub>н</sub>	44
Base timer 1 IRQ0						
Base timer 1 IRQ1	61	3D	ICR45	308 <sub>H</sub>	000FFF08 <sub>H</sub>	45
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 <sub>H</sub>	000FFF04 <sub>H</sub>	-
Delay interrupt	63	3F	ICR47	300н	000FFF00 <sub>н</sub>	-
System reserved (Used for REALOS)	64	40	-	2FC <sub>H</sub>	000FFEFC <sub>H</sub>	-
System reserved (Used for REALOS)	65	41	-	2F8 <sub>H</sub>	000FFEF8 <sub>н</sub>	-
Used with the INT instruction	66   255	42   FF	-		000FFEF4 <sub>H</sub>   000FFC00 <sub>H</sub>	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

<sup>\*1:</sup> It does not support a DMA transfer by the status of the multi-function serial interface and I<sup>2</sup>C reception.

<sup>\*2:</sup> Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

<sup>\*3:</sup> PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

<sup>\*4:</sup> The clock calibration unit does not support a DMA transfer by the interrupt.

<sup>\*5: 32-</sup>bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

<sup>\*6:</sup> There is no resource corresponding to the interrupt level.

<sup>\*7:</sup> It does not support a DMA transfer by the external low-voltage detection interrupt.



		upt number	Interrupt		Default		
Interrupt factor	Decimal	Hexadecimal	level	Offset	address for TBR	r RN	
32-bit ICU5 (fetching/measurement)							
A/D converter	57	39	ICR41	318 <sub>H</sub>	000FFF18 <sub>н</sub>	41	
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47							
32-bit OCU 6/7/10/11 (match)	58	3A	ICR42	314 <sub>H</sub>	000FFF14 <sub>н</sub>	42	
32-bit OCU 8/9 (match)	59	3B	ICR43	310 <sub>H</sub>	000FFF10 <sub>н</sub>	43	
-	60	3C	ICR44	30Сн	000FFF0С <sub>н</sub>	44	
Base timer 1 IRQ0							
Base timer 1 IRQ1	61	3D	ICR45	308 <sub>H</sub>	000FFF08 <sub>H</sub>	45	
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 <sub>H</sub>	000FFF04 <sub>H</sub>	-	
Delay interrupt	63	3F	ICR47	300 <sub>H</sub>	000FFF00 <sub>н</sub>	-	
System reserved (Used for REALOS)	64	40	-	2FC <sub>H</sub>	000FFEFC <sub>н</sub>	-	
System reserved (Used for REALOS)	65	41	-	2F8 <sub>H</sub>	000FFEF8 <sub>H</sub>	-	
	66	42		2F4 <sub>H</sub>	000FFEF4 <sub>H</sub>		
Used with the INT instruction		I	-	I		-	
	255	FF		000 <sub>H</sub>	000FFC00 <sub>H</sub>		

**Note:** It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

<sup>\*1:</sup> It does not support a DMA transfer by the status of the multi-function serial interface and I<sup>2</sup>C reception.

<sup>\*2:</sup> Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

<sup>\*3:</sup> PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

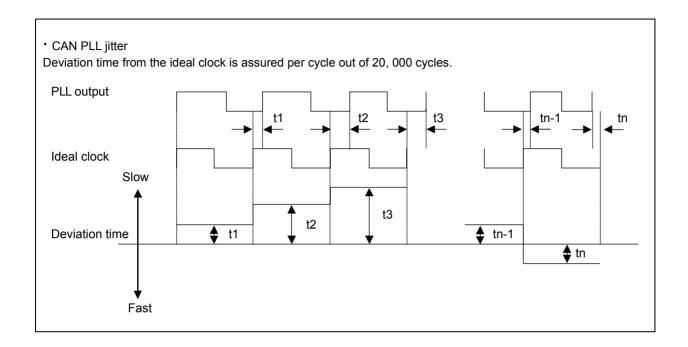
<sup>\*4:</sup> The clock calibration unit does not support a DMA transfer by the interrupt.

<sup>\*5: 32-</sup>bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

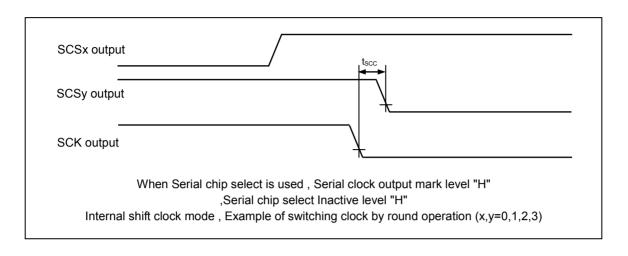
<sup>\*6:</sup> There is no resource corresponding to the interrupt level.

<sup>\*7:</sup> It does not support a DMA transfer by the external low-voltage detection interrupt.











Part number	Sub clock	CSV Initial value	LVD Initial value	Package* <sup>2</sup>
MB91F526KWBPMC1	Yes	ON	ON	
MB91F526KYBPMC1			OFF	
MB91F526KJBPMC1		OFF	ON	
MB91F526KLBPMC1			OFF	
MB91F525KWBPMC1		ON	ON	
MB91F525KYBPMC1			OFF	
MB91F525KJBPMC1		OFF	ON	
MB91F525KLBPMC1			OFF	
MB91F524KWBPMC1		ON	ON	
MB91F524KYBPMC1			OFF	
MB91F524KJBPMC1		OFF	ON	
MB91F524KLBPMC1			OFF	
MB91F523KWBPMC1		ON	ON	
MB91F523KYBPMC1			OFF	
MB91F523KJBPMC1		OFF	ON	
MB91F523KLBPMC1			OFF	
MB91F522KWBPMC1		ON	ON	
MB91F522KYBPMC1			OFF	
MB91F522KJBPMC1		OFF	ON	
MB91F522KLBPMC1			OFF	LQN • 144 pin,
MB91F526KSBPMC1	None	ON	ON	(Lead pitch 0.4mm) Plastic
MB91F526KUBPMC1			OFF	
MB91F526KHBPMC1		OFF	ON	
MB91F526KKBPMC1			OFF	
MB91F525KSBPMC1		ON	ON	
MB91F525KUBPMC1			OFF	
MB91F525KHBPMC1		OFF	ON	
MB91F525KKBPMC1			OFF	
MB91F524KSBPMC1		ON	ON	
MB91F524KUBPMC1			OFF	
MB91F524KHBPMC1		OFF	ON	
MB91F524KKBPMC1			OFF	
MB91F523KSBPMC1		ON	ON	
MB91F523KUBPMC1			OFF	
MB91F523KHBPMC1		OFF	ON	
MB91F523KKBPMC1			OFF	
MB91F522KSBPMC1		ON	ON	
MB91F522KUBPMC1			OFF	
MB91F522KHBPMC1		OFF	ON	
MB91F522KKBPMC1			OFF	



Page	Section	Change Results						
		A List of "Pin Description" modified.						
		(Error)						
		Pin no.				Pin		
		64	80	100	120	144	176	Name
					_	40	40	
		-	-	4	7	10	12	
								Name P025 WR1X SOT4_1 PPG25_0 TIN2_0 P172 PPG38_1 P026 A00 SCK4_1 PPG26_0 TIN3_0 P027 A01 SCS40_1 PPG27_0 TOT0_0 RTO3_1 P173 PPG39_1 P030 A02 SCS41_1 PPG28_0 TOT1_0 P031 A03 SCS42_1 PPG29_0 TOT2_0 P032 A04 SCS43_1 PPG30_0 TOT3_0 RTO3_1 PPG30_0 TOT3_0 RTO3_1
		-	-	-	-	-	13	
			4	5	8	11	14	
		-						
								SOT4_1 PPG25_0 TIN2_0 P172 PPG38_1 P026 A00 SCK4_1 PPG26_0 TIN3_0 P027 A01 SCS40_1 PPG27_0 TOT0_0 RT03_1 P173 PPG39_1 P030 A02 SCS41_1 PPG28_0 TOT1_0 P031 A03 SCS42_1 PPG29_0 TOT2_0 P032
		4	-		0	40	4.5	Name P025 WR1X SOT4_1 PPG25_0 TIN2_0 P172 PPG38_1 P026 A00 SCK4_1 PPG26_0 TIN3_0 P027 A01 SCS40_1 PPG27_0 TOT0_0 RTO3_1 P173 PPG39_1 P030 A02 SCS41_1 PPG28_0 TOT1_0 P031 A03 SCS42_1 PPG29_0 TOT2_0 P032 A04 SCS43_1 PPG30_0 TOT3_0 RTO2_1 P033 A04 SCS43_1 PPG30_0 TOT3_0 RTO2_1 P033 A05
		4	5	6	9	12	2 15	
								Name P025 WR1X SOT4_1 PPG25_0 TIN2_0 P172 PPG38_1 P026 A00 SCK4_1 PPG26_0 TIN3_0 P027 A01 SCS40_1 PPG27_0 TOT0_0 RTO3_1 P173 PPG39_1 P030 A02 SCS41_1 PPG28_0 TOT1_0 P031 A03 SCS42_1 PPG29_0 TOT2_0 P032 A04 SCS43_1 PPG30_0 TOT3_0 RTO2_1 P033 A04 SCS43_1 PPG30_0 TOT3_0 RTO2_1 P033 A05 PPG31_0 ICU3_3 TIN4_0 RTO1_1
20	■PIN Description	-	-	-	-	-	16	
			_	- 7	7 10	13	17	
		-						
			6	8	11	14	18	
							15 19	
		5	7	9	12	15		
								Name P025 WR1X SOT4_1 PPG25_0 TIN2_0 P172 PPG38_1 P026 A00 SCK4_1 PPG26_0 TIN3_0 P027 A01 SCS40_1 PPG27_0 TOT0_0 RT03_1 P173 PPG39_1 P030 A02 SCS41_1 PPG28_0 TOT1_0 P031 A03 SCS42_1 PPG29_0 TOT2_0 P032 A04 SCS43_1 PPG30_0 TOT2_0 P032 A04 SCS43_1 PPG30_0 TOT3_0 RT03_1 PPG30_0 TOT3_0 RT03_1 PO30 RT04 SCS43_1 PPG30_0 TOT3_0 RT05_1 RT06_1 RT07_1 R
			8	10	13	16	20	
		6						
								SCK3_2



Pin Name P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1 P177
Name P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1 P177
Name P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1 P177
Name P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1 P177
P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1 P177
AN45 TRG8_0 TIN3_2 SOT0_1 P177
TRG8_0 TIN3_2 SOT0_1 P177
TIN3_2 SOT0_1 P177
SOT0_1 P177
P177
Name P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1 P177 TRG11_0 P050 A18 TRG5_1 PPG33_0 P051 A19 TRG9_0 P052 A20 PPG34_0 INT14_0 P053 A21 AN44 PPG35_0 INT14_1 SCK0_1 P054 SYSCLK PPG36_0 P055 CS2X SIN10_0 AN43 PPG37_0 TIN4_1 P056 CS3X ICU9_0
TRG11 0
A18
Name P047 A17 AN45 TRG8_0 TIN3_2 SOT0_1 P177 TRG11_0 P050 A18 TRG5_1 PPG33_0 P051 A19 TRG9_0 P052 A20 PPG34_0 INT14_0 P053 A21 AN44 PPG35_0 INT14_1 SCK0_1 P054 SYSCLK PPG36_0 P055 CS2X SIN10_0 AN43 PPG37_0 TIN4_1 P056 CS3X
TIN4_1
DOEC
PPG0_1
ICU0_1
TIN5 1



Page	Section	Change Results
Rev *C	I	
2	Features Peripheral Functions	The following sentence modified in I2C as following:  (Error)  < I2C >  2 channels ch.3 , ch.4 Standard mode/high-speed mode supported.  Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported  (Correct)  < I2C >  2 channels ch.3 , ch.4 Standard mode/fast mode supported.  Standard mode (Max. 100kbps) / fast mode (Max. 400kbps)
5,6,7,8,9 ,10	1. Product Lineup	The following *2 added as follows:  (Error)  Power supply  (Correct)  Power supply  2.7 V to 5.5 V  (2.7 V to 5.5 V)
5,6,7,8,9 ,10	1. Product Lineup	The following sentence added as follows:  (Correct)  *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V).  This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V).  Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector.  Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
8, 9, 10,	1. Product Lineup	The following sentence modified in the bottom of Product lineup comparison table as following:  (Error)  *1: Only channel 3 and channel 4 support the I2C (high-speed mode/standard mode).  (Correct)
11	1 Product Linguin	*1: Only channel 3 and channel 4 support the I2C (fast mode/standard mode).
11	Product Lineup	Added silicon version E



Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Package  ↓ Package*²  Added the following description.  *¹: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.  Corrected the following description.  For details of the package, see "■ PACKAGE DIMENSIONS ".  ↓  *²: For details of the package, see "■ PACKAGE DIMENSIONS ".  Added the following description.  • ORDERING INFORMATION MB91F52xxxC  Company name and layout design change
*A	4999456	JHMU	11/13/2015	Updated to Cypress template.  Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in "Absolute Maximum Ratings" of "ELECTRICAL CHARACTERISTICS".  *9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.  *10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.  Added Errata section.
*B	5112138	KUME	01/28/2016	Fixed some clerical errors.  For details, please see the chapter 18. Major Changes.
*C	5196285	KUME	04/28/2016	For details, please see the chapter 19. Major Changes.
*D	5318862	KUME	06/23/2016	For details, please see the chapter 19. Major Changes.



## Sales, Solutions, and Legal Information

## **Worldwide Sales and Design Support**

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

**Products** 

ARM® Cortex® Microcontrollers cypress.com/arm

Automotive cypress.com/automotive

Clocks & Buffers cypress.com/clocks

Interface cypress.com/interface

Lighting & Power Control cypress.com/powerpsoc

Memory cypress.com/memory

PSoC cypress.com/psoc

Touch Sensing cypress.com/touch

USB Controllers cypress.com/usb

Wireless/RF cypress.com/wireless

**PSoC® Solutions** 

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

**Cypress Developer Community** 

Community | Forums | Blogs | Video | Training | Components

Technical Support cypress.com/support

ARM and Cortex are the registered trademarks of ARM Limited in the EU and other countries

© Cypress Semiconductor Corporation, 2014-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Document Number: 002-04662 Rev. \*D June 23, 2016 Page 289 of 289