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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526fscpmc-gs-ere2

Product lineup comparison 176 pins

	MB91F522L	MB91F523L	MB91F524L	MB91F525L	MB91F526L
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB	(64+8)KB	(96+8)KB	(128+8)KB	
External BUS I/F (22address/16data/4cs)	Yes				
DMA Transfer	16ch				
16-bit Base Timer	2ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×48ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×32ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch ^{*1}				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	152 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T _A)	-40°C to +125°C				
Power supply	2.7V to 5.5V ^{*2}				
Package	LQP176				

*1: Only channel 3 and channel 4 support the I²C (fast mode/standard mode).

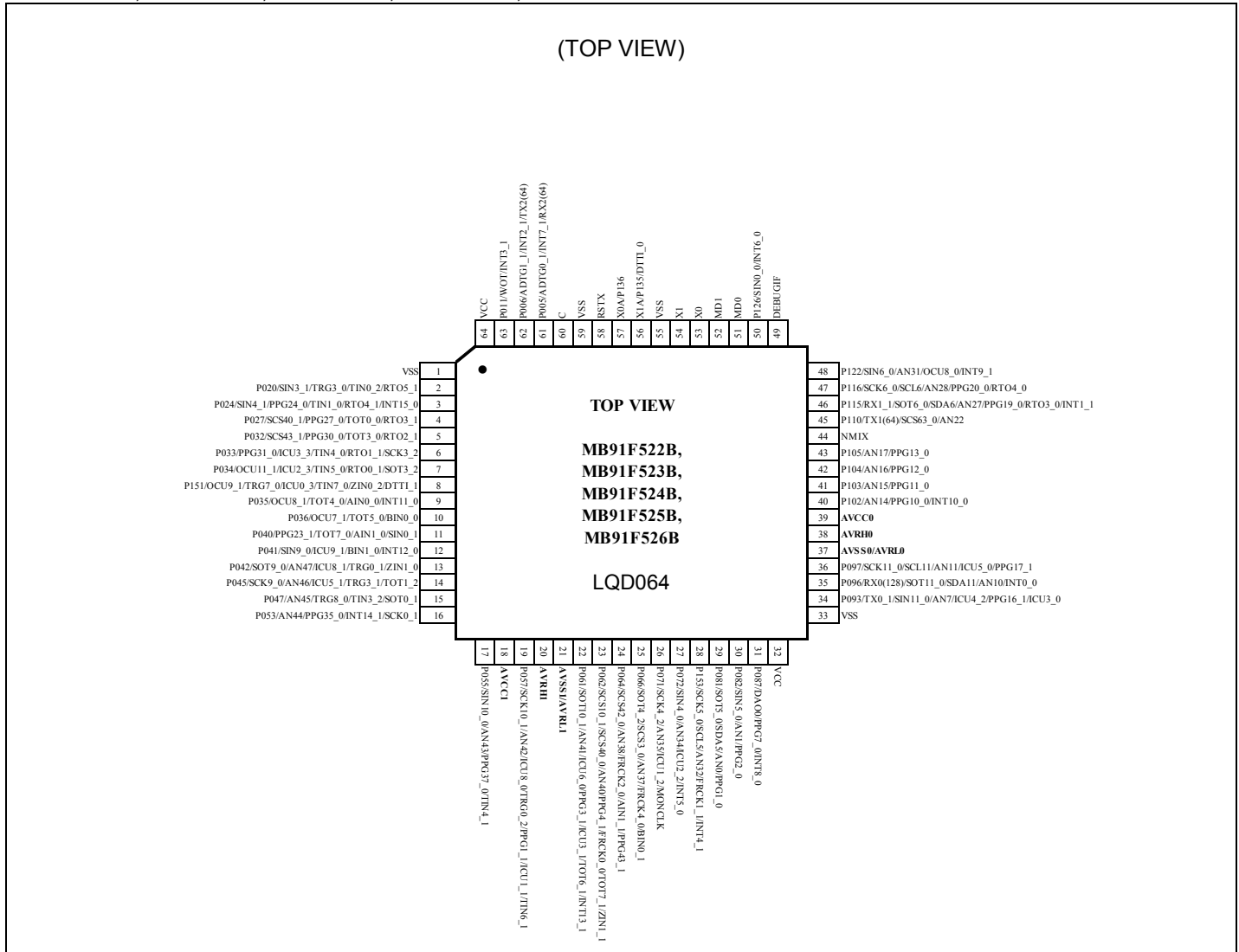
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

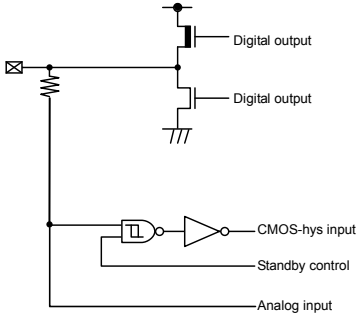
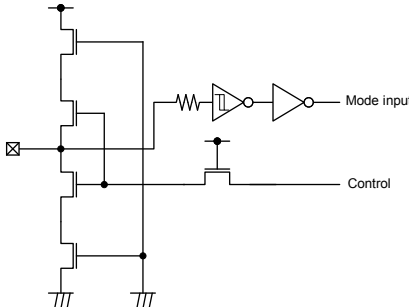
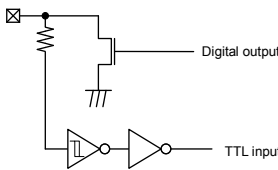
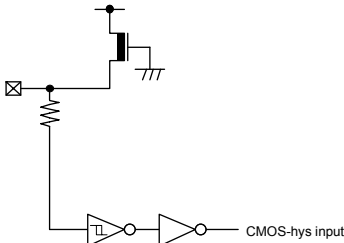
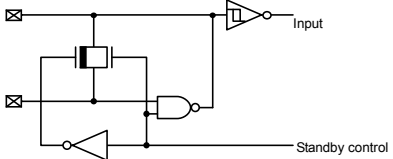
2. Pin Assignment

MB91F52xB

MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B



* In a single clock product, pin 56 and pin 57 are the general-purpose ports.

Type	Circuit	Remarks
J		<ul style="list-style-type: none"> • Analog input, General-purpose I/O port (5V tolerant) • Output 4mA • CMOS hysteresis input
K		<ul style="list-style-type: none"> • Mode I/O • CMOS hysteresis input
L		<ul style="list-style-type: none"> • Open-drain I/O • Output 25mA (Nch open-drain) • TTL input
M		<ul style="list-style-type: none"> • CMOS hysteresis input • Pull-up resistor 50kΩ
N		<ul style="list-style-type: none"> • Main oscillation I/O

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000CF0 _H	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
000CF4 _H	DCSR15 [R/W] H 0-----000		DTCR15 [R/W] H 00000000 00000000		
000CF8 _H	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CFC _H	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000D00 _H to 000DF0 _H	—	—	—	—	Reserved [S]
000DF4 _H	—	—	DNMIR [R/W] B 0-----0	DILVR [R/W] B ---11111	DMA Controller [S]
000DF8 _H	DMACR[R/W] W 0-----0-----0-----0-----				
000DFC _H	—	—	—	—	Reserved [S]
000E00 _H	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
000E04 _H	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
000E08 _H	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register
000E0C _H	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -0000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000	
000E10 _H	—	—	—	—	
000E14 _H	—	—	—	—	
000E18 _H	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
000E1C _H	—	—	—	—	Reserved
000E20 _H	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
000E24 _H	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
000E28 _H	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
000E2C _H	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
000E30 _H	—	—	—	—	
000E34 _H	—	—	—	—	
000E38 _H	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000F70 _H	RCRH0 [W] H,W XXXXXXXX	RCRL0 [W] B,H,W XXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/Down Counter 0
000F74 _H	CCR0 [R/W] B,H 00000000 -0001000		—	CSR0 [R/W] B 00000000	
000F78 _H to 000F7C _H	—	—	—	—	Reserved
000F80 _H	RCRH1 [W] H,W XXXXXXXX	RCRL1 [W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/Down Counter 1
000F84 _H	CCR1 [R/W] B,H 00000000 -0001000		—	CSR1 [R/W] B 00000000	
000F88 _H	—	—	MSCH45 [R] B,H,W 00000000	MSCL45 [R/W] B,H,W -----00	Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45
000F8C _H	—	—	MSCH67 [R] B,H,W 00000000	MSCL67 [R/W] B,H,W -----00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67
000F90 _H	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU
000F94 _H	OCCP11 [R/W] W 00000000 00000000 00000000 00000000				
000F98 _H	—	—	OCSH1011 [R/W] B,H,W ---0--00	OCSL1011 [R/W] B,H,W 0000--00	Output Compare 10,11 32-bit OCU
000F9C _H	—	—	—	OCLS1011 [R/W] B,H,W ----0000	OCU1011 Output level control register
000FA0 _H	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 5 32-bit FRT
000FA4 _H	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FA8 _H	TCCSH5 [R/W]B,H,W 0-----00	TCCSL5 [R/W]B,H,W -1-00000	—	—	
000FAC _H to 000FCC _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001344 _H	ADCOMP28/ADCOMPB28[R/W] H,W 00000000 00000000		ADCOMP29/ADCOMPB29[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001348 _H	ADCOMP30/ADCOMPB30[R/W] H,W 00000000 00000000		ADCOMP31/ADCOMPB31[R/W] H,W 00000000 00000000		
00134C _H	ADTCS0[R/W] B,H,W 00000000 0010----		ADTCS1[R/W] B,H,W 00000000 0010----		
001350 _H	ADTCS2[R/W] B,H,W 00000000 0010----		ADTCS3[R/W] B,H,W 00000000 0010----		
001354 _H	ADTCS4[R/W] B,H,W 00000000 0010----		ADTCS5[R/W] B,H,W 00000000 0010----		
001358 _H	ADTCS6[R/W] B,H,W 00000000 0010----		ADTCS7[R/W] B,H,W 00000000 0010----		
00135C _H	ADTCS8[R/W] B,H,W 00000000 0010----		ADTCS9[R/W] B,H,W 00000000 0010----		
001360 _H	ADTCS10[R/W] B,H,W 00000000 0010----		ADTCS11[R/W] B,H,W 00000000 0010----		
001364 _H	ADTCS12[R/W] B,H,W 00000000 0010----		ADTCS13[R/W] B,H,W 00000000 0010----		
001368 _H	ADTCS14[R/W] B,H,W 00000000 0010----		ADTCS15[R/W] B,H,W 00000000 0010----		
00136C _H	ADTCS16[R/W] B,H,W 00000000 0010----		ADTCS17[R/W] B,H,W 00000000 0010----		
001370 _H	ADTCS18[R/W] B,H,W 00000000 0010----		ADTCS19[R/W] B,H,W 00000000 0010----		
001374 _H	ADTCS20[R/W] B,H,W 00000000 0010----		ADTCS21[R/W] B,H,W 00000000 0010----		
001378 _H	ADTCS22[R/W] B,H,W 00000000 0010----		ADTCS23[R/W] B,H,W 00000000 0010----		
00137C _H	ADTCS24[R/W] B,H,W 00000000 0010----		ADTCS25[R/W] B,H,W 00000000 0010----		
001380 _H	ADTCS26[R/W] B,H,W 00000000 0010----		ADTCS27[R/W] B,H,W 00000000 0010----		
001384 _H	ADTCS28[R/W] B,H,W 00000000 0010----		ADTCS29[R/W] B,H,W 00000000 0010----		
001388 _H	ADTCS30[R/W] B,H,W 00000000 0010----		ADTCS31[R/W] B,H,W 00000000 0010----		
00138C _H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001390 _H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001790 _H	—/(TBYTE31)/ (LAMESR1) [R/W] B,H,W ----- *3	—/(TBYTE21)/ (LAMERT1) [R/W] B,H,W ----- *3	—/(TBYTE11)/ (LAMIER1) [R/W] B,H,W ----- *3	TBYTE01/(LAMRID1) / (LAMTID1) [R/W] B,H,W 00000000	Multi-UART1 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001794 _H	BGR1[R/W] H,W 00000000 00000000		—/(ISMK1)[R/W] B,H,W ----- *2	—/(ISBA1)[R/W] B,H,W ----- *2	
001798 _H	FCR11[R/W] B,H,W ---00100	FCR01[R/W] B,H,W -0000000	FBYTE1[R/W] B,H,W 00000000 00000000		
00179C _H	FTICR1[R/W] B,H,W 00000000 00000000		—	—	
0017A0 _H	SCR2/(IBCR2)[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000-00-0	SSR2[R/W] B,H,W 0-000011	ESCR2/(IBSR2)[R/W]] B,H,W 00000000	Multi-UART2 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017A4 _H	—/(RDR12/(TDR12))[R/W] B,H,W ----- *3		RDR02/(TDR02)[R/W] B,H,W -----0 00000000 *1		
0017A8 _H	SACSR2[R/W] B,H,W 0---000 00000000		STMR2[R] B,H,W 00000000 00000000		
0017AC _H	STMCR2[R/W] B,H,W 00000000 00000000		—/(SCSCR2/SFUR2)[R/W] B,H,W ----- *3 *4		
0017B0 _H	—/(SCSTR32)/ (LAMSR2) [R/W] B,H,W ----- *3	—/(SCSTR22)/ (LAMCR2) [R/W] B,H,W ----- *3	—/(SCSTR12)/ (SFLR12) [R/W] B,H,W ----- *3	—/(SCSTR02)/ (SFLR02) [R/W] B,H,W ----- *3	
0017B4 _H	—	—/(SCSFR22) [R/W] B,H,W ----- *3	—/(SCSFR12) [R/W] B,H,W ----- *3	—/(SCSFR02) [R/W] B,H,W ----- *3	
0017B8 _H	—/(TBYTE32)/ (LAMESR2) [R/W] B,H,W ----- *3	—/(TBYTE22)/ (LAMERT2) [R/W] B,H,W ----- *3	—/(TBYTE12)/ (LAMIER2) [R/W] B,H,W ----- *3	TBYTE02/(LAMRID2) / (LAMTID2) [R/W] B,H,W 00000000	
0017BC _H	BGR2[R/W] H, W 00000000 00000000		—/(ISMK2)[R/W] B,H,W ----- *2	—/(ISBA2)[R/W] B,H,W ----- *2	
0017C0 _H	FCR12[R/W] B,H,W ---00100	FCR02[R/W] B,H,W -0000000	FBYTE2[R/W] B,H,W 00000000 00000000		Multi-UART2
0017C4 _H	FTICR2[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0020BC _H	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0 _H to 0020FC _H	—				
002100 _H	CTRLR1 [R/W] B,H,W ----- 000-0001		STATR1 [R/W] B,H,W ----- 00000000		
002104 _H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108 _H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W ----- X00000--		
00210C _H	BRPER1 [R/W] B,H,W ----- ----0000		—	—	
002110 _H	IF1CREQ1 [R/W] B,H,W 0----- 00000001		IF1CMSK1 [R/W] B,H,W ----- 00000000		
002114 _H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118 _H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C _H	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120 _H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124 _H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128 _H	—	—	—	—	
00212C _H	—	—	—	—	
002130 _H , 002134 _H	Reserved (IF1 data mirror)				CAN1 (64msb)
002138 _H	—	—	—	—	
00213C _H	—	—	—	—	
002140 _H	IF2CREQ1 [R/W] B,H,W 0----- 00000001		IF2CMSK1 [R/W] B,H,W ----- 00000000		
002144 _H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148 _H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C _H	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Used with the INT instruction	66 255	42 FF	-	2F4 _H 000 _H	000FFE4 _H 000FFC00 _H	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

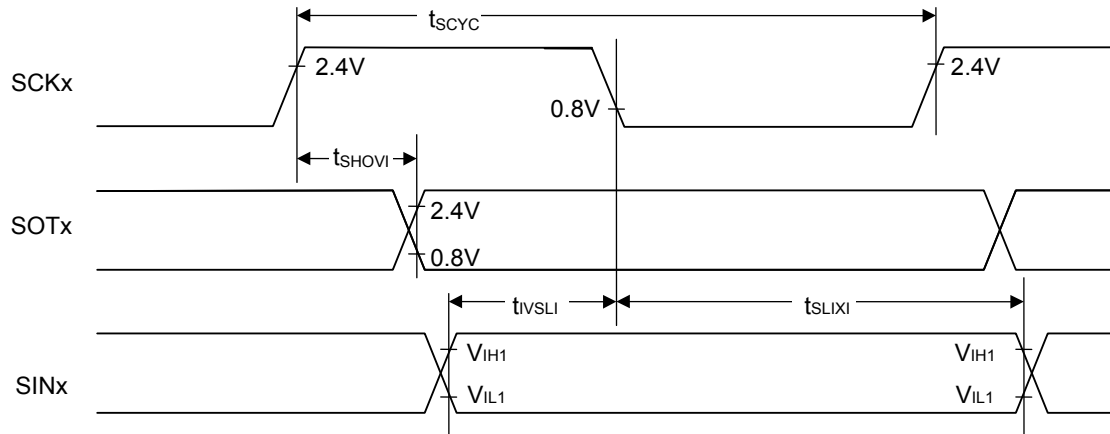
*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: REALOS is a trademark of Cypress.

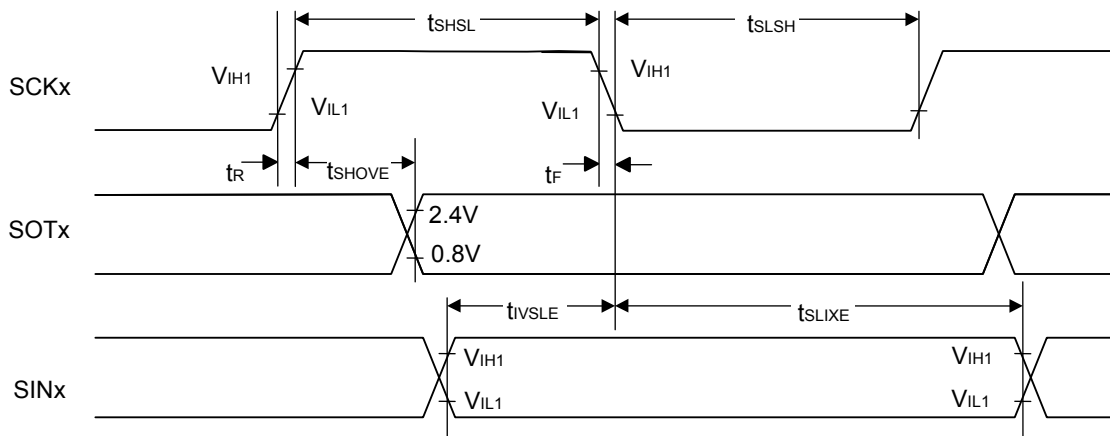
120 pins

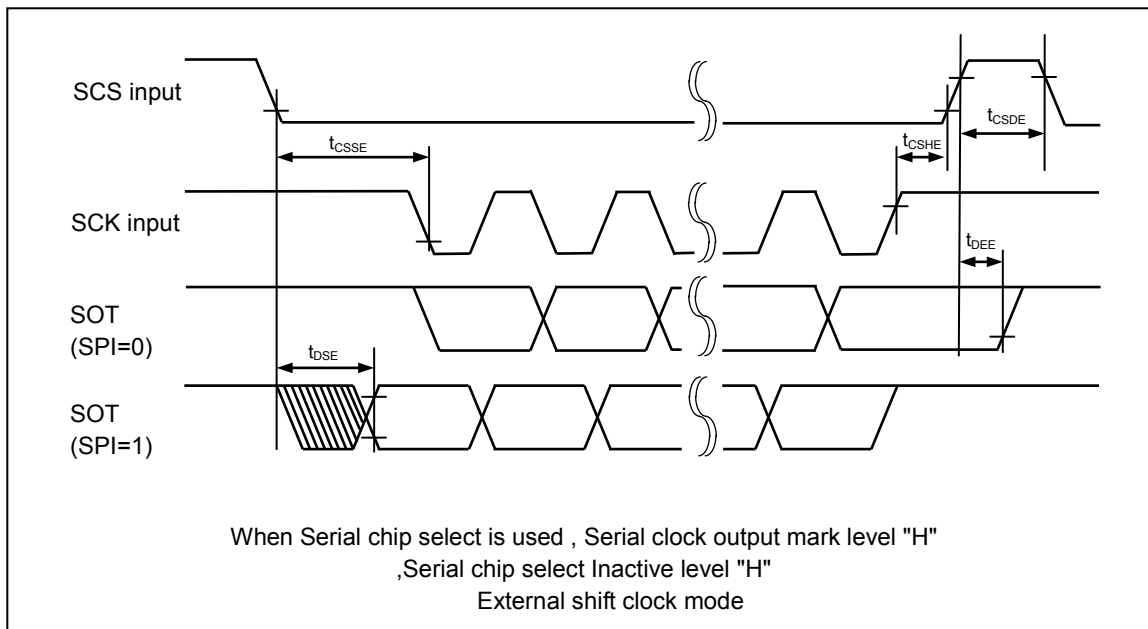
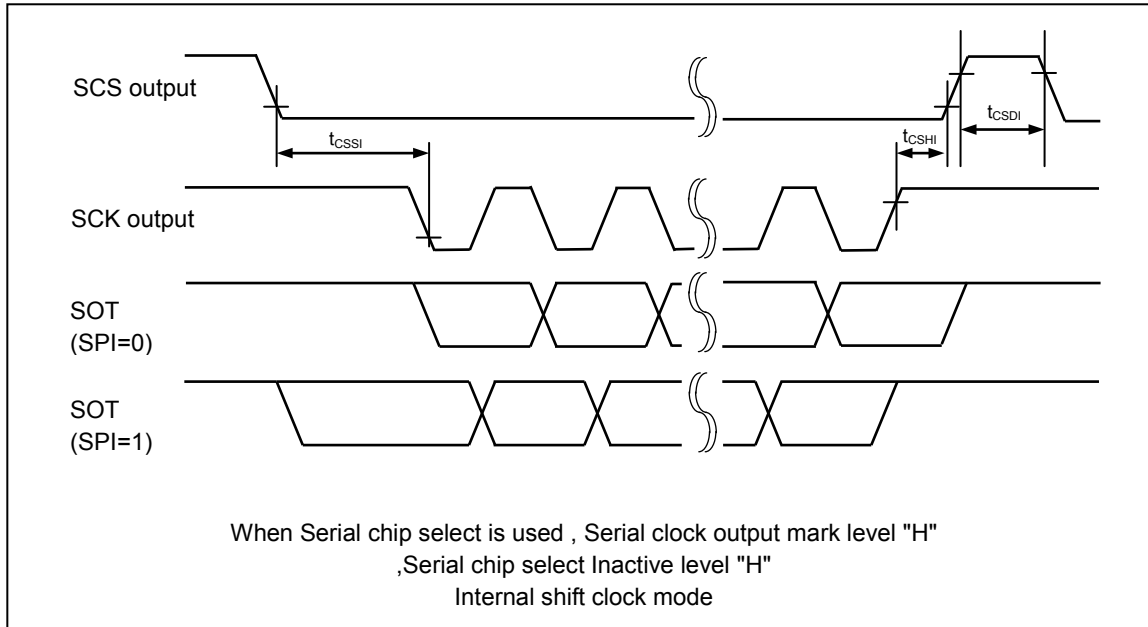
Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFE4 _H	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFD4 _H	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFC4 _H	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation during internal bus diagnosis						
XBS RAM double-bit error generation						
Backup RAM double-bit error generation						
TPU violation	16	10	ICR00	3BC _H	000FFFB4 _H	0
External interrupt 0-7						
External interrupt 8-15						
External low-voltage detection interrupt						
Reload timer 0/1/4/5	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁷
Reload timer 2/3/6/7	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFA4 _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						

☐ Internal shift clock mode



• External shift clock mode





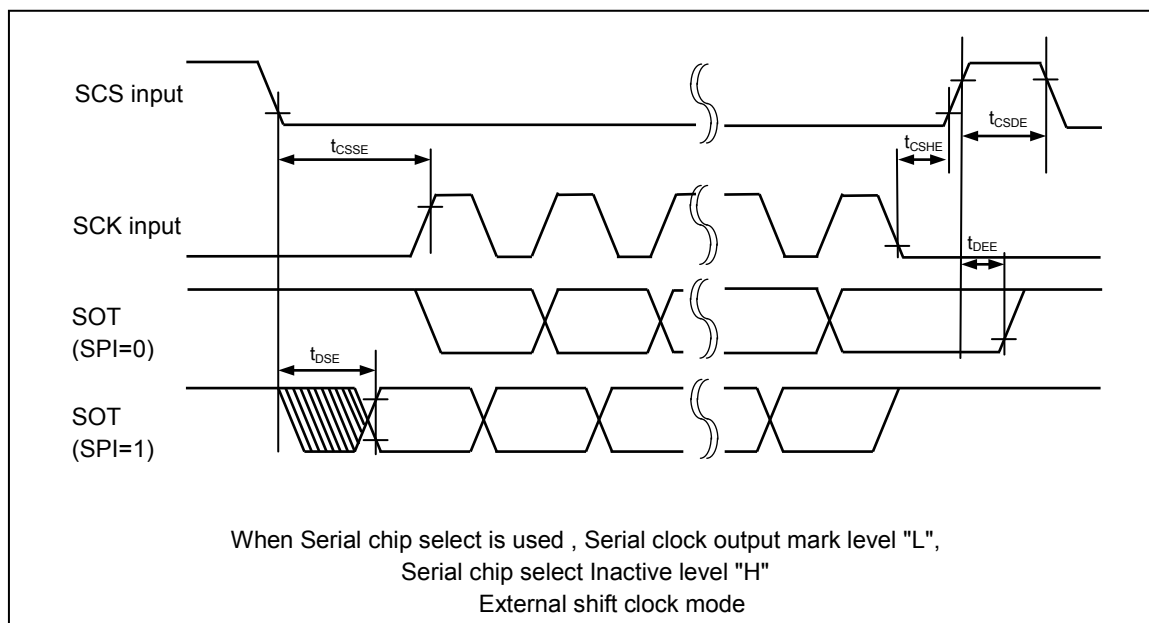
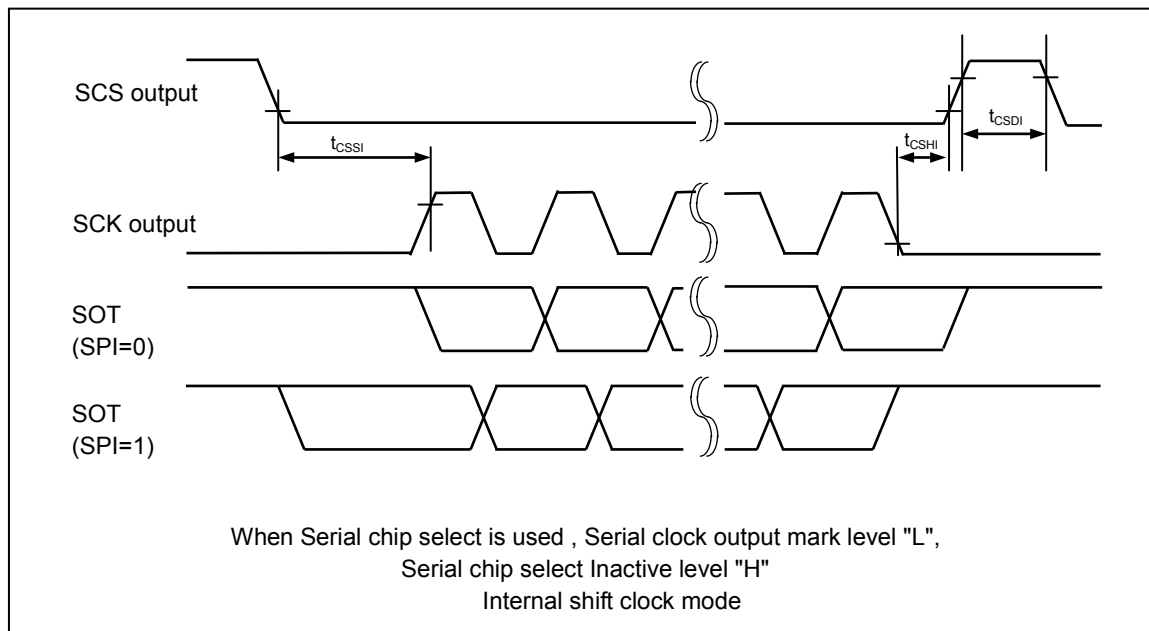
SCSx output

SCSy output

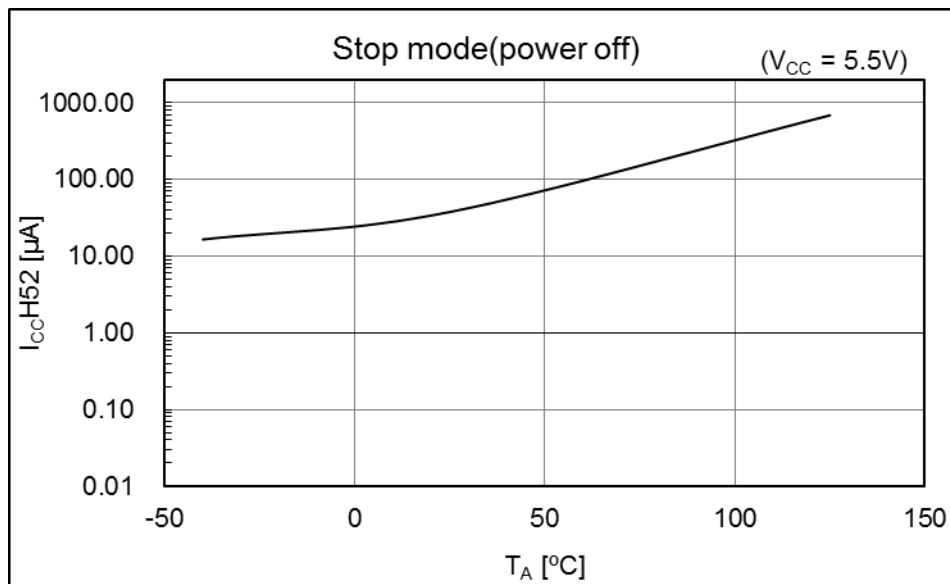
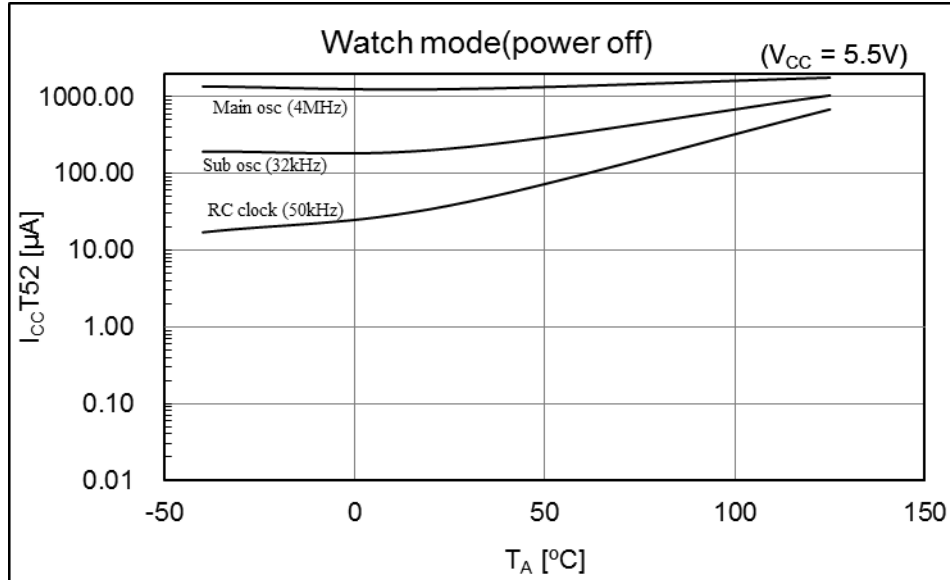
SCK output

t_{scc}

When Serial chip select is used , Serial clock output mark level "H"
 ,Serial chip select Inactive level "H"
 Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)



MB91F526



14. Ordering Information MB91F52xxxC*¹

Part number	Sub clock	CSV Initial value	LVD Initial value	Package ⁷²
MB91F526LWCPMC	Yes	ON	ON	LQP • 176 pin, Plastic
MB91F526LYCPMC			OFF	
MB91F526LJCPMC		OFF	ON	
MB91F526LLCPMC			OFF	
MB91F525LWCPMC		ON	ON	
MB91F525LYCPMC			OFF	
MB91F525LJCPMC		OFF	ON	
MB91F525LLCPMC			OFF	
MB91F524LWCPMC		ON	ON	
MB91F524LYCPMC			OFF	
MB91F524LJCPMC		OFF	ON	
MB91F524LLCPMC			OFF	
MB91F523LWCPMC		ON	ON	
MB91F523LYCPMC			OFF	
MB91F523LJCPMC		OFF	ON	
MB91F523LLCPMC			OFF	
MB91F522LWCPMC		ON	ON	
MB91F522LYCPMC			OFF	
MB91F522LJCPMC		OFF	ON	
MB91F522LLCPMC			OFF	
MB91F526LSCPMC	None	ON	ON	
MB91F526LUCPMC			OFF	
MB91F526LHCPMC		OFF	ON	
MB91F526LKCPMC			OFF	
MB91F525LSCPMC		ON	ON	
MB91F525LUCPMC			OFF	
MB91F525LHCPMC		OFF	ON	
MB91F525LKCPMC			OFF	
MB91F524LSCPMC		ON	ON	
MB91F524LUCPMC			OFF	
MB91F524LHCPMC		OFF	ON	
MB91F524LKCPMC			OFF	
MB91F523LSCPMC		ON	ON	
MB91F523LUCPMC			OFF	
MB91F523LHCPMC		OFF	ON	
MB91F523LKCPMC			OFF	
MB91F522LSCPMC		ON	ON	
MB91F522LUCPMC			OFF	
MB91F522LHCPMC		OFF	ON	
MB91F522LKCPMC			OFF	

Page	Section	Change Results				
8	■Product Lineup	Corrected the following description for Product lineup comparison(100 pin). <table><tr><td>Multi-Function Serial Interface</td><td>12ch</td></tr></table> ↓ <table><tr><td>Multi-Function Serial Interface</td><td>12ch*1</td></tr></table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
8	■Product Lineup	Added the following sentences under Product lineup comparison(100 pin) *1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I ² C (standard mode).				
9	■Product Lineup	Corrected the following description for Product lineup comparison(120 pin). <table><tr><td>Multi-Function Serial Interface</td><td>12ch</td></tr></table> ↓ <table><tr><td>Multi-Function Serial Interface</td><td>12ch*1</td></tr></table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
9	■Product Lineup	Added the following sentences under Product lineup comparison(120 pin) *1: Only channel 3 and channel 4 support the I ² C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I ² C (standard mode).				
10	■Product Lineup	Corrected the following description for Product lineup comparison(144 pin). <table><tr><td>Multi-Function Serial Interface</td><td>12ch</td></tr></table> ↓ <table><tr><td>Multi-Function Serial Interface</td><td>12ch*1</td></tr></table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
10	■Product Lineup	Added the following sentences under Product lineup comparison(144 pin) *1: Only channel 3 and channel 4 support the I ² C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I ² C (standard mode).				
11	■Product Lineup	Corrected the following description for Product lineup comparison(176 pin). <table><tr><td>Multi-Function Serial Interface</td><td>12ch</td></tr></table> ↓ <table><tr><td>Multi-Function Serial Interface</td><td>12ch*1</td></tr></table>	Multi-Function Serial Interface	12ch	Multi-Function Serial Interface	12ch*1
Multi-Function Serial Interface	12ch					
Multi-Function Serial Interface	12ch*1					
11	■Product Lineup	Added the following sentences under Product lineup comparison(176 pin) *1: Only channel 3 and channel 4 support the I ² C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I ² C (standard mode).				

Page	Section	Change Results																																																																																																		
15	■ Pin Assignment MB91F52xF	Signals indicated by the shading below deleted in Figure.																																																																																																		
		<div>(Error) - Bottom</div> <table><tr><td>49</td><td>P087/DA00/PG7_0/INT8_0</td><td>50</td><td>VCC</td></tr><tr><td>48</td><td>P086/DA01/PG6_0</td><td>49</td><td>P087/DA00/PG7_0/INT8_0</td></tr><tr><td>47</td><td>P082/SIN5_0/ANI/PG2_0</td><td>48</td><td>P086/DA01/PG6_0</td></tr><tr><td>46</td><td>P081/SOT5_0/SDA5/ANO/PG1_0</td><td>47</td><td>P082/SIN5_0/ANI/PG2_0</td></tr><tr><td>45</td><td>P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1</td><td>46</td><td>P081/SOT5_0/SDA5/ANO/PG1_0</td></tr><tr><td>44</td><td>P152/SCS53_0</td><td>45</td><td>P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1</td></tr><tr><td>43</td><td>P073/SOT4_0/SDA4/AN33/ICU3_2</td><td>44</td><td>P152/SCS53_0</td></tr><tr><td>42</td><td>P072/SIN4_0/AN34/ICU2_2/INT5_0</td><td>43</td><td>P073/AN33/ICU3_2</td></tr><tr><td>41</td><td>P071/SCK4_2/AN35/ICU1_2/MONCLK</td><td>42</td><td>P072/SIN4_0/AN34/ICU2_2/INT5_0</td></tr><tr><td>40</td><td>P070/ICU0_2</td><td>41</td><td>P071/SCK4_2/AN35/ICU1_2/MONCLK</td></tr><tr><td>39</td><td>P067/AN36/FRCK5_0/AIN0_1</td><td>40</td><td>P070/ICU0_2</td></tr><tr><td>38</td><td>P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1</td><td>39</td><td>P067/AN36/FRCK5_0/AIN0_1</td></tr><tr><td>37</td><td>P065/SCS43_0/FRCK3_0/ZIN0_1/PG44_1</td><td>38</td><td>P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1</td></tr><tr><td>36</td><td>P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PG43_1</td><td>37</td><td>P065/SCS43_0/FRCK3_0/ZIN0_1/PG44_1</td></tr><tr><td>35</td><td>P063/SCS41_0/AN39/PG5_1/FRCK1_0/BIN1_1</td><td>36</td><td>P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PG43_1</td></tr><tr><td>34</td><td>P062/SCS10_1/SCS40_0/AN40/PG4_1/FRCK0_0/TOT7_1/ZIN1_1</td><td>35</td><td>P063/SCS41_0/AN39/PG5_1/FRCK1_0/BIN1_1</td></tr><tr><td>33</td><td>P061/SOT10_1/AN41/ICU6_0/PG3_1/ICU3_1/TOT6_1/INT13_1</td><td>34</td><td>P062/SCS10_1/SCS40_0/AN40/PG4_1/FRCK0_0/TOT7_1/ZIN1_1</td></tr><tr><td>32</td><td>P060/SCS10_0/PG2_1/ICU2_1/TOT5_1/INT13_0</td><td>33</td><td>P061/SOT10_1/AN41/ICU6_0/PG3_1/ICU3_1/TOT6_1/INT13_1</td></tr><tr><td>31</td><td>AVSSI/AVRL1</td><td>32</td><td>P060/SCS10_0/PG2_1/ICU2_1/TOT5_1/INT13_0</td></tr><tr><td>30</td><td>AVRHI</td><td>31</td><td>AVSSI/AVRL1</td></tr><tr><td>29</td><td>P057/SCK10_1/AN42/ICU8_0/TRG0_2/PG1_1/ICU1_1/TIN6_1</td><td>30</td><td>AVRHI</td></tr><tr><td>28</td><td>AVCCI</td><td>29</td><td>P057/SCK10_1/AN42/ICU8_0/TRG0_2/PG1_1/ICU1_1/TIN6_1</td></tr><tr><td>27</td><td>P055/SIN10_0/AN43/PG37_0/TIN4_1</td><td>28</td><td>AVCCI</td></tr><tr><td>26</td><td>VSS</td><td>27</td><td>P055/SIN10_0/AN43/PG37_0/TIN4_1</td></tr><tr><td></td><td></td><td>26</td><td>VSS</td></tr></table>	49	P087/DA00/PG7_0/INT8_0	50	VCC	48	P086/DA01/PG6_0	49	P087/DA00/PG7_0/INT8_0	47	P082/SIN5_0/ANI/PG2_0	48	P086/DA01/PG6_0	46	P081/SOT5_0/SDA5/ANO/PG1_0	47	P082/SIN5_0/ANI/PG2_0	45	P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1	46	P081/SOT5_0/SDA5/ANO/PG1_0	44	P152/SCS53_0	45	P153/SCK5_0/SC15/AN32/FRCK1_1/INT4_1	43	P073/SOT4_0/SDA4/AN33/ICU3_2	44	P152/SCS53_0	42	P072/SIN4_0/AN34/ICU2_2/INT5_0	43	P073/AN33/ICU3_2	41	P071/SCK4_2/AN35/ICU1_2/MONCLK	42	P072/SIN4_0/AN34/ICU2_2/INT5_0	40	P070/ICU0_2	41	P071/SCK4_2/AN35/ICU1_2/MONCLK	39	P067/AN36/FRCK5_0/AIN0_1	40	P070/ICU0_2	38	P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1	39	P067/AN36/FRCK5_0/AIN0_1	37	P065/SCS43_0/FRCK3_0/ZIN0_1/PG44_1	38	P066/SOT4_2/SCS3_0/AN37/FRCK4_0/BIN0_1	36	P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PG43_1	37	P065/SCS43_0/FRCK3_0/ZIN0_1/PG44_1	35	P063/SCS41_0/AN39/PG5_1/FRCK1_0/BIN1_1	36	P064/SCS42_0/AN38/FRCK2_0/AIN1_1/PG43_1	34	P062/SCS10_1/SCS40_0/AN40/PG4_1/FRCK0_0/TOT7_1/ZIN1_1	35	P063/SCS41_0/AN39/PG5_1/FRCK1_0/BIN1_1	33	P061/SOT10_1/AN41/ICU6_0/PG3_1/ICU3_1/TOT6_1/INT13_1	34	P062/SCS10_1/SCS40_0/AN40/PG4_1/FRCK0_0/TOT7_1/ZIN1_1	32	P060/SCS10_0/PG2_1/ICU2_1/TOT5_1/INT13_0	33	P061/SOT10_1/AN41/ICU6_0/PG3_1/ICU3_1/TOT6_1/INT13_1	31	AVSSI/AVRL1	32	P060/SCS10_0/PG2_1/ICU2_1/TOT5_1/INT13_0	30	AVRHI	31	AVSSI/AVRL1	29	P057/SCK10_1/AN42/ICU8_0/TRG0_2/PG1_1/ICU1_1/TIN6_1	30	AVRHI	28	AVCCI	29	P057/SCK10_1/AN42/ICU8_0/TRG0_2/PG1_1/ICU1_1/TIN6_1	27	P055/SIN10_0/AN43/PG37_0/TIN4_1	28	AVCCI	26	VSS	27	P055/SIN10_0/AN43/PG37_0/TIN4_1		
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Page	Section	Change Results																				
135	■Interrupt Vector Table	<p>"42" is deleted as shown below from the interrupt factor in Interrupt vector 144pin.</p> <p>(Error)</p> <table><tr><td>PPG2/3/12/13/22/23/32/33/42/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000F FF58 H</td><td rowspan="2">25[*] 3</td></tr><tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr></table> <p>(Correct)</p> <table><tr><td>PPG2/3/12/13/22/23/32/33/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000F FF58 H</td><td rowspan="2">25[*] 3</td></tr><tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr></table>	PPG2/3/12/13/22/23/32/33/42/43	41	29	ICR 25	358 H	000F FF58 H	25 [*] 3	16-bit free-run timer 2 (0 detection) / (compare clear)	PPG2/3/12/13/22/23/32/33/43	41	29	ICR 25	358 H	000F FF58 H	25 [*] 3	16-bit free-run timer 2 (0 detection) / (compare clear)				
PPG2/3/12/13/22/23/32/33/42/43	41	29	ICR 25							358 H	000F FF58 H							25 [*] 3				
16-bit free-run timer 2 (0 detection) / (compare clear)																						
PPG2/3/12/13/22/23/32/33/43	41	29	ICR 25	358 H	000F FF58 H	25 [*] 3																
16-bit free-run timer 2 (0 detection) / (compare clear)																						
137	■Interrupt Vector Table	<p>The interrupt factor in Interrupt vector 144pin modified as follows:</p> <p>(Error)</p> <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45^{*5}</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>-</td></tr><tr><td>-</td></tr></table> <p>(Correct)</p> <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>-</td></tr><tr><td>-</td></tr></table>	Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45 ^{*5}	Base timer 1 IRQ1	-	-	Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45	Base timer 1 IRQ1	-	-
Base timer 1 IRQ0	61	3D	ICR 45							308 H	000F FF08 H	45 ^{*5}										
Base timer 1 IRQ1																						
-																						
-																						
Base timer 1 IRQ0	61	3D	ICR 45	308 H	000F FF08 H	45																
Base timer 1 IRQ1																						
-																						
-																						
137	■Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector 144pins.</p> <p>(Error)</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>																				

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