Infineon Technologies - MB91F526FSCPMC-GTE1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526fscpmc-gte1

- Power-on reset
- Low-voltage detection reset (independently monitor the external power supply and the internal power supply)
  - The external power supply can select initial value ON/OFF by the part number.
- Device Package : 176/144/120/100/80/64
- CMOS 90nm Technology
- Power supplies
  - 5V Power supply
  - The internal 1.2V is generated from 5V with the voltage step-down circuit

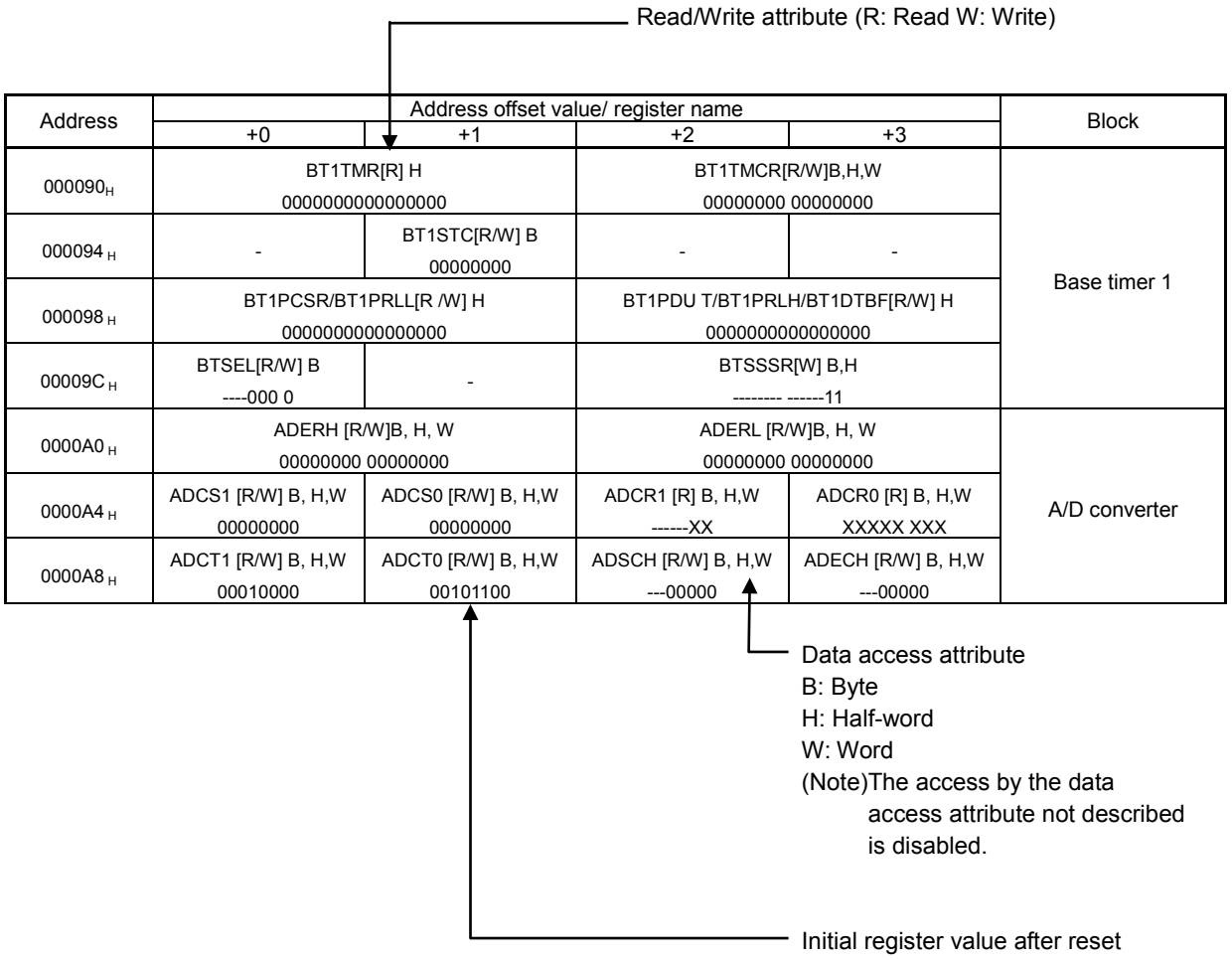
3. Pin Description

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	2	2	P015	-	A	General-purpose I/O port
						D29	-		External bus data bit29 I/O (0)
						TRG0_0	-		PPG trigger 0 input (0)
-	-	-	-	3	3	P016	-	A	General-purpose I/O port
						D30	-		External bus data bit30 I/O (0)
						TRG1_0	-		PPG trigger 1 input (0)
-	-	-	-	-	4	P170	-	A	General-purpose I/O port
						PPG36_1	-		PPG ch.36 output (1)
-	-	-	-	4	5	P017	-	A	General-purpose I/O port
						D31	-		External bus data bit31 I/O (0)
						TRG2_0	-		PPG trigger 2 input (0)
-	-	-	-	-	6	P171	-	A	General-purpose I/O port
						PPG37_1	-		PPG ch.37 output (1)
2 *1	2 *1	2 *1	2 *1	5	7	P020	-	F	General-purpose I/O port
						ASX *2, *3, *4, *5	-		External bus/Address strobe output
						SIN3_1	-		Multi-function serial ch.3 serial data input (1)
						TRG3_0	-		PPG trigger 3 input (0)
						TIN0_2	-		Reload timer ch.0 event input (2)
						RTO5_1	-		Waveform generator ch.5 output pin (1)
-	-	-	3 *1	6	8	P021	-	A	General-purpose I/O port
						CS0X *5	-		External bus chip select 0 output
						SOT3_1	-		Multi-function serial ch.3 serial data output (1)
						TRG6_1	-		PPG trigger 6 input (1)
						TRG4_0	-		PPG trigger 4 input (0)
-	-	-	4 *1	7	9	P022	-	F	General-purpose I/O port
						CS1X *5	-		External bus chip select 1 output
						SCK3_1	-		Multi-function serial ch.3 clock I/O (1)
						TRG7_1	-		PPG trigger 7 input (1)
						TRG5_0	-		PPG trigger 5 input (0)
-	-	-	5 *1	8	10	P023	-	A	General-purpose I/O port
						RDX *5	-		External bus/Read strobe output
						SCS3_1	-		Serial chip select 3 output (1)
						PPG32_0	-		PPG ch.32 output (0)
						TIN0_0	-		Reload timer ch.0 event input (0)

9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map



Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090 H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094 H	-	BT1STC[R/W] B 00000000	-	-	
000098 H	BT1PCSR/BT1PRLL[R /W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
00009C H	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -------- ------11		
0000A0 H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4 H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8 H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00049C$_H$	IORR12 [R/W] B,H,W -0000000	IORR13 [R/W] B,H,W -0000000	IORR14 [R/W] B,H,W -0000000	IORR15 [R/W] B,H,W -0000000	DMA request by peripheral [S]
0004A0$_H$	—	—	—	—	Reserved
0004A4$_H$	CANPRE [R/W] B,H,W ---00000	—	—	—	CAN prescaler
0004A8$_H$	—	—	CSCFG[R/W]B,H,W ---0----	CMCFG[R/W]B,H,W 00000000	Clock monitor control register
0004AC$_H$	ADERH0[R/W] B,H 11111111 11111111		ADERL0[R/W] B,H 11111111 11111111		Analog input control register 0
0004B0$_H$	—		ADERL1[R/W] B,H 11111111 11111111		Analog input control register 1
0004B4$_H$	—	—	—	—	Reserved
0004B8$_H$	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration
0004BC$_H$	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
0004C0$_H$	—	—	—	—	
0004C4$_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1 [R/W] B,H,W 11000011 01010000		
0004C8$_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
0004CC$_H$ to 00050C$_H$	—	—	—	—	Reserved
000510$_H$	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock Control [S]
000514$_H$	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518$_H$	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset Control [S]
00051C$_H$	—	—	—	—	Reserved [S]
000520$_H$	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock Control 2 [S]
000524$_H$	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528$_H$	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CF0_H$	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000CF4_H$	DCSR15 [R/W] H 0------- -----000		DTCR15 [R/W] H 00000000 00000000		
$000CF8_H$	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CFC_H$	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000D00_H$ to $000DF0_H$	—	—	—	—	Reserved [S]
$000DF4_H$	—	—	DNMIR [R/W] B 0------0	DILVR [R/W] B ---11111	DMA Controller [S]
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	—	—	—	—	Reserved [S]
$000E00_H$	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
$000E04_H$	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
$000E08_H$	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register
$000E0C_H$	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -0000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000	
$000E10_H$	—	—	—	—	
$000E14_H$	—	—	—	—	
$000E18_H$	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
$000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
$000E24_H$	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
$000E28_H$	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
$000E2C_H$	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
$000E30_H$	—	—	—	—	
$000E34_H$	—	—	—	—	
$000E38_H$	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001344_H	ADCOMP28/ADCOMPB28[R/W] H,W 00000000 00000000		ADCOMP29/ADCOMPB29[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001348_H	ADCOMP30/ADCOMPB30[R/W] H,W 00000000 00000000		ADCOMP31/ADCOMPB31[R/W] H,W 00000000 00000000		
$00134C_H$	ADTCS0[R/W] B,H,W 00000000 0010----		ADTCS1[R/W] B,H,W 00000000 0010----		
001350_H	ADTCS2[R/W] B,H,W 00000000 0010----		ADTCS3[R/W] B,H,W 00000000 0010----		
001354_H	ADTCS4[R/W] B,H,W 00000000 0010----		ADTCS5[R/W] B,H,W 00000000 0010----		
001358_H	ADTCS6[R/W] B,H,W 00000000 0010----		ADTCS7[R/W] B,H,W 00000000 0010----		
$00135C_H$	ADTCS8[R/W] B,H,W 00000000 0010----		ADTCS9[R/W] B,H,W 00000000 0010----		
001360_H	ADTCS10[R/W] B,H,W 00000000 0010----		ADTCS11[R/W] B,H,W 00000000 0010----		
001364_H	ADTCS12[R/W] B,H,W 00000000 0010----		ADTCS13[R/W] B,H,W 00000000 0010----		
001368_H	ADTCS14[R/W] B,H,W 00000000 0010----		ADTCS15[R/W] B,H,W 00000000 0010----		
$00136C_H$	ADTCS16[R/W] B,H,W 00000000 0010----		ADTCS17[R/W] B,H,W 00000000 0010----		
001370_H	ADTCS18[R/W] B,H,W 00000000 0010----		ADTCS19[R/W] B,H,W 00000000 0010----		
001374_H	ADTCS20[R/W] B,H,W 00000000 0010----		ADTCS21[R/W] B,H,W 00000000 0010----		
001378_H	ADTCS22[R/W] B,H,W 00000000 0010----		ADTCS23[R/W] B,H,W 00000000 0010----		
$00137C_H$	ADTCS24[R/W] B,H,W 00000000 0010----		ADTCS25[R/W] B,H,W 00000000 0010----		
001380_H	ADTCS26[R/W] B,H,W 00000000 0010----		ADTCS27[R/W] B,H,W 00000000 0010----		
001384_H	ADTCS28[R/W] B,H,W 00000000 0010----		ADTCS29[R/W] B,H,W 00000000 0010----		
001388_H	ADTCS30[R/W] B,H,W 00000000 0010----		ADTCS31[R/W] B,H,W 00000000 0010----		
$00138C_H$	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001390_H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001394_H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		12-bit A/D converter 1/2 unit
001398_H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
$00139C_H$	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
$0013A0_H$	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
$0013A4_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
$0013A8_H$	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
$0013AC_H$	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
$0013B0_H$	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
$0013B4_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
$0013B8_H$	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
$0013BC_H$	ADTCD24[R] B,H,W 10--0000 00000000		ADTCD25[R] B,H,W 10--0000 00000000		
$0013C0_H$	ADTCD26[R] B,H,W 10--0000 00000000		ADTCD27[R] B,H,W 10--0000 00000000		
$0013C4_H$	ADTCD28[R] B,H,W 10--0000 00000000		ADTCD29[R] B,H,W 10--0000 00000000		
$0013C8_H$	ADTCD30[R] B,H,W 10--0000 00000000		ADTCD31[R] B,H,W 10--0000 00000000		
$0013CC_H$	ADTECS0[R/W] B,H,W -------0 ---00000		ADTECS1[R/W] B,H,W -------0 ---00000		
$0013D0_H$	ADTECS2[R/W] B,H,W -------0 ---00000		ADTECS3[R/W] B,H,W -------0 ---00000		
$0013D4_H$	ADTECS4[R/W] B,H,W -------0 ---00000		ADTECS5[R/W] B,H,W -------0 ---00000		
$0013D8_H$	ADTECS6[R/W] B,H,W -------0 ---00000		ADTECS7[R/W] B,H,W -------0 ---00000		
$0013DC_H$	ADTECS8[R/W] B,H,W -------0 ---00000		ADTECS9[R/W] B,H,W -------0 ---00000		
$0013E0_H$	ADTECS10[R/W] B,H,W -------0 ---00000		ADTECS11[R/W] B,H,W -------0 ---00000		
$0013E4_H$	ADTECS12[R/W] B,H,W -------0 ---00000		ADTECS13[R/W] B,H,W -------0 ---00000		

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1,*4
A/D converter 0/1/7/10/11/14/15/16/17/22/27/28/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/34/35/37/38/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU7/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
-	60	3C	ICR44	$30C_H$	$000FFF0C_H$	-*6
- -	61	3D	ICR45	308_H	$000FFF08_H$	-
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS™*8)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-

11. Electrical Characteristics

Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage *1,*2		V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog power supply voltage *1,*2		AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC} ≤ V_{CC}
Analog reference voltage *1		AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC}
Input voltage *1		V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage *1		V_{IA5}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage *1		V_o	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current		I_{CLAMP}	-	4.0	mA	*6
Total maximum clamp current		$\Sigma\|I_{CLAMP}\|$	-	20	mA	*6
"L" level maximum output current *3		I_{OL1}	-	15	mA	
		I_{OL2}	-	30	mA	
"L" level average output current *4		I_{OLAV1}	-	4	mA	*9
		I_{OLAV2}	-	12	mA	*10
"L" level total output current *5		ΣI_{OL1}	-	100	mA	
		ΣI_{OL2}	-	120	mA	
"H" level maximum output current*3		I_{OH1}	-	-15	mA	
		I_{OH2}	-	-30	mA	
"H" level average output current*4		I_{OHAV1}	-	-4	mA	*9
		I_{OHAV2}	-	-12	mA	*10
"H" level total output current *5		ΣI_{OH1}	-	-100	mA	
		ΣI_{OH2}	-	-120	mA	
Power consumption	T_A: -40°C to +105°C	P_D	-	882	mW	*8
	T_A: -40°C to +125°C		-	675	mW	*8
Operating temperature		T_A	-40	+105	°C	
			-40	+125	°C	*7
Storage temperature		Tstg	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0V

*2: Caution must be taken that AV_{CC}, AVRH do not exceed V_{CC} upon power-on and under other circumstances.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6:
- Corresponding pins: all general-purpose ports except P035, 041, 093, 122.
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*7: When it is used under this condition, contact your sales representative.

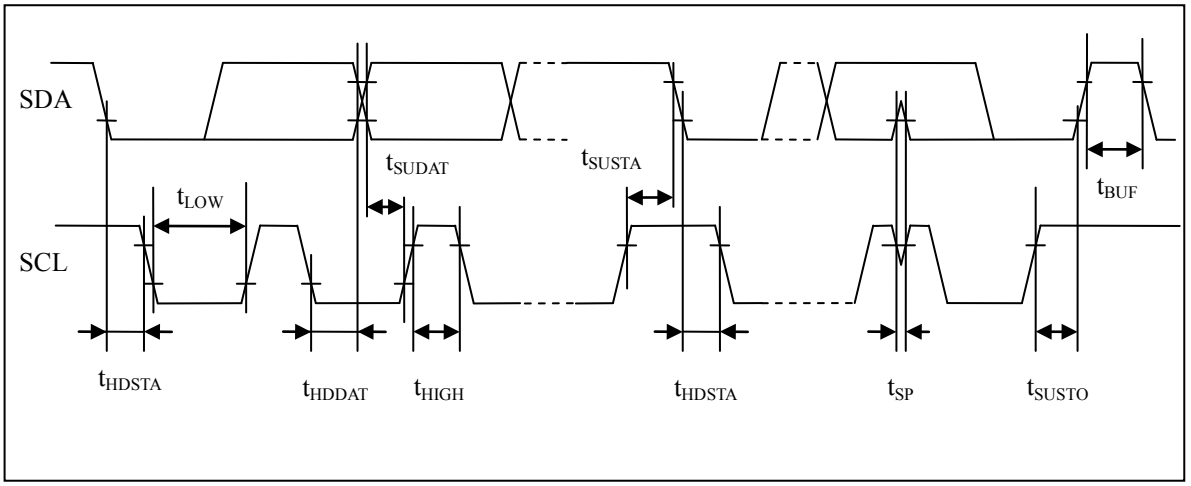
(T_A: -40°C to +125°C, V_{CC}= AVcc=5.0V±10%/3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value Min	Value Typ	Value Max	Unit	Remarks
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	60	102	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write		-	70	115	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase		-	70	115	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	54	92	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write		-	64	105	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase		-	64	105	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	46	82	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write		-	56	95	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase		-	56	95	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	45	82	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	23	72	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*	-	1500	2610	µA	
				When using built-in CR clock 50kHz T_A=+25°C*	-	450	2000		
				When using sub clock 32kHz T_A=+25°C*	-	460	2000		
	$I_{CCH}5$		Stop mode	T_A=+25°C*	-	450	2000	µA	
	$I_{CCT}52$		Watch mode (power off)	When using crystal 4MHz T_A=+25°C*	-	1100	1300	µA	LVD/ RTC operation , Backup RAM 8KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*	-	77	267		
				When using sub clock 32kHz T_A=+25°C*	-	100	285		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*	-	74	265	µA	Backup RAM 8KB retention

"t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I^2C.

・ I^2C timing



(9) Low voltage detection (Internal low-voltage detection)
(T_A: -40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

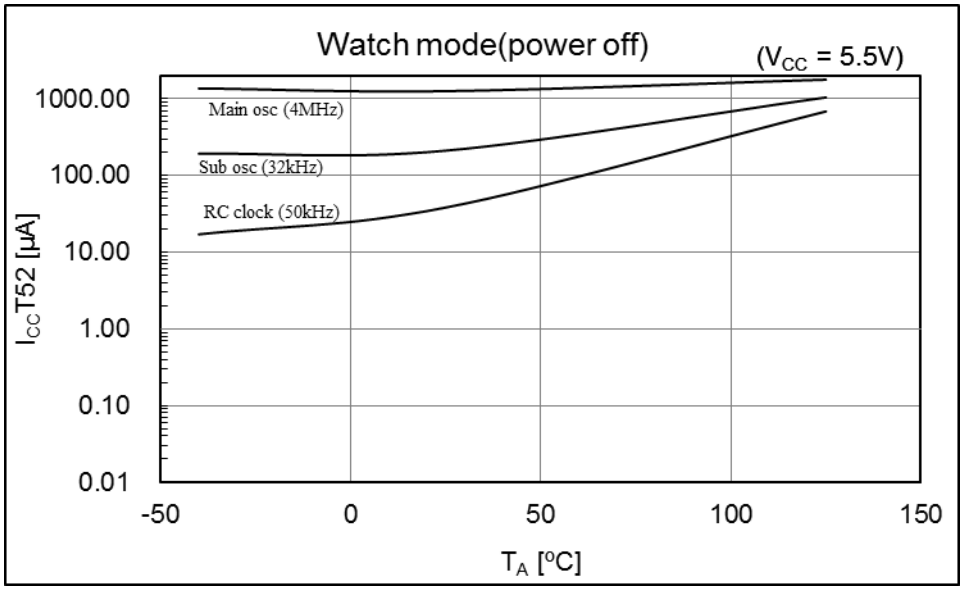
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage*2	V_{RDL}		*1	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	-	-		-	-	30	µs	

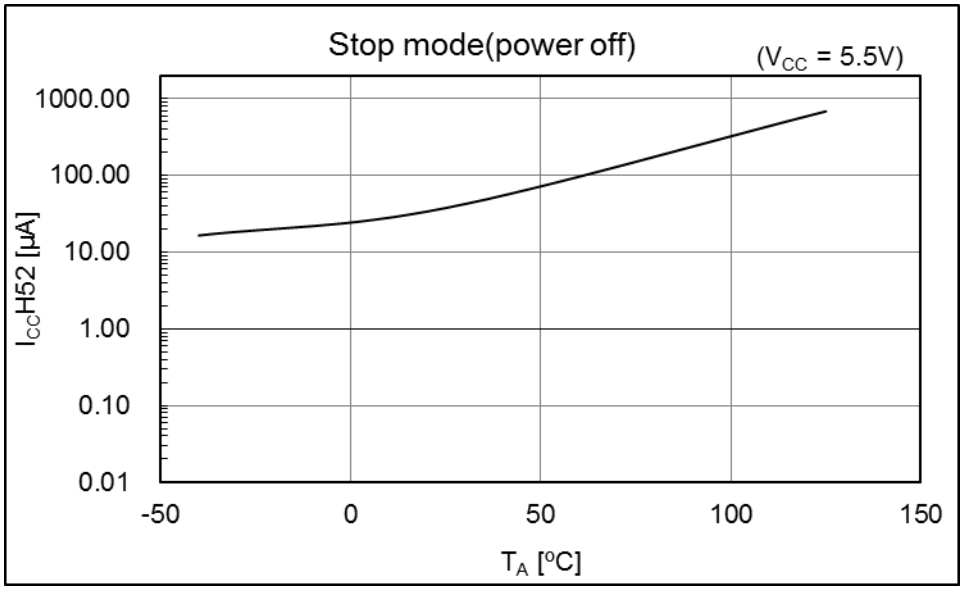
*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.
*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V.
This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(10) External bus I/F (synchronous mode) timing
(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	V_{CC}=5.0V±10%*1
			31.25			V_{CC}=3.3V±0.3V
ASX delay time	t_{CHASL}, t_{CHASH}	SYSCLK ASX	0.5	18	ns	
CS0X to CS3X delay time	t_{CHCSL}, t_{CHCSH}	SYSCLK CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t_{CHAV}, t_{CHAX}	SYSCLK A00 to A21	0.5	18	ns	
RDX delay time	t_{CHRL}, t_{CHRH}	SYSCLK RDX	0.5	18	ns	
RDX minimum pulse	t_{RLRH}	RDX	t_{CYC}× 2 - 20	-	ns	RWT=1, set RWT to 1 or more.*2
Data setup → RDX↑time	t_{DSRH}	RDX D16 to D31	18+t_{CYC}	-	ns	Same as above
RDX↑→ data hold	t_{RHDH}		0	-	ns	

MB91F526


Watch mode(power off)
(V_{CC} = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
I_{CC}T52 [µA]
-50
0
50
100
150
T_A [°C]


Stop mode(power off)
(V_{CC} = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
I_{CC}H52 [µA]
-50
0
50
100
150
T_A [°C]

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYBPMC1			OFF	
MB91F526KJBPMC1		OFF	ON	
MB91F526KLBPMC1			OFF	
MB91F525KWBPMC1		ON	ON	
MB91F525KYBPMC1			OFF	
MB91F525KJBPMC1		OFF	ON	
MB91F525KLBPMC1			OFF	
MB91F524KWBPMC1		ON	ON	
MB91F524KYBPMC1			OFF	
MB91F524KJBPMC1		OFF	ON	
MB91F524KLBPMC1			OFF	
MB91F523KWBPMC1		ON	ON	
MB91F523KYBPMC1			OFF	
MB91F523KJBPMC1		OFF	ON	
MB91F523KLBPMC1			OFF	
MB91F522KWBPMC1		ON	ON	
MB91F522KYBPMC1			OFF	
MB91F522KJBPMC1		OFF	ON	
MB91F522KLBPMC1			OFF	
MB91F526KSBPMC1	None	ON	ON	
MB91F526KUBPMC1			OFF	
MB91F526KHBPMC1		OFF	ON	
MB91F526KKBPMC1			OFF	
MB91F525KSBPMC1		ON	ON	
MB91F525KUBPMC1			OFF	
MB91F525KHBPMC1		OFF	ON	
MB91F525KKBPMC1			OFF	
MB91F524KSBPMC1		ON	ON	
MB91F524KUBPMC1			OFF	
MB91F524KHBPMC1		OFF	ON	
MB91F524KKBPMC1			OFF	
MB91F523KSBPMC1		ON	ON	
MB91F523KUBPMC1			OFF	
MB91F523KHBPMC1		OFF	ON	
MB91F523KKBPMC1			OFF	
MB91F522KSBPMC1		ON	ON	
MB91F522KUBPMC1			OFF	
MB91F522KHBPMC1		OFF	ON	
MB91F522KKBPMC1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526BWDPMC1	Yes	ON	ON	LQD・64 pin, Plastic
MB91F526BJDPMC1		OFF	ON	
MB91F525BWDPMC1		ON	ON	
MB91F525BJDPMC1		OFF	ON	
MB91F524BWDPMC1		ON	ON	
MB91F524BJDPMC1		OFF	ON	
MB91F523BWDPMC1		ON	ON	
MB91F523BJDPMC1		OFF	ON	
MB91F522BWDPMC1		ON	ON	
MB91F522BJDPMC1		OFF	ON	
MB91F526BSDPMC1	None	ON	ON	
MB91F526BHDPMC1		OFF	ON	
MB91F525BSDPMC1		ON	ON	
MB91F525BHDPMC1		OFF	ON	
MB91F524BSDPMC1		ON	ON	
MB91F524BHDPMC1		OFF	ON	
MB91F523BSDPMC1		ON	ON	
MB91F523BHDPMC1		OFF	ON	
MB91F522BSDPMC1		ON	ON	
MB91F522BHDPMC1		OFF	ON	

*: For details of the package, see "■ PACKAGE DIMENSIONS ".

Page	Section	Change Results
8	■Product Lineup	Corrected the following description for Product lineup comparison(100 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
8	■Product Lineup	Added the following sentences under Product lineup comparison(100 pin) *1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
9	■Product Lineup	Corrected the following description for Product lineup comparison(120 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
9	■Product Lineup	Added the following sentences under Product lineup comparison(120 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
10	■Product Lineup	Corrected the following description for Product lineup comparison(144 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
10	■Product Lineup	Added the following sentences under Product lineup comparison(144 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).
11	■Product Lineup	Corrected the following description for Product lineup comparison(176 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
11	■Product Lineup	Added the following sentences under Product lineup comparison(176 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>25</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="10">19</td><td rowspan="10">24</td><td rowspan="10">29</td><td rowspan="10">35</td><td rowspan="10">41</td><td rowspan="10">51</td><td>P057</td></tr>
<tr><td>RDY</td></tr>
<tr><td>SCK10_1</td></tr>
<tr><td>AN42</td></tr>
<tr><td>ICU8_0</td></tr>
<tr><td>TRG0_2</td></tr>
<tr><td>PPG1_1</td></tr>
<tr><td>ICU1_1</td></tr>
<tr><td>TIN6_1</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td rowspan="10">19 *1</td><td rowspan="10">24 *1</td><td rowspan="10">29 *1</td><td rowspan="10">35 *1</td><td rowspan="10">41</td><td rowspan="10">51</td><td>P057</td></tr>
<tr><td>RDY *2, *3, *4, *5</td></tr>
<tr><td>SCK10_1</td></tr>
<tr><td>AN42</td></tr>
<tr><td>ICU8_0</td></tr>
<tr><td>TRG0_2</td></tr>
<tr><td>PPG1_1</td></tr>
<tr><td>ICU1_1</td></tr>
<tr><td>TIN6_1</td></tr>
</table></td></tr>
<tr><td>27</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">35</td><td rowspan="4">43</td><td rowspan="4">49</td><td rowspan="4">57</td><td rowspan="4">71</td><td>P073</td></tr>
<tr><td>SOT4_0/ SDA4</td></tr>
<tr><td>AN33</td></tr>
<tr><td>ICU3_2</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">35 *3</td><td rowspan="4">43 *4</td><td rowspan="4">49</td><td rowspan="4">57</td><td rowspan="4">71</td><td>P073</td></tr>
<tr><td>SOT4_0/ SDA4 *3, *4</td></tr>
<tr><td>AN33</td></tr>
<tr><td>ICU3_2</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>29</td><td>■PIN Description</td><td>A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="8">34</td><td rowspan="8">42</td><td rowspan="8">52</td><td rowspan="8">62</td><td rowspan="8">77</td><td rowspan="8">96</td><td>P093</td></tr>
<tr><td>TX0_1</td></tr>
<tr><td>SIN11_0</td></tr>
<tr><td>AN7</td></tr>
<tr><td>ICU4_2</td></tr>
<tr><td>PPG16_1</td></tr>
<tr><td>ICU3_0</td></tr>
<tr><td>TOT2_1</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="8">34*1</td><td rowspan="8">42*1</td><td rowspan="8">52</td><td rowspan="8">62</td><td rowspan="8">77</td><td rowspan="8">96</td><td>P093</td></tr>
<tr><td>TX0_1</td></tr>
<tr><td>SIN11_0</td></tr>
<tr><td>AN7</td></tr>
<tr><td>ICU4_2</td></tr>
<tr><td>PPG16_1</td></tr>
<tr><td>ICU3_0</td></tr>
<tr><td>TOT2_1*2, *3</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type L in "I/O Circuit Types" modified as follows:

(Error)
- Open-drain I/O
- Output 25mA (NOD)
- TTL input

(Correct)
- Open-drain I/O
- Output 25mA (Nch open-drain)
- TTL input</td></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type M in "I/O Circuit Types" modified as follows:

(Error)
- CMOS hysteresis input
- Pull-up resistor 50kΩ (5V cont)

(Correct)
- CMOS hysteresis input
- Pull-up resistor 50kΩ</td></tr>
<tr><td>121</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 64pins.
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>124</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 80pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45*5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
</table>

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Package ↓ Package*2 Added the following description. *1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products. Corrected the following description. For details of the package, see "■ PACKAGE DIMENSIONS ". ↓ *2: For details of the package, see "■ PACKAGE DIMENSIONS ". Added the following description. • ORDERING INFORMATION MB91F52xxxC Company name and layout design change
*A	4999456	JHMU	11/13/2015	Updated to Cypress template. Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in “Absolute Maximum Ratings” of “ELECTRICAL CHARACTERISTICS”. *9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106. Added Errata section.
*B	5112138	KUME	01/28/2016	Fixed some clerical errors. For details, please see the chapter 18. Major Changes.
*C	5196285	KUME	04/28/2016	For details, please see the chapter 19. Major Changes.
*D	5318862	KUME	06/23/2016	For details, please see the chapter 19. Major Changes.