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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526lkbpmc-gsk5e1

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Product lineup comparison 100 pins

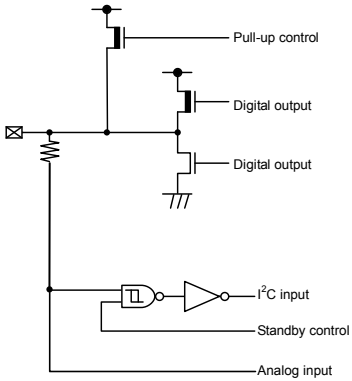
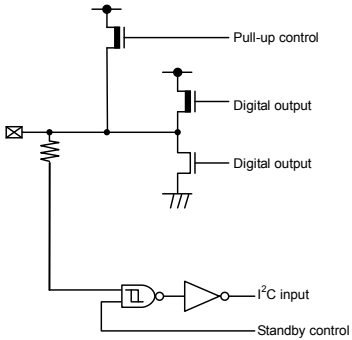
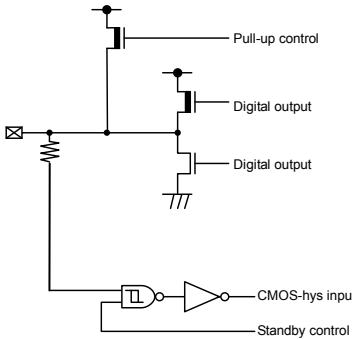
	MB91F522F	MB91F523F	MB91F524F	MB91F525F	MB91F526F
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB	(64+8)KB	(96+8)KB	(128+8)KB	
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	1ch				
Free-run Timer	16bit×3ch, 32bit×3ch				
Input capture	16bit×4ch, 32bit×6ch				
Output Compare	16bit×6ch, 32bit×6ch				
16-bit Reload Timer	8ch				
PPG	16bit×34ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×21ch (1unit), 12bit×16ch (1unit)				
D/A converter (8bit)	2ch				
Multi-Function Serial Interface	12ch ^{*1}				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	76 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
NMI request function	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
Operation guaranteed temperature (T _A)	-40°C to +125°C				
Power supply	2.7V to 5.5V ^{*2}				
Package	LQI100				

*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
13 *1	15 *1	19 *1	22 *1	25	31	P042	-	B	General-purpose I/O port
						A12 *2, *3, *4, *5	-		External bus/Address bit12 output
						SOT9_0	-		Multi-function serial ch.9 serial data output (0)
						AN47	-		ADC analog 47 input
						ICU8_1	-		Input capture ch.8 input (1)
						TRG0_1	-		PPG trigger 0 input (1)
						ZIN1_0	-		U/D counter ch.1 ZIN input (0)
-	-	20 *1	23 *1	26	32	P043	-	A	General-purpose I/O port
						A13 *4, *5	-		External bus/Address bit13 output (0)
						ICU7_1	-		Input capture ch.7 input (1)
						TRG1_1	-		PPG trigger 1 input (1)
-	16 *1	21 *1	24 *1	27	33	P044	-	A	General-purpose I/O port
						A14 *3, *4, *5	-		External bus/Address bit14 output (0)
						SCS9_0	-		Serial chip select 9 I/O (0)
						ICU6_1	-		Input capture ch.6 input (1)
						TRG2_1	-		PPG trigger 2 input (1)
14 *1	17 *1	22 *1	25 *1	28	34	P045	-	G	General-purpose I/O port
						A15 *2, *3, *4, *5	-		External bus/Address bit15 output (0)
						SCK9_0	-		Multi-function serial ch.9 clock I/O (0)
						AN46	-		ADC analog 46 input
						ICU5_1	-		Input capture ch.5 input (1)
						TRG3_1	-		PPG trigger 3 input (1)
						TOT1_2	-		Reload timer ch.1 output (2)
-	-	-	26 *1	29	35	P046	-	A	General-purpose I/O port
						A16 *5	-		External bus/Address bit16 output (0)
						ICU4_1	-		Input capture ch.4 input (1)
						TRG4_1	-		PPG trigger 4 input (1)
-	-	-	-	-	36	P176	-	A	General-purpose I/O port
						TRG10_0	-		PPG trigger 10 input (0)
15 *1	18 *1	23 *1	27 *1	30	37	P047	-	B	General-purpose I/O port
						A17 *2, *3, *4, *5	-		External bus/Address bit17 output (0)
						AN45	-		ADC analog 45 input
						TRG8_0	-		PPG trigger 8 input (0)
						TIN3_2	-		Reload timer ch.3 event input (2)
						SOT0_1	-		Multi-function serial ch.0 serial data output (1)
-	-	-	-	-	38	P177	-	A	General-purpose I/O port
						TRG11_0	-		PPG trigger 11 input (0)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	76	94	P092	-	B	General-purpose I/O port
						AN6	-		ADC analog 6 input
						PPG40_1	-		PPG ch.40 output (1)
						ICU2_0	-		Input capture ch.2 input (0)
						TOT0_1	-		Reload timer ch.0 output (1)
-	-	-	-	-	95	P192	-	A	General-purpose I/O port
						PPG24_1	-		PPG ch.24 output (1)
						TOT1_1	-		Reload timer ch.1 output (1)
34 *1	42 *1	52	62	77	96	P093	-	J	General-purpose I/O port
						TX0_1	-		CAN transmission data 0 output (1)
						SIN11_0	-		Multi-function serial ch.11 serial data input (0)
						AN7	-		ADC analog 7 input
						ICU4_2	-		Input capture ch.4 input (2)
						PPG16_1	-		PPG ch.16 output (1)
						ICU3_0	-		Input capture ch.3 input (0)
						TOT2_1 *2, *3	-		Reload timer ch.2 output (1)
-	-	-	-	78	97	P094	-	B	General-purpose I/O port
						AN8	-		ADC analog 8 input
						ICU4_0	-		Input capture ch.4 input (0)
						TOT3_1	-		Reload timer ch.3 output (1)
-	-	53	63	79	98	P095	-	B	General-purpose I/O port
						TX0(128)	-		CAN transmission data 0 output
						SCS11_0	-		Serial chip select 11 I/O (0)
						AN9	-		ADC analog 9 input
35	43	54	64	80	99	P096	-	G	General-purpose I/O port
						RX0(128)	-		CAN reception data 0 input
						SOT11_0 / SDA11	-		Multi-function serial ch.11 serial data output (0)/I ² C bus serial data I/O
						AN10	-		ADC analog 10 input
						INT0_0	-		INT0 External interrupt input (0)
36	44	55	65	81	100	P097	-	G	General-purpose I/O port
						SCK11_0 / SCL11	-		Multi-function serial ch.11 clock I/O (0)/I ² C bus serial clock I/O
						AN11	-		ADC analog 11 input
						ICU5_0	-		Input capture ch.5 input (0)
						PPG17_1	-		PPG ch.17 output (1)

Type	Circuit	Remarks
D		•I²C Analog input, General-purpose I/O port •Output 3mA •Pull-up resistor control 50kΩ •I²C hysteresis input
E		•I²C, General-purpose I/O port •Output 3mA •Pull-up resistor control 50kΩ •I²C hysteresis input
F		•General-purpose I/O port •Output 4mA •Pull-up resistor control 50kΩ •CMOS hysteresis input

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440 _H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444 _H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448 _H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
00044C _H	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450 _H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454 _H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458 _H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
00045C _H	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460 _H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464 _H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468 _H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
00046C _H	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470 _H to 00047C _H	—	—	—	—	Reserved [S]
000480 _H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111---0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484 _H	—	—	—	—	Reserved [S]
000488 _H	DIVR0 [R/W] B,H,W 000----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
00048C _H	—	—	—	—	Reserved [S]
000490 _H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494 _H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498 _H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E94 _H	—	—	—	—	Extended Port Function Register
000E98 _H	EPFR56 [R/W] B,H,W ----0-0	EPFR57 [R/W] B,H,W ----00-0	EPFR58 [R/W] B,H,W ----00-0	EPFR59 [R/W] B,H,W ----00-0	
000E9C _H	EPFR60 [R/W] B,H,W ----00-0	EPFR61 [R/W] B,H,W ----00-	EPFR62 [R/W] B,H,W ----00-	EPFR63 [R/W] B,H,W ---0000-	
000EA0 _H to 000EBC _H	—	—	—	—	Reserved
000EC0 _H	PPER00 [R/W] B,H,W 00000000	PPER01 [R/W] B,H,W 00000000	PPER02 [R/W] B,H,W 00000000	PPER03 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
000EC4 _H	PPER04 [R/W] B,H,W 00000000	PPER05 [R/W] B,H,W 00000000	PPER06 [R/W] B,H,W 00000000	PPER07 [R/W] B,H,W 00000000	
000EC8 _H	PPER08 [R/W] B,H,W 00000000	PPER09 [R/W] B,H,W 00000000	PPER10 [R/W] B,H,W 00000000	PPER11 [R/W] B,H,W 00000000	
000ECC _H	PPER12 [R/W] B,H,W 00000000	PPER13 [R/W] B,H,W -0000000	PPER14 [R/W] B,H,W ---000--	PPER15 [R/W] B,H,W --000000	
000ED0 _H	—	—	—	—	
000ED4 _H	—	—	—	—	
000ED8 _H	PPER16 [R/W] B,H,W 00000000	PPER17 [R/W] B,H,W 00000000	PPER18 [R/W] B,H,W 00000000	PPER19 [R/W] B,H,W 00000000	Reserved
000EDC _H to 000F3C _H	—	—	—	—	
000F40 _H	PORTEN [R/W] B,H,W -----0	—	—	—	Port Enable Register
000F44 _H	KEYCDR [R/W] H 00000000 00000000		—	—	KeyCodeRegister
000F48 _H to 000F64 _H	—	—	—	—	Reserved
000F68 _H	MSCY6 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 Cycle measurement data register 67
000F6C _H	MSCY7 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C78 _H	PCN232 [R/W] B,H,W --000000 -----110		PSDR32 [R/W] H,W 00000000 00000000		PPG32
001C7C _H	PTPC32 [R/W] H,W 00000000 00000000		—	—	
001C80 _H	PCN33 [R/W] B,H,W 00000000 000000-0		PCSR33 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG33
001C84 _H	PDUT33 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR33 [R] H,W 11111111 11111111		
001C88 _H	PCN233 [R/W] B,H,W --000000 -----110		PSDR33 [R/W] H,W 00000000 00000000		PPG33
001C8C _H	PTPC33 [R/W] H,W 00000000 00000000		—	—	
001C90 _H	PCN34 [R/W] B,H,W 00000000 000000-0		PCSR34 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG34
001C94 _H	PDUT34 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR34 [R] H,W 11111111 11111111		
001C98 _H	PCN234 [R/W] B,H,W --000000 -----110		PSDR34 [R/W] H,W 00000000 00000000		
001C9C _H	PTPC34 [R/W] H,W 00000000 00000000		—	—	
001CA0 _H	PCN35 [R/W] B,H,W 00000000 000000-0		PCSR35 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG35
001CA4 _H	PDUT35 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR35 [R] H,W 11111111 11111111		
001CA8 _H	PCN235 [R/W] B,H,W --000000 -----110		PSDR35 [R/W] H,W 00000000 00000000		
001CAC _H	PTPC35 [R/W] H,W 00000000 00000000		—	—	
001CB0 _H	PCN36 [R/W] B,H,W 00000000 000000-0		PCSR36 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG36
001CB4 _H	PDUT36 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR36 [R] H,W 11111111 11111111		
001CB8 _H	PCN236 [R/W] B,H,W --000000 -----110		PSDR36 [R/W] H,W 00000000 00000000		
001CBC _H	PTPC36 [R/W] H,W 00000000 00000000		—	—	
001CC0 _H	PCN37 [R/W] B,H,W 00000000 000000-0		PCSR37 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG37
001CC4 _H	PDUT37 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR37 [R] H,W 11111111 11111111		
001CC8 _H	PCN237 [R/W] B,H,W --000000 -----110		PSDR37 [R/W] H,W 00000000 00000000		

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
-	38	26	ICR22	364 _H	000FFF64 _H	-* ⁶
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
PPG 1/10/11/20/30/31	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/24/35	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 7/16/17/27/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 19	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48 _H	29
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
-	38	26	ICR22	364 _H	000FFF64 _H	-* ⁶
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
PPG 1/10/11/20/30/31	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/15/24/35	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 7/16/17/26/27/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/18/19/29	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48 _H	29
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						

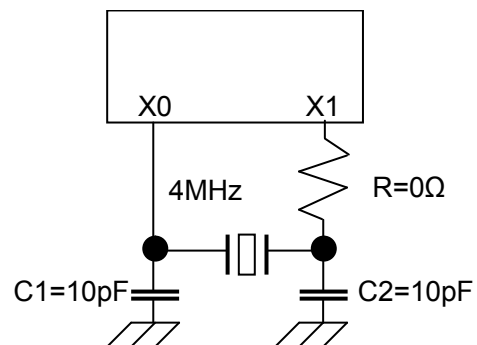
(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I _{IL}	All input pins	V _{CC} =AV _{CC} =5.5V V _{SS} <V _I <V _{CC}	-5	-	5	μA	
Input capacitance 1	C _{IN1}	Other than VCC, VSS, AVCC, AVSS, C	-	-	5	15	pF	
Pull-up resistance	R _{UP1}	RSTX, NMIX	V _{CC} =5.0V±10%	25	-	100	kΩ	
			V _{CC} =3.3V±0.3V	45	-	140		
	R _{UP2}	P073,074 076,077	V _{CC} =5.0V±10%	25	-	60		
			V _{CC} =3.3V±0.3V	33	-	90		
	R _{UP3}	Port pin other than P035, 041,073,074, 076,077,093, 122	V _{CC} =5.0V±10%	25	-	100	kΩ	
			V _{CC} =3.3V±0.3V	45	-	140		
“H” level output voltage	V _{OH1}	Normal output pin	V _{CC} =4.5V I _{OH} =-4.0mA	V _{CC} -0.5	-	V _{CC}	V	
			V _{CC} =3.0V I _{OH} =-2.0mA					
	V _{OH2}	P073,074,076, 077	V _{CC} =4.5V I _{OH} =-3.0mA	V _{CC} -0.5	-	V _{CC}	V	I ² C pin output
	V _{OH3}	P103 to 106	V _{CC} =4.5V I _{OH} =-12.0mA	V _{CC} -0.5	-	V _{CC}	V	
			V _{CC} =3.0V I _{OH} =-8.0mA					
	V _{OH3}	P103 to 106	V _{CC} =3.0V I _{OH} =-8.0mA	-0.5	-	V _{CC}	V	
“L” level output voltage	V _{OL1}	Normal output pin	V _{CC} =4.5V I _{OL} =4.0mA	0	-	0.4	V	
			V _{CC} =3.0V I _{OL} =2.0mA					
	V _{OL2}	P073,074,076, 077	V _{CC} =4.5V I _{OL} =3.0mA	0	-	0.4	V	I ² C pin output
	V _{OL3}	P103 to 106	V _{CC} =4.5V I _{OL} =12.0mA	0	-	0.4	V	
			V _{CC} =3.0V I _{OL} =8.0mA					
	V _{OL3}	P103 to 106	V _{CC} =3.0V I _{OL} =8.0mA	-0.5	-	V _{CC}	V	

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency							
		Main Clock	PLL clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 19	Multiplied by 20
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	76MHz	80MHz

• Example of oscillation circuit



Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.

Design your print circuit board so that the oscillator can start oscillation within 20ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.



External bus mode, write operation, and multiplex mode

Timing diagram showing signals and timing parameters:

- Signals:**
 - SYSCLK:** System clock signal.
 - ASX:** Address Strobe signal.
 - CS0X to CS3X:** Chip Select signals.
 - WR0X to WR1X:** Write Strobe signals.
 - D16 to D31:** Data bus signals.
- Timing Parameters:**
 - t_{OVC}:** Output Validity Delay.
 - ACS=0:** Address Validity Delay.
 - ASCY=0:** Address Validity Delay.
 - CSWR=2:** Chip Select Validity Delay.
 - WWT=0:** Write Strobe Validity Delay.
 - ADCY=1:** Address Validity Delay.
 - Valid Address:** Period during which the address is valid.
 - Write Data:** Period during which the data is valid.
- Clock Cycles:** The diagram is divided into four clock cycles: t1, t2, t3, and t4.

External bus in (non-bus mode, write operation, and spike mode) timing

The diagram illustrates the timing for an external bus in non-bus mode during a write operation. It shows the relationship between the system clock (SYSCLK) and various control and data signals over four clock cycles (t1, t2, t3, t4).

- SYSCLK:** The system clock, showing four full cycles (t1, t2, t3, t4). The clock period is labeled t_{cvc} .
- ASX:** The address strobe signal. It is active (low) during t1 and t2, and then becomes high (inactive) at the start of t3.
- CS0X to CS3X:** The chip select signals. They are active (low) during t1 and t2, and then become high (inactive) at the start of t3.
- WR0X to WR1X:** The write enable signals. They are active (low) during t1 and t2, and then become high (inactive) at the start of t3.
- A00 to A21:** The address bus. It is labeled "Valid Address" during t1 and t2, and then becomes invalid at the start of t3.
- D16 to D31:** The data bus. It is labeled "Write Data" during t1 and t2, and then becomes invalid at the start of t3.
- Timing Parameters:**
 - t_{cvc} : Clock cycle time.
 - $ACS=0$: Address strobe to chip select delay.
 - $WRCs=1$: Write enable to chip select delay.
 - $CSWR=0$, $WWT=0$: Chip select to write enable delay.
 - t_{ASWH} : Address strobe to address valid delay.
 - t_{WHAH} : Write enable to address valid delay.
 - t_{DSWH} : Data strobe to data valid delay.
 - t_{WHDH} : Write enable to data valid delay.

D/A converter

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	—	—	—	8	bit	
Differential linearity error	-	-	—	—	—	± 3.0	LSB	
Conversion time	-	-	—	0.47	0.58	0.69	μs	C _L =20
			—	2.37	2.90	3.43	μs	C _L =100
Output impedance	R _o	DA0, DA1	—	3.1	3.8	4.5	kΩ	
Power supply current *1	I _A	AVCC	—	—	475	580	μA	Each channel
	I _{AH}	AVCC	—	—	—	7.5	μA	When powerdown Each channel

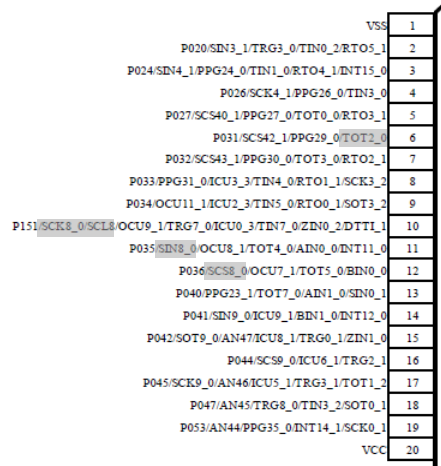
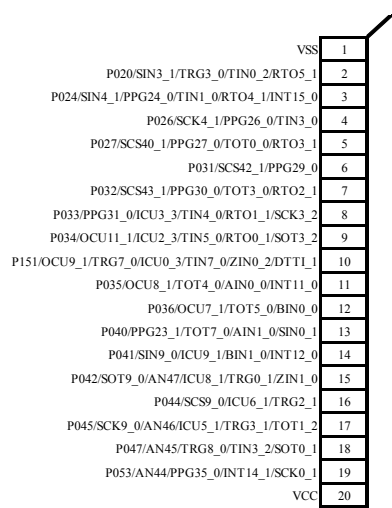
*1: The power supply current described only current value on D/A converter.

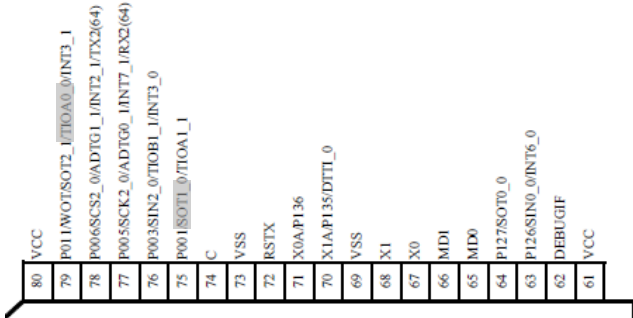
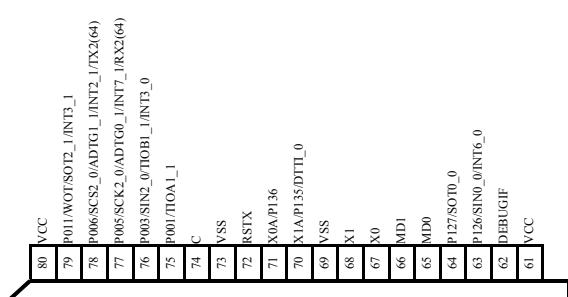
The total AV_{CC} current value must be calculated the power supply current for D/A converter and A/D converter.

Part number	Sub clock	CSV Initial value	LVD Initial value	Package ⁷²
MB91F526KWCPMC	Yes	ON	ON	LQS • 144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KYCPMC			OFF	
MB91F526KJCPMC		OFF	ON	
MB91F526KLCPMC			OFF	
MB91F525KWCPMC		ON	ON	
MB91F525KYCPMC			OFF	
MB91F525KJCPMC		OFF	ON	
MB91F525KLCPMC			OFF	
MB91F524KWCPMC		ON	ON	
MB91F524KYCPMC			OFF	
MB91F524KJCPMC		OFF	ON	
MB91F524KLCPMC			OFF	
MB91F523KWCPMC		ON	ON	
MB91F523KYCPMC			OFF	
MB91F523KJCPMC		OFF	ON	
MB91F523KLCPMC			OFF	
MB91F522KWCPMC		ON	ON	
MB91F522KYCPMC			OFF	
MB91F522KJCPMC		OFF	ON	
MB91F522KLCPMC			OFF	
MB91F526KSCPMC	None	ON	ON	
MB91F526KUCPMC			OFF	
MB91F526KHCPMC		OFF	ON	
MB91F526KKCPMC			OFF	
MB91F525KSCPMC		ON	ON	
MB91F525KUCPMC			OFF	
MB91F525KHCPMC		OFF	ON	
MB91F525KKCPMC			OFF	
MB91F524KSCPMC		ON	ON	
MB91F524KUCPMC			OFF	
MB91F524KHCPMC		OFF	ON	
MB91F524KKCPMC			OFF	
MB91F523KSCPMC		ON	ON	
MB91F523KUCPMC			OFF	
MB91F523KHCPMC		OFF	ON	
MB91F523KKCPMC			OFF	
MB91F522KSCPMC		ON	ON	
MB91F522KUCPMC			OFF	
MB91F522KHCPMC		OFF	ON	
MB91F522KKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package ^{*2}
MB91F526KWCPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KYCPMC1			OFF	
MB91F526KJCPMC1		OFF	ON	
MB91F526KLCPMC1			OFF	
MB91F525KWCPMC1		ON	ON	
MB91F525KYCPMC1			OFF	
MB91F525KJCPMC1		OFF	ON	
MB91F525KLCPMC1			OFF	
MB91F524KWCPMC1		ON	ON	
MB91F524KYCPMC1			OFF	
MB91F524KJCPMC1		OFF	ON	
MB91F524KLCPMC1			OFF	
MB91F523KWCPMC1		ON	ON	
MB91F523KYCPMC1			OFF	
MB91F523KJCPMC1		OFF	ON	
MB91F523KLCPMC1			OFF	
MB91F522KWCPMC1		ON	ON	
MB91F522KYCPMC1			OFF	
MB91F522KJCPMC1		OFF	ON	
MB91F522KLCPMC1			OFF	
MB91F526KSCPMC1	None	ON	ON	
MB91F526KUCPMC1			OFF	
MB91F526KHCPMC1		OFF	ON	
MB91F526KKCPMC1			OFF	
MB91F525KSCPMC1		ON	ON	
MB91F525KUCPMC1			OFF	
MB91F525KHCPMC1		OFF	ON	
MB91F525KKCPMC1			OFF	
MB91F524KSCPMC1		ON	ON	
MB91F524KUCPMC1			OFF	
MB91F524KHCPMC1		OFF	ON	
MB91F524KKCPMC1			OFF	
MB91F523KSCPMC1		ON	ON	
MB91F523KUCPMC1			OFF	
MB91F523KHCPMC1		OFF	ON	
MB91F523KKCPMC1			OFF	
MB91F522KSCPMC1		ON	ON	
MB91F522KUCPMC1			OFF	
MB91F522KHCPMC1		OFF	ON	
MB91F522KKCPMC1			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526KWDPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4mm) Plastic
MB91F526KJDPMC1		OFF	ON	
MB91F525KWDPMC1		ON	ON	
MB91F525KJDPMC1		OFF	ON	
MB91F524KWDPMC1		ON	ON	
MB91F524KJDPMC1		OFF	ON	
MB91F523KWDPMC1		ON	ON	
MB91F523KJDPMC1		OFF	ON	
MB91F522KWDPMC1		ON	ON	
MB91F522KJDPMC1		OFF	ON	
MB91F526KSDPMC1	None	ON	ON	
MB91F526KHDPMC1		OFF	ON	
MB91F525KSDPMC1		ON	ON	
MB91F525KHDPMC1		OFF	ON	
MB91F524KSDPMC1		ON	ON	
MB91F524KHDPMC1		OFF	ON	
MB91F523KSDPMC1		ON	ON	
MB91F523KHDPMC1		OFF	ON	
MB91F522KSDPMC1		ON	ON	
MB91F522KHDPMC1		OFF	ON	
MB91F526JWDPMC	Yes	ON	ON	LQM • 120 pin, Plastic
MB91F526JJDPMC		OFF	ON	
MB91F525JWDPMC		ON	ON	
MB91F525JJDPMC		OFF	ON	
MB91F524JWDPMC		ON	ON	
MB91F524JJDPMC		OFF	ON	
MB91F523JWDPMC		ON	ON	
MB91F523JJDPMC		OFF	ON	
MB91F522JWDPMC		ON	ON	
MB91F522JJDPMC		OFF	ON	
MB91F526JSDPMC	None	ON	ON	
MB91F526JHDPMC		OFF	ON	
MB91F525JSDPMC		ON	ON	
MB91F525JHDPMC		OFF	ON	
MB91F524JSDPMC		ON	ON	
MB91F524JHDPMC		OFF	ON	
MB91F523JSDPMC		ON	ON	
MB91F523JHDPMC		OFF	ON	
MB91F522JSDPMC		ON	ON	
MB91F522JHDPMC		OFF	ON	

Page	Section	Change Results
14	■ Pin Assignment MB91F52xD	Signals indicated by the shading below deleted in Figure. - Left side  ↓ 

Page	Section	Change Results
14	■ Pin Assignment MB91F52xD	- Top  ↓ 
14	■ Pin Assignment MB91F52xD	The following note added on the bottom left of Figure. * In a single clock product, pin 71 and pin 72 are the general-purpose ports.

Page	Section	Change Results
188	11. Electrical Characteristics (9) Low voltage detection (Internal low-voltage detection)	The following sentence modified as following: (Error) (9) Low voltage detection (RAM retention low-voltage detection) (Correct) (9) Low voltage detection (Internal low-voltage detection)
		The following symbol should be modified as follows: (Error) * (Correct) *1
		Note of Detection voltage should be added as follows: (Correct) Detection voltage *2 *2: The detection voltage of the internal low voltage detection is 0.9V±0.1V. This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
233 to 235	18. Errata	Limitation for Watch mode (power off) should be added in Errata.

Document History

Document Title: MB91520 Series 32-bit FR81S Microcontroller

Document Number: 002-04662

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	—	—	Initial release
	—	—	2/20/2014	Features: Corrected the following description. 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input ↓ 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input I/O CIRCUIT TYPE: Corrected the following description to "Type F, G, I, J, K, M". Schmitt input → CMOS hysteresis input