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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526lsbpmc-gsk5e1

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0001F8 _H	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXX		Reload Timer 6
0001FC _H	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000		
000200 _H to 000238 _H	—	—	—	—	Reserved
00023C _H	DACR0 [R/W] B,H,W -----0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -----0	DADR1 [R/W] B,H,W XXXXXXXX	DA Converter
000240 _H	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 3 32-bit FRT
000244 _H	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000248 _H	TCCSH3 [R/W] B,H,W 0-----00	TCCSL3 [R/W] B,H,W -1-00000	—	—	
00024C _H	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 4 32-bit FRT
000250 _H	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000254 _H	TCCSH4 [R/W] B,H,W 0-----00	TCCSL4 [R/W] B,H,W -1-00000	—	—	
000258 _H to 0002C0 _H	—	—	—	—	Reserved
0002C4 _H to 0002FC _H	—	—	—	—	Reserved
000300 _H to 00030C _H	—	—	—	—	Reserved
000310 _H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314 _H	—	—	—	—	
000318 _H	—				
00031C _H	—	—	—		
000320 _H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324 _H	—	—	DPVSR [R/W] H ----- 00000--0		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000328 _H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				MPU [S] (Only CPU core can access this area)
00032C _H	—	—	DESR [R/W] H ----- 00000--0		
000330 _H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334 _H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338 _H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00033C _H	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340 _H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only CPU core can access this area)
000344 _H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348 _H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00034C _H	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350 _H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354 _H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358 _H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00035C _H	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360 _H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364 _H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368 _H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				Reserved [S]
00036C _H	—	—	PACR7 [R/W] H 000000-0 00000--0		
000370 _H to 0003AC _H	—				
0003B0 _H to 0003FC _H	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001D20 _H	PCN43 [R/W] B,H,W 00000000 000000-0		PCSR43 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG43
001D24 _H	PDUT43 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR43 [R] H,W 11111111 11111111		
001D28 _H	PCN243 [R/W] B,H,W --000000 -----110		PSDR43 [R/W] H,W 00000000 00000000		
001D2C _H	PTPC43 [R/W] H,W 00000000 00000000		—	—	
001D30 _H	PCN44 [R/W] B,H,W 00000000 000000-0		PCSR44 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG44
001D34 _H	PDUT44 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR44 [R] H,W 11111111 11111111		
001D38 _H	PCN244 [R/W] B,H,W --000000 -----110		PSDR44 [R/W] H,W 00000000 00000000		
001D3C _H	PTPC44 [R/W] H,W 00000000 00000000		—	—	
001D40 _H	PCN45 [R/W] B,H,W 00000000 000000-0		PCSR45 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG45
001D44 _H	PDUT45 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR45 [R] H,W 11111111 11111111		
001D48 _H	PCN245 [R/W] B,H,W --000000 -----110		PSDR45 [R/W] H,W 00000000 00000000		
001D4C _H	PTPC45 [R/W] H,W 00000000 00000000		—	—	
001D50 _H	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG46
001D54 _H	PDUT46 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
001D58 _H	PCN246 [R/W] B,H,W --000000 -----110		PSDR46 [R/W] H,W 00000000 00000000		
001D5C _H	PTPC46 [R/W] H,W 00000000 00000000		—	—	
001D60 _H	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG47
001D64 _H	PDUT47 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
001D68 _H	PCN247 [R/W] B,H,W --000000 -----110		PSDR47 [R/W] H,W 00000000 00000000		
001D6C _H	PTPC47 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002150 _H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		CAN1 (64msb)
002154 _H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158 _H	—	—	—	—	
00215C _H	—	—	—	—	
002160 _H , 002164 _H	Reserved (IF2 data mirror)				
002168 _H to 00217C _H	—				
002180 _H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184 _H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188 _H	—	—	—	—	
00218C _H	—	—	—	—	
002190 _H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194 _H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198 _H	—	—	—	—	
00219C _H	—	—	—	—	
0021A0 _H	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
0021A4 _H	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
0021A8 _H	—	—	—	—	
0021AC _H	—	—	—	—	
0021B0 _H	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
0021B4 _H	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		
0021B8 _H	—	—	—	—	
0021BC _H	—	—	—	—	

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12 ^{*1}
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14 ^{*1}
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16 ^{*1}
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
-	38	26	ICR22	364 _H	000FFF64 _H	- ^{*6}
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
PPG 1/10/11/20/30/31	40	28	ICR24	35C _H	000FFF5C _H	24 ^{*3}
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/43	41	29	ICR25	358 _H	000FFF58 _H	25 ^{*3}
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/24/35	42	2A	ICR26	354 _H	000FFF54 _H	26 ^{*3}
PPG 7/16/17/27/37	43	2B	ICR27	350 _H	000FFF50 _H	27 ^{*3}
PPG 19	44	2C	ICR28	34C _H	000FFF4C _H	28 ^{*3}
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48 _H	29
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7 (status)						
16-bit Free-running timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 1/10/11/20/21/30/31	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/23/32/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/9/18/19/28/29	44	2C	ICR28	34C _H	000FFF4C _H	28* ³

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29* ¹
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						
Clock calibration unit (sub oscillation)	47	2F	ICR31	340 _H	000FFF40 _H	31* ¹ , * ⁴
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	33C _H	000FFF3C _H	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit Free-run timer 4	50	32	ICR34	334 _H	000FFF34 _H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit Free-run timer 3/5	51	33	ICR35	330 _H	000FFF30 _H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching/measurement)	52	34	ICR36	32C _H	000FFF2C _H	36* ¹
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching/measurement)	53	35	ICR37	328 _H	000FFF28 _H	37
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching/measurement)	54	36	ICR38	324 _H	000FFF24 _H	38* ¹
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching/measurement)	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer underflow 0/1/2						
WG dead timer reload 0/1/2						
WG DTTI 0						
32-bit ICU4 (fetching/measurement)	56	38	ICR40	31C _H	000FFF1C _H	40
Multi-function serial interface ch.11 (transmission completed)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
32-bit ICU5 (fetching/measurement)	57	39	ICR41	318 _H	000FFF18 _H	41
A/D converter						
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47						
32-bit OCU 6/7/10/11 (match)						
32-bit OCU 8/9 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
Base timer 0 IRQ0	59	3B	ICR43	310 _H	000FFF10 _H	43
Base timer 0 IRQ1						
Base timer 1 IRQ0	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 1 IRQ1						
-						
-						
DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	61	3D	ICR45	308 _H	000FFF08 _H	45
Delay interrupt	62	3E	ICR46	304 _H	000FFF04 _H	-
System reserved (Used for REALOS)	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFEFC _H	-
Used with the INT instruction	66	42	-	2F4 _H	000FFEFC _H	-
			-			-
	255	FF		000 _H	000FFC00 _H	

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I²C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

11. Electrical Characteristics

Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage *1,*2		V _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	
Analog power supply voltage *1,*2		AV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	AVRH ≤ AV _{CC} ≤ V _{CC}
Analog reference voltage *1		AVRH	V _{SS} -0.3	V _{SS} +6.0	V	AVRH ≤ AV _{CC}
Input voltage *1		V _I	V _{SS} -0.3	V _{CC} +0.3	V	
Analog pin input voltage *1		V _{IA5}	V _{SS} -0.3	V _{CC} +0.3	V	
Output voltage *1		V _o	V _{SS} -0.3	V _{CC} +0.3	V	
Maximum clamp current		I _{CLAMP}	-	4.0	mA	*6
Total maximum clamp current		Σ I _{CLAMP}	-	20	mA	*6
"L" level maximum output current *3		I _{OL1}	-	15	mA	
		I _{OL2}	-	30	mA	
"L" level average output current *4		I _{OLAV1}	-	4	mA	*9
		I _{OLAV2}	-	12	mA	*10
"L" level total output current *5		ΣI _{OL1}	-	100	mA	
		ΣI _{OL2}	-	120	mA	
"H" level maximum output current*3		I _{OH1}	-	-15	mA	
		I _{OH2}	-	-30	mA	
"H" level average output current*4		I _{OHAV1}	-	-4	mA	*9
		I _{OHAV2}	-	-12	mA	*10
"H" level total output current *5		ΣI _{OH1}	-	-100	mA	
		ΣI _{OH2}	-	-120	mA	
Power consumption	T _A : -40°C to +105°C	P _D	-	882	mW	*8
	T _A : -40°C to +125°C		-	675	mW	*8
Operating temperature		T _A	-40	+105	°C	
			-40	+125	°C	
Storage temperature		T _{stg}	-55	+150	°C	

*1: These parameters are based on the condition that $V_{SS}=AV_{SS}=0.0\text{V}$

*2: Caution must be taken that AV_{CC} , $AVRH$ do not exceed V_{CC} upon power-on and under other circumstances.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current $\times$ the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: · Corresponding pins: all general-purpose ports except P035, 041, 093, 122.

· Use within recommended operating conditions.

· Use at DC voltage (current).

· The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.

· The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.

· Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.

· Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.

· Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.

· Do not leave + B input pins open.

*7: When it is used under this condition, contact your sales representative.

(3) Power-on Conditions

(3-1) [MB9152xxxB/MB9152xxxC/MB9152xxxD]

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	—	V _{CC}	—	2.024	2.2	2.376	V	
Level detection hysteresis width	—	V _{CC}	—	—	100	—	mV	
Level detection time	—	—	—	—	—	30	μs	*1
Power off time	t _{OFF}	V _{CC}	—	50	—	—	ms	*2
Power ramp rate	dV/dt	V _{CC}	V _{CC} : 0.2V to 2.376V	—	—	4	mV/μs	*3
C pin voltage at Power-on	—	C	—	—	—	60	mV	*4

*1: This spec is at 4mV/μs of power ramp rate. If the power ramp rate is faster than 4mV/μs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}.

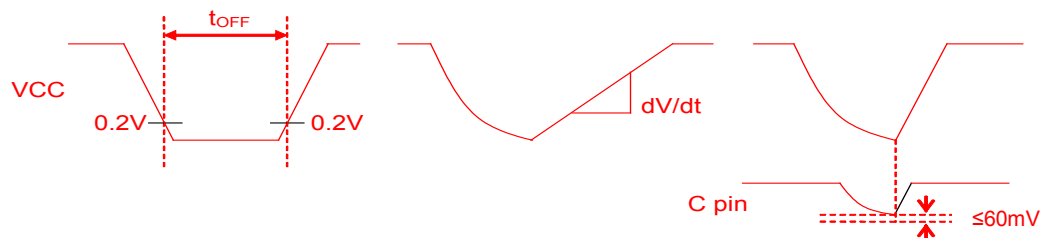
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when V_{CC} is turned on again.

Note:

When using MB91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use MB91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

• Power off time, Power ramp rate, C pin voltage at Power-on



Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}+30$	-	ns	External shift clock mode output pin: $C_L=50pF$
SCK↓→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}+30$	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1, SOT2, SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS↑→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: $C_L=50pF$
SCK↑→SCS↓ clock switch time	t_{SCC}	SCK1, SCK2, SCK5 to SCK11 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}-10$	$3t_{CPP}+50$	ns	Internal shift clock mode Round operation output pin: $C_L=50pF$
		SCK3, SCK4 SCS3, SCS40 to SCS43		$3t_{CPP}-300$	$3t_{CPP}+50$	ns	

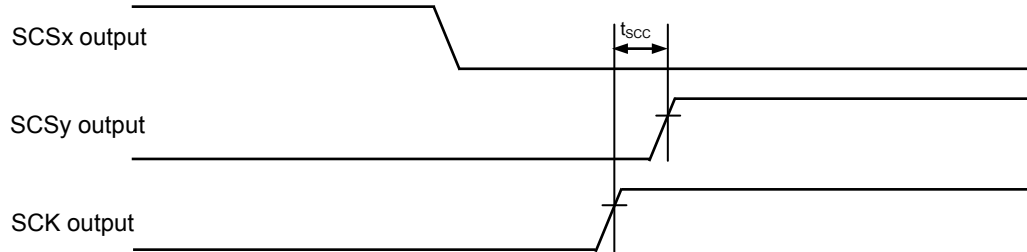
*1: t_{CSSU} = SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD7-0×Serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1, *2, and *3



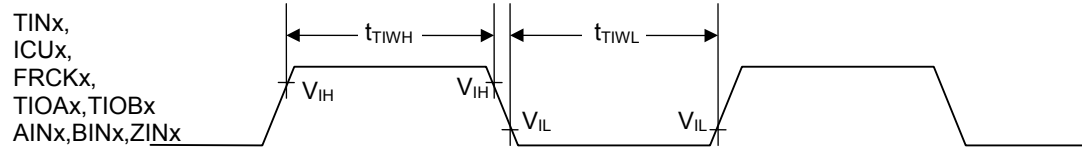
When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

(5) Timer input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TIWH} , t _{TIWL}	TIN0 to TIN7 ICU0 to ICU9 FRCK0 to FRCK5 TIOA0, TIOA1, TIOB0, TIOB1, AIN0, AIN1, BIN0, BIN1, ZIN0, ZIN1	—	4t _{CPP}	—	ns	

• Timer input timing

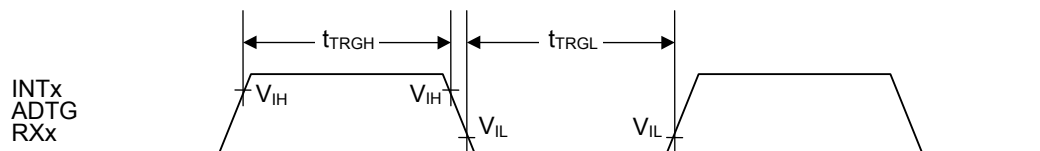


(6) Trigger input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TRGH} , t _{TRGL}	INT0 to INT15, ADTG, RX0, RX1, RX2	—	5t _{CPP}	—	ns	
				1	—	μs	At stop mode

• Trigger input timing

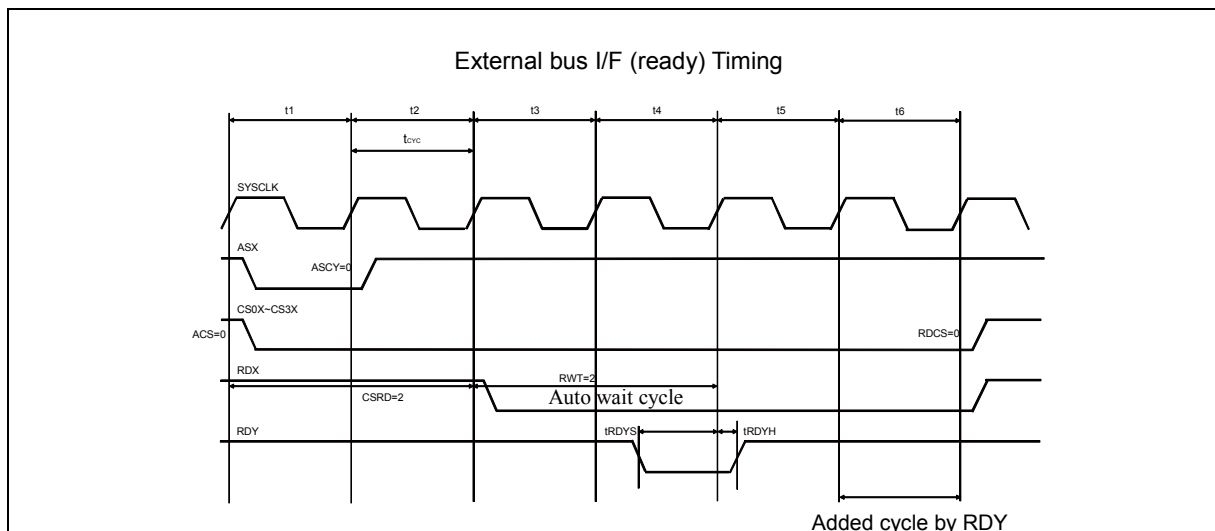


(12) External bus I/F (ready) Timing

(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK↑	t _{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK↑→ RDY hold time	t _{RDYH}	SYSCLK, RDY	0	-	ns	



13. Ordering Information MB91F52xxxB*¹

Part number	Sub clock	CSV Initial value	LVD Initial value	Package* ²
MB91F526LWBPMC	Yes	ON	ON	LQP • 176 pin, Plastic
MB91F526LYBPMC			OFF	
MB91F526LJBPMC		OFF	ON	
MB91F526LLBPMC			OFF	
MB91F525LWBPMC		ON	ON	
MB91F525LYBPMC			OFF	
MB91F525LJBPMC		OFF	ON	
MB91F525LLBPMC			OFF	
MB91F524LWBPMC		ON	ON	
MB91F524LYBPMC			OFF	
MB91F524LJBPMC		OFF	ON	
MB91F524LLBPMC			OFF	
MB91F523LWBPMC		ON	ON	
MB91F523LYBPMC			OFF	
MB91F523LJBPMC		OFF	ON	
MB91F523LLBPMC			OFF	
MB91F522LWBPMC		ON	ON	
MB91F522LYBPMC			OFF	
MB91F522LJBPMC		OFF	ON	
MB91F522LLBPMC			OFF	
MB91F526LSBPMC	None	ON	ON	
MB91F526LUBPMC			OFF	
MB91F526LHBPMC		OFF	ON	
MB91F526LKBPMC			OFF	
MB91F525LSBPMC		ON	ON	
MB91F525LUBPMC			OFF	
MB91F525LHBPMC		OFF	ON	
MB91F525LKBPMC			OFF	
MB91F524LSBPMC		ON	ON	
MB91F524LUBPMC			OFF	
MB91F524LHBPMC		OFF	ON	
MB91F524LKBPMC			OFF	
MB91F523LSBPMC		ON	ON	
MB91F523LUBPMC			OFF	
MB91F523LHBPMC		OFF	ON	
MB91F523LKBPMC			OFF	
MB91F522LSBPMC		ON	ON	
MB91F522LUBPMC			OFF	
MB91F522LHBPMC		OFF	ON	
MB91F522LKBPMC			OFF	

15. Ordering Information MB91F52xxxD

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWDPMC	Yes	ON	ON	LQP • 176 pin, Plastic
MB91F526LJDPMC		OFF	ON	
MB91F525LWDPMC		ON	ON	
MB91F525LJDPMC		OFF	ON	
MB91F524LWDPMC		ON	ON	
MB91F524LJDPMC		OFF	ON	
MB91F523LWDPMC		ON	ON	
MB91F523LJDPMC		OFF	ON	
MB91F522LWDPMC		ON	ON	
MB91F522LJDPMC		OFF	ON	
MB91F526LSDPMC	None	ON	ON	
MB91F526LHDPHC		OFF	ON	
MB91F525LSDPMC		ON	ON	
MB91F525LHDPHC		OFF	ON	
MB91F524LSDPMC		ON	ON	
MB91F524LHDPHC		OFF	ON	
MB91F523LSDPMC		ON	ON	
MB91F523LHDPHC		OFF	ON	
MB91F522LSDPMC		ON	ON	
MB91F522LHDPHC		OFF	ON	
MB91F526KWDPMC	Yes	ON	ON	LQS • 144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJDPMC		OFF	ON	
MB91F525KWDPMC		ON	ON	
MB91F525KJDPMC		OFF	ON	
MB91F524KWDPMC		ON	ON	
MB91F524KJDPMC		OFF	ON	
MB91F523KWDPMC		ON	ON	
MB91F523KJDPMC		OFF	ON	
MB91F522KWDPMC		ON	ON	
MB91F522KJDPMC		OFF	ON	
MB91F526KSDPMC	None	ON	ON	
MB91F526KHDPHC		OFF	ON	
MB91F525KSDPMC		ON	ON	
MB91F525KHDPHC		OFF	ON	
MB91F524KSDPMC		ON	ON	
MB91F524KHDPHC		OFF	ON	
MB91F523KSDPMC		ON	ON	
MB91F523KHDPHC		OFF	ON	
MB91F522KSDPMC		ON	ON	
MB91F522KHDPHC		OFF	ON	

Page	Section	Change Results																																																																																																																										
20	■PIN Description	A List of "Pin Description" modified.																																																																																																																										
		(Error)																																																																																																																										
		<table><tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr><tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr><tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">4</td><td rowspan="5">7</td><td rowspan="5">10</td><td rowspan="5">12</td><td>P025</td></tr><tr><td>WR1X</td></tr><tr><td>SOT4_1</td></tr><tr><td>PPG25_0</td></tr><tr><td>TIN2_0</td></tr><tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">13</td><td>P172</td></tr><tr><td>PPG38_1</td></tr><tr><td rowspan="5">-</td><td rowspan="5">4</td><td rowspan="5">5</td><td rowspan="5">8</td><td rowspan="5">11</td><td rowspan="5">14</td><td>P026</td></tr><tr><td>A00</td></tr><tr><td>SCK4_1</td></tr><tr><td>PPG26_0</td></tr><tr><td>TIN3_0</td></tr><tr><td rowspan="5">4</td><td rowspan="5">5</td><td rowspan="5">6</td><td rowspan="5">9</td><td rowspan="5">12</td><td rowspan="5">15</td><td>P027</td></tr><tr><td>A01</td></tr><tr><td>SCS40_1</td></tr><tr><td>PPG27_0</td></tr><tr><td>TOT0_0</td></tr><tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">16</td><td>RTO3_1</td></tr><tr><td>P173</td></tr><tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">7</td><td rowspan="5">10</td><td rowspan="5">13</td><td rowspan="5">17</td><td>PPG39_1</td></tr><tr><td>P030</td></tr><tr><td>A02</td></tr><tr><td>SCS41_1</td></tr><tr><td>PPG28_0</td></tr><tr><td rowspan="5">-</td><td rowspan="5">6</td><td rowspan="5">8</td><td rowspan="5">11</td><td rowspan="5">14</td><td rowspan="5">18</td><td>TOT1_0</td></tr><tr><td>P031</td></tr><tr><td>A03</td></tr><tr><td>SCS42_1</td></tr><tr><td>PPG29_0</td></tr><tr><td rowspan="5">5</td><td rowspan="5">7</td><td rowspan="5">9</td><td rowspan="5">12</td><td rowspan="5">15</td><td rowspan="5">19</td><td>TOT2_0</td></tr><tr><td>P032</td></tr><tr><td>A04</td></tr><tr><td>SCS43_1</td></tr><tr><td>PPG30_0</td></tr><tr><td rowspan="5">6</td><td rowspan="5">8</td><td rowspan="5">10</td><td rowspan="5">13</td><td rowspan="5">16</td><td rowspan="5">20</td><td>TOT3_0</td></tr><tr><td>RTO2_1</td></tr><tr><td>P033</td></tr><tr><td>A05</td></tr><tr><td>PPG31_0</td></tr><tr><td rowspan="3">6</td><td rowspan="3">8</td><td rowspan="3">10</td><td rowspan="3">13</td><td rowspan="3">16</td><td rowspan="3">20</td><td>ICU3_3</td></tr><tr><td>TIN4_0</td></tr><tr><td>RTO1_1</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SCK3_2</td></tr></table>	Pin no.						Pin Name	64	80	100	120	144	176	-	-	4	7	10	12	P025	WR1X	SOT4_1	PPG25_0	TIN2_0	-	-	-	-	-	13	P172	PPG38_1	-	4	5	8	11	14	P026	A00	SCK4_1	PPG26_0	TIN3_0	4	5	6	9	12	15	P027	A01	SCS40_1	PPG27_0	TOT0_0	-	-	-	-	-	16	RTO3_1	P173	-	-	7	10	13	17	PPG39_1	P030	A02	SCS41_1	PPG28_0	-	6	8	11	14	18	TOT1_0	P031	A03	SCS42_1	PPG29_0	5	7	9	12	15	19	TOT2_0	P032	A04	SCS43_1	PPG30_0	6	8	10	13	16	20	TOT3_0	RTO2_1	P033	A05	PPG31_0	6	8	10	13	16	20	ICU3_3	TIN4_0	RTO1_1							SCK3_2
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Page	Section	Change Results																				
40	■ I/O Circuit Type	Remarks for Type L in "I/O Circuit Types" modified as follows: (Error) - Open-drain I/O - Output 25mA (NOD) - TTL input (Correct) - Open-drain I/O - Output 25mA (Nch open-drain) - TTL input																				
40	■ I/O Circuit Type	Remarks for Type M in "I/O Circuit Types" modified as follows: (Error) - CMOS hysteresis input - Pull-up resistor 50kΩ (5V cont) (Correct) - CMOS hysteresis input - Pull-up resistor 50kΩ																				
121	■ Interrupt Vector Table	The following sentence deleted from Interrupt vector 64pins. *5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.																				
124	■ Interrupt Vector Table	The interrupt factor in Interrupt vector 80pin modified as follows: (Error) <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08_H</td><td rowspan="4">45^{*5}</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>-</td></tr><tr><td>-</td></tr></table> (Correct) <table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08_H</td><td rowspan="4">45</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>-</td></tr><tr><td>-</td></tr></table>	Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45 ^{*5}	Base timer 1 IRQ1	-	-	Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45	Base timer 1 IRQ1	-	-
Base timer 1 IRQ0	61	3D	ICR 45							308 _H	000F FF08 _H	45 ^{*5}										
Base timer 1 IRQ1																						
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-																						
Base timer 1 IRQ0	61	3D	ICR 45	308 _H	000F FF08 _H	45																
Base timer 1 IRQ1																						
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Revision	ECN	Orig. of Change	Submission Date	Description of Change
				(1) 12-bit A/D Converter Electrical Characteristics: Added the value of "Total error". Total error value Min – Typ – Max ± 12 LSB Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB Added the following description. Parameter : Power supply current I_AAVCC*3 *3: The power supply current described only current value on A/D converter. The total AVCC current value must be calculated the power supply current for A/D converter and D/A converter. Electrical Characteristics 7.D/A Converter: Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter. The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter. Electrical Characteristics 6.Flash memory: Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing $T_j < +105^\circ\text{C}$" Electrical Characteristics 7.D/A Converter: Corrected the following description. Parameter : Power supply current Symbol I_A Pin name AV_{CC} Symbol I_{AH} Pin name AV_{CC} ↓ Symbol I_A Pin name AVCC Symbol I_{AH} Pin name AVCC Example Characteristics Corrected the following description. Watch mode Ordering Information Corrected the following description. • ORDERING INFORMATION ↓ • ORDERING INFORMATION MB91F52xxB*1