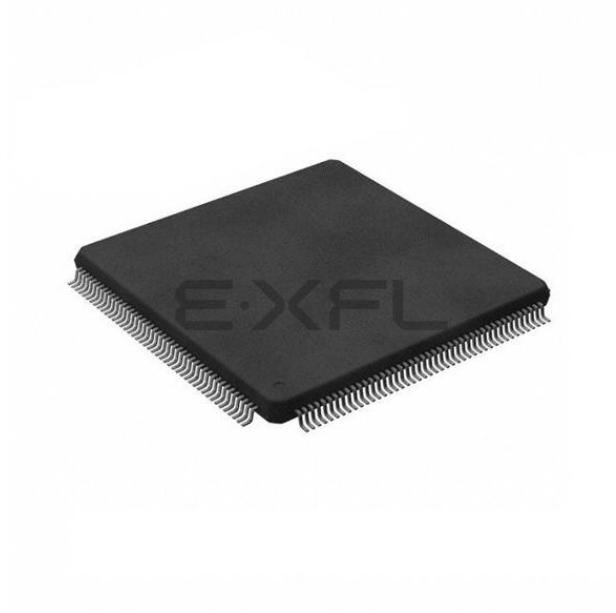
Infineon Technologies - MB91F526LSBPMC-GTK5E1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 48x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f526lsbpmc-gtk5e1

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	40	46	54	68	P070	-	A	General-purpose I/O port
						ICU0_2	-		Input capture ch.0 input (2)
26	33	41	47	55	69	P071	-	G	General-purpose I/O port
						SCK4_2	-		Multi-function serial ch.4 clock I/O (2)
						AN35	-		ADC analog 35 input
						ICU1_2	-		Input capture ch.1 input (2)
						MONCLK	-		Clock monitor output pin
27	34	42	48	56	70	P072	-	G	General-purpose I/O port
						SIN4_0	-		Multi-function serial ch.4 serial data input (0)
						AN34	-		ADC analog 34 input
						ICU2_2	-		Input capture ch.2 input (2)
						INT5_0	-		INT5 External interrupt input (0)
-	35 *3	43 *4	49	57	71	P073	-	D	General-purpose I/O port
						SOT4_0/ SDA4 *3, *4	-		Multi-function serial ch.4 serial data output (0)/I^{2}C bus serial data I/O
						AN33	-		ADC analog 33 input
						ICU3_2	-		Input capture ch.3 input (2)
-	-	-	-	-	72	P186	-	A	General-purpose I/O port
						PPG46_0	-		PPG ch.46 output (0)
-	-	-	-	-	73	P187	-	A	General-purpose I/O port
						PPG47_0	-		PPG ch.47 output (0)
-	-	-	50	58	74	P074	-	E	General-purpose I/O port
						SCK4_0/ SCL4	-		Multi-function serial ch.4 clock I/O (0)/ I^{2}C bus serial clock I/O
-	-	-	51	59	75	P075	-	F	General-purpose I/O port
						SIN3_0	-		Multi-function serial ch.3 serial data input (0)
						INT4_0	-		INT4 External interrupt input (0)
-	-	-	52	60	76	P076	-	E	General-purpose I/O port
						SOT3_0/ SDA3	-		Multi-function serial ch.3 serial data output (0)/I^{2}C bus serial data I/O
-	-	-	53	61	77	P077	-	E	General-purpose I/O port
						SCK3_0/ SCL3	-		Multi-function serial ch.3 clock I/O (0)/ I^{2}C bus serial clock I/O
-	-	44	54	62	78	P152	-	A	General-purpose I/O port
						SCS53_0	-		Serial chip select 53 output (0)
28	36	45	55	63	79	P153	-	G	General-purpose I/O port
						SCK5_0/ SCL5	-		Multi-function serial ch.5 clock I/O (0)/ I^{2}C bus serial clock I/O
						AN32	-		ADC analog 32 input
						FRCK1_1	-		Free-run timer 1 clock input (1)
						INT4_1	-		INT4 External interrupt input (1)

*1: There is a restriction of pin functions. See "Pin Name" of this table.
*2: not supported in 64pin
*3: not supported in 80pin
*4: not supported in 100pin
*5: not supported in 120pin
*6: not supported in 144pin
*7: not supported in 176pin
*8: For the I/O circuit types, see "I/O CIRCUIT TYPE".
*9: For switching, see "I/O Port" in HARDWARE MANUAL.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000F70_H$	RCRH0 [W] H,W XXXXXXXX	RCRL0 [W] B,H,W XXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/Down Counter 0
$000F74_H$	CCR0 [R/W] B,H 00000000 -0001000		—	CSR0 [R/W] B 00000000	
$000F78_H$ to $000F7C_H$	—	—	—	—	Reserved
$000F80_H$	RCRH1 [W] H,W XXXXXXXX	RCRL1 [W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/Down Counter 1
$000F84_H$	CCR1 [R/W] B,H 00000000 -0001000		—	CSR1 [R/W] B 00000000	
$000F88_H$	—	—	MSCH45 [R] B,H,W 00000000	MSCL45 [R/W] B,H,W ------00	Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45
$000F8C_H$	—	—	MSCH67 [R] B,H,W 00000000	MSCL67 [R/W] B,H,W ------00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67
$000F90_H$	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU
$000F94_H$	OCCP11 [R/W] W 00000000 00000000 00000000 00000000				
$000F98_H$	—	—	OCSH1011 [R/W] B,H,W ---0--00	OCSL1011 [R/W] B,H,W 0000--00	Output Compare 10,11 32-bit OCU
$000F9C_H$	—	—	—	OCLS1011 [R/W] B,H,W ----0000	OCU1011 Output level control register
$000FA0_H$	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 5 32-bit FRT
$000FA4_H$	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
$000FA8_H$	TCCSH5 [R/W]B,H,W 0-----00	TCCSL5 [R/W]B,H,W -1-00000	—	—	
$000FAC_H$ to $000FCC_H$	—	—	—	—	Reserved

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Clock calibration unit (sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1,*4
A/D converter 0/1/7/10/11/14/15/16/17/22/27/28/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit Free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35
32-bit ICU6 (fetching/measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching/measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching/measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching/measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching/measurement) A/D converter 32/34/35/37/38/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU7/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
-	60	3C	ICR44	$30C_H$	$000FFF0C_H$	-*6
- -	61	3D	ICR45	308_H	$000FFF08_H$	-
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS™*8)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Used with the INT instruction	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and I^2C reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

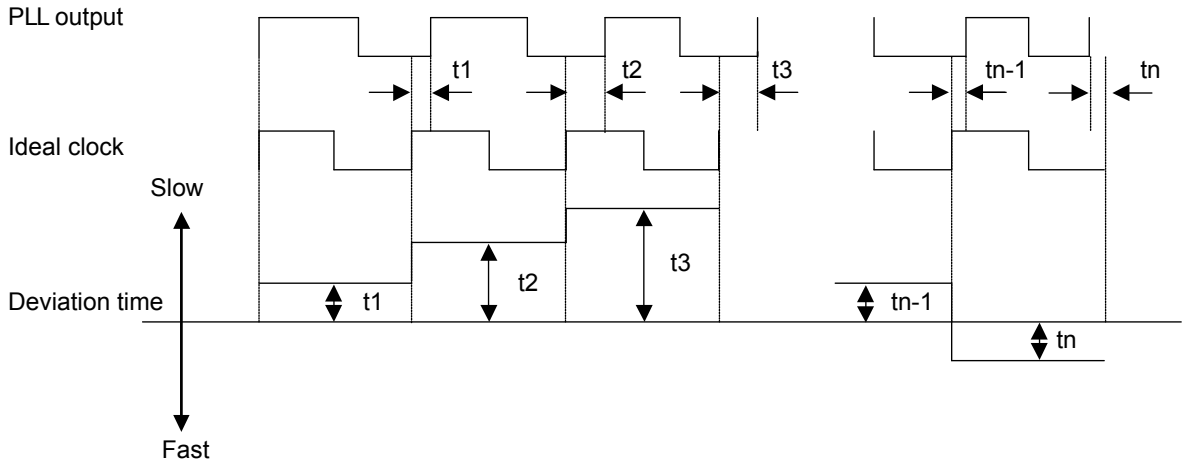
*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: REALOS is a trademark of Cypress.

• CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



(3) Power-on Conditions

(3-1) [MB9152xxxB/MB9152xxxC/MB9152xxxD]

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Power off time	t_{OFF}	V_{CC}	–	50	–	–	ms	*2
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2V to 2.376V	–	–	4	mV/µs	*3
C pin voltage at Power-on	–	C	–	–	–	60	mV	*4

*1: This spec is at 4mV/µs of power ramp rate. If the power ramp rate is faster than 4mV/µs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Vcc must be held below 0.2V for a minimum period of t_{OFF}.

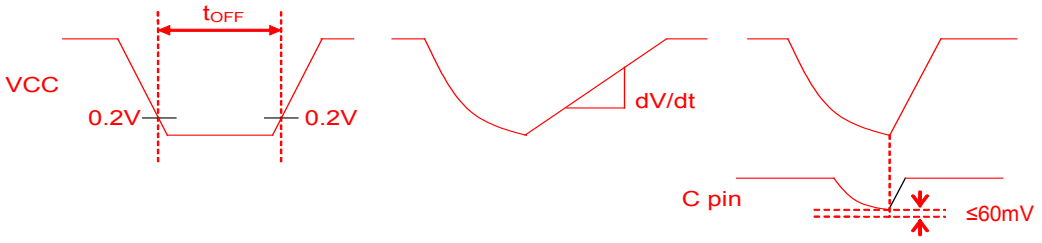
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when VCC is turned on again.

Note:

When using MB91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use MB91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate, C pin voltage at Power-on

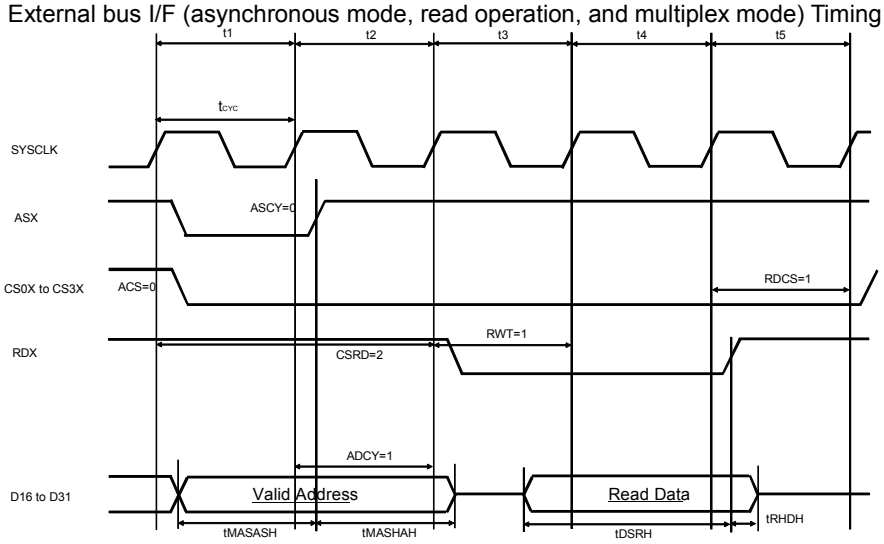


Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	-	ns	WWT=0 *2
SYSCLK↑→ data output time	t_{CHDV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t_{CHDX}		-	18	ns	Set WRCS to 1 or more.
SYSCLK↑→ address output time	t_{CHMAV}	SYSCLK D16 to D31	0.5	18	ns	
SYSCLK↑→ address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: □Set CSWR and CSRD to 2 or more. □ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

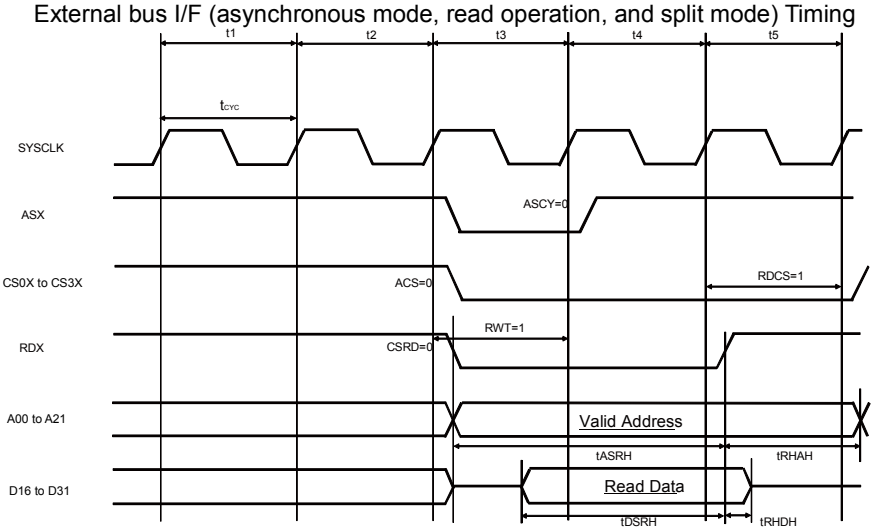
*1: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



External bus I/F (asynchronous mode, read operation, and split mode) Timing



A/D Converter

(1) 12-bit A/D Converter Electrical Characteristics

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±12	LSB	
Linearity error	-	-	-	-	± 4.0	LSB	
Differential linearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN47	AVRL-11.5LSB	-	AVRL+12.5LSB	V	1LSB= (V_{FST}-V_{OT})/4094
Full-scale transition voltage	V_{FST}	AN0 to AN47	AVRH-13.5LSB	-	AVRH+10.5LSB	V	
Sampling time	t_{SMP}	-	0.7	-	-	µs	*1
Compare time	t_{CMP}	-	0.7	-	-	µs	*1
A/D conversion time	t_{CNV}	-	1.4	-	-	µs	*1
Analog port input current	I_{AIN}	AN0 to AN47	-1.0	-	+1.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN47	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH	3.0	-	5.5	V	
	AVRL	AVSS/AVRL	-	0.0	-	V	
Power supply current	I_A	AVCC*3	-	0.47	0.63	mA	Per unit T_A: +105°C
			-	0.47	0.7	mA	Per unit T_A: +125°C
	I_{AH}		-	-	2.5	µA	*2
	I_R	AVRH	-	1	1.96	mA	Per unit
	I_{RH}		-	-	1.6	µA	*2
Variation between channels	-	AN0 to AN47	-	-	4	LSB	

*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

*3: The power supply current described only current value on A/D converter.
The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.

(Note) Please use the clock of 0.5MHz-20MHz for the output clock of A/D converter to guarantee accuracy.

D/A converter

(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	–	–	–	8	bit	
Differential linearity error	-	-	–	–	–	± 3.0	LSB	
Conversion time	-	-	–	0.47	0.58	0.69	µs	C_L=20
			–	2.37	2.90	3.43	µs	C_L=100
Output impedance	Ro	DA0, DA1	–	3.1	3.8	4.5	kΩ	
Power supply current *1	IA	AVCC	–	–	475	580	µA	Each channel
	IAH	AVCC	–	–	–	7.5	µA	When powerdown Each channel

*1: The power supply current described only current value on D/A converter.
The total AVcc current value must be calculated the power supply current for D/A converter and A/D converter.

14. Ordering Information MB91F52xxxC[*1]

Part number	Sub clock	CSV Initial value	LVD Initial value	Package[*2]
MB91F526LWCPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LYCPMC			OFF	
MB91F526LJCPMC		OFF	ON	
MB91F526LLCPMC			OFF	
MB91F525LWCPMC		ON	ON	
MB91F525LYCPMC			OFF	
MB91F525LJCPMC		OFF	ON	
MB91F525LLCPMC			OFF	
MB91F524LWCPMC		ON	ON	
MB91F524LYCPMC			OFF	
MB91F524LJCPMC		OFF	ON	
MB91F524LLCPMC			OFF	
MB91F523LWCPMC		ON	ON	
MB91F523LYCPMC			OFF	
MB91F523LJCPMC		OFF	ON	
MB91F523LLCPMC			OFF	
MB91F522LWCPMC		ON	ON	
MB91F522LYCPMC			OFF	
MB91F522LJCPMC		OFF	ON	
MB91F522LLCPMC			OFF	
MB91F526LSCPMC	None	ON	ON	
MB91F526LUCPMC			OFF	
MB91F526LHCPMC		OFF	ON	
MB91F526LKCPMC			OFF	
MB91F525LSCPMC		ON	ON	
MB91F525LUCPMC			OFF	
MB91F525LHCPMC		OFF	ON	
MB91F525LKCPMC			OFF	
MB91F524LSCPMC		ON	ON	
MB91F524LUCPMC			OFF	
MB91F524LHCPMC		OFF	ON	
MB91F524LKCPMC			OFF	
MB91F523LSCPMC		ON	ON	
MB91F523LUCPMC			OFF	
MB91F523LHCPMC		OFF	ON	
MB91F523LKCPMC			OFF	
MB91F522LSCPMC		ON	ON	
MB91F522LUCPMC			OFF	
MB91F522LHCPMC		OFF	ON	
MB91F522LKCPMC			OFF	

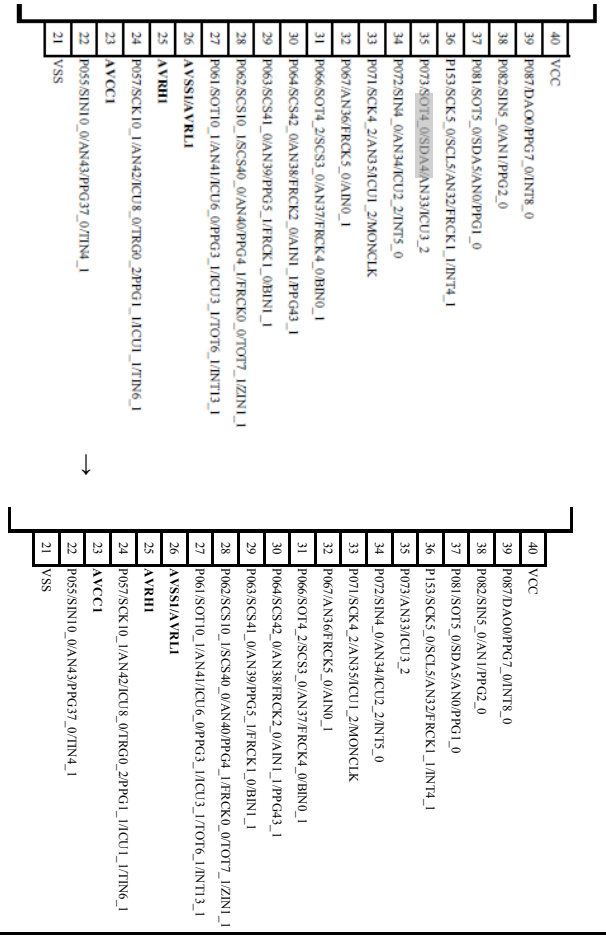
Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526FWCPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FYCPMC			OFF	
MB91F526FJCPMC		OFF	ON	
MB91F526FLCPMC			OFF	
MB91F525FWCPMC		ON	ON	
MB91F525FYCPMC			OFF	
MB91F525FJCPMC		OFF	ON	
MB91F525FLCPMC			OFF	
MB91F524FWCPMC		ON	ON	
MB91F524FYCPMC			OFF	
MB91F524FJCPMC		OFF	ON	
MB91F524FLCPMC			OFF	
MB91F523FWCPMC		ON	ON	
MB91F523FYCPMC			OFF	
MB91F523FJCPMC		OFF	ON	
MB91F523FLCPMC			OFF	
MB91F522FWCPMC		ON	ON	
MB91F522FYCPMC			OFF	
MB91F522FJCPMC		OFF	ON	
MB91F522FLCPMC			OFF	
MB91F526FSCPMC	None	ON	ON	
MB91F526FUCPMC			OFF	
MB91F526FHCPMC		OFF	ON	
MB91F526FKCPMC			OFF	
MB91F525FSCPMC		ON	ON	
MB91F525FUCPMC			OFF	
MB91F525FHCPMC		OFF	ON	
MB91F525FKCPMC			OFF	
MB91F524FSCPMC		ON	ON	
MB91F524FUCPMC			OFF	
MB91F524FHCPMC		OFF	ON	
MB91F524FKCPMC			OFF	
MB91F523FSCPMC		ON	ON	
MB91F523FUCPMC			OFF	
MB91F523FHCPMC		OFF	ON	
MB91F523FKCPMC			OFF	
MB91F522FSCPMC		ON	ON	
MB91F522FUCPMC			OFF	
MB91F522FHCPMC		OFF	ON	
MB91F522FKCPMC			OFF	

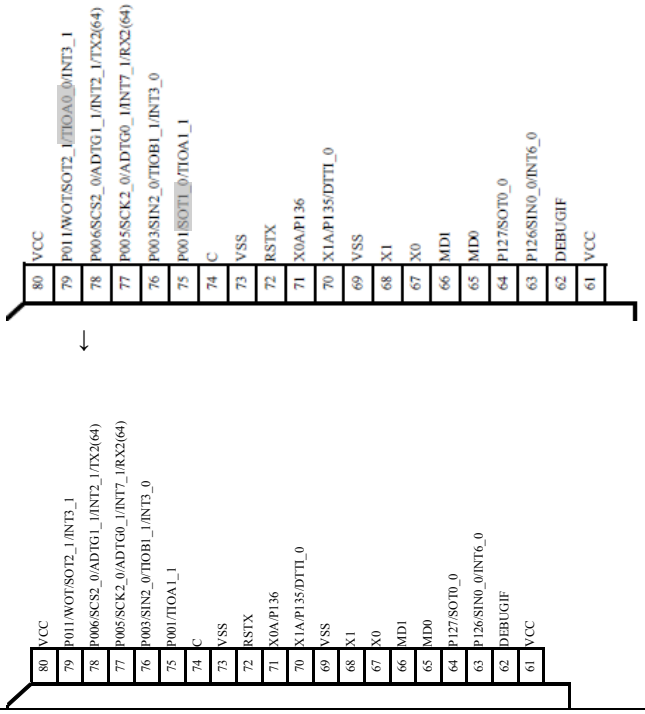
15. Ordering Information MB91F52xxxD

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWDPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LJDPMC		OFF	ON	
MB91F525LWDPMC		ON	ON	
MB91F525LJDPMC		OFF	ON	
MB91F524LWDPMC		ON	ON	
MB91F524LJDPMC		OFF	ON	
MB91F523LWDPMC		ON	ON	
MB91F523LJDPMC		OFF	ON	
MB91F522LWDPMC		ON	ON	
MB91F522LJDPMC		OFF	ON	
MB91F526LSDPMC	None	ON	ON	
MB91F526LHDPMC		OFF	ON	
MB91F525LSDPMC		ON	ON	
MB91F525LHDPMC		OFF	ON	
MB91F524LSDPMC		ON	ON	
MB91F524LHDPMC		OFF	ON	
MB91F523LSDPMC		ON	ON	
MB91F523LHDPMC		OFF	ON	
MB91F522LSDPMC		ON	ON	
MB91F522LHDPMC		OFF	ON	
MB91F526KWDPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJDPMC		OFF	ON	
MB91F525KWDPMC		ON	ON	
MB91F525KJDPMC		OFF	ON	
MB91F524KWDPMC		ON	ON	
MB91F524KJDPMC		OFF	ON	
MB91F523KWDPMC		ON	ON	
MB91F523KJDPMC		OFF	ON	
MB91F522KWDPMC		ON	ON	
MB91F522KJDPMC		OFF	ON	
MB91F526KSDPMC	None	ON	ON	
MB91F526KHDPMC		OFF	ON	
MB91F525KSDPMC		ON	ON	
MB91F525KHDPMC		OFF	ON	
MB91F524KSDPMC		ON	ON	
MB91F524KHDPMC		OFF	ON	
MB91F523KSDPMC		ON	ON	
MB91F523KHDPMC		OFF	ON	
MB91F522KSDPMC		ON	ON	
MB91F522KHDPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526BWDPMC1	Yes	ON	ON	LQD・64 pin, Plastic
MB91F526BJDPMC1		OFF	ON	
MB91F525BWDPMC1		ON	ON	
MB91F525BJDPMC1		OFF	ON	
MB91F524BWDPMC1		ON	ON	
MB91F524BJDPMC1		OFF	ON	
MB91F523BWDPMC1		ON	ON	
MB91F523BJDPMC1		OFF	ON	
MB91F522BWDPMC1		ON	ON	
MB91F522BJDPMC1		OFF	ON	
MB91F526BSDPMC1	None	ON	ON	
MB91F526BHDPMC1		OFF	ON	
MB91F525BSDPMC1		ON	ON	
MB91F525BHDPMC1		OFF	ON	
MB91F524BSDPMC1		ON	ON	
MB91F524BHDPMC1		OFF	ON	
MB91F523BSDPMC1		ON	ON	
MB91F523BHDPMC1		OFF	ON	
MB91F522BSDPMC1		ON	ON	
MB91F522BHDPMC1		OFF	ON	

*: For details of the package, see "■ PACKAGE DIMENSIONS ".

Page	Section	Change Results
14	■Pin Assignment MB91F52xD	- Bottom 

Page	Section	Change Results
14	■Pin Assignment MB91F52xD	- Top  ↓
14	■Pin Assignment MB91F52xD	The following note added on the bottom left of Figure. * In a single clock product, pin 71 and pin 72 are the general-purpose ports.

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>33</td><td>■PIN Description</td><td>
A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94</td><td rowspan="5">111</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75</td><td rowspan="4">95</td><td rowspan="4">112</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17</td></tr>
<tr><td>SOT1_0</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94 *1</td><td rowspan="5">111 *1</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16 *4, *5</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1 *4</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75 *1</td><td rowspan="4">95 *1</td><td rowspan="4">112 *1</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17 *3, *4, *5</td></tr>
<tr><td>SOT1_0 *3</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>
</td></tr>
</table>

Page	Section	Change Results
Rev *C		
2	Features Peripheral Functions	The following sentence modified in I2C as following: (Error) < I2C > 2 channels ch.3 , ch.4 Standard mode/high-speed mode supported. Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported (Correct) < I2C > 2 channels ch.3 , ch.4 Standard mode/fast mode supported. Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported
5,6,7,8,9 ,10	1. Product Lineup	The following *2 added as follows: (Error) Power supply | 2.7 V to 5.5 V (Correct) Power supply | 2.7 V to 5.5 V *2
5,6,7,8,9 ,10	1. Product Lineup	The following sentence added as follows: (Correct) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
8, 9, 10,	1. Product Lineup	The following sentence modified in the bottom of Product lineup comparison table as following: (Error) *1: Only channel 3 and channel 4 support the I2C (high-speed mode/standard mode). (Correct) *1: Only channel 3 and channel 4 support the I2C (fast mode/standard mode).
11	1. Product Lineup	Added silicon version E

Page	Section	Change Results
142,143	11. Electrical Characteristics Recommended operating conditions	The following sentence should be modified as follows: (Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. (Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
146	11. Electrical Characteristics DC Characteristics	Pin name of R_{UP3} should be modified as follows: (Error) Port pin other than P035,041,093,122 (Correct) Port pin other than P035,041,073,074,076,077,093,122
187	11. Electrical Characteristics (8) Low voltage detection (External low-voltage detection)	Note of Detection voltage should be added as follows: (Correct) Detection voltage *3 *3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V). Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.