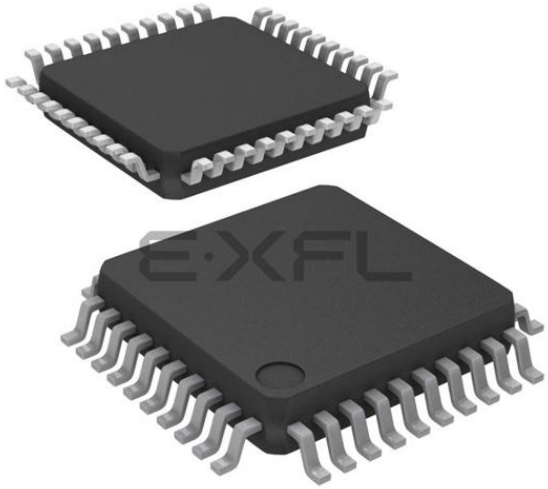

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 740 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | SIO, UART/USART |
| Peripherals | WDT |
| Number of I/O | 25 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | QzROM |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 6x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m37544g2agp-u0 |

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# 7544 Group (QzROM version)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0108-0103
Rev.1.03
Mar 31, 2009

## DESCRIPTION

The 7544 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7544 Group has a serial interface, 8-bit timers, a 16-bit timer, and an A/D converter, and is useful for control of home electric appliances and office automation equipment.

## FEATURES

- Basic machine-language instructions ..... 71
- The minimum instruction execution time ..... 0.25 µs
  (at 8 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size ROM ..... 8 K bytes
  RAM ..... 256 bytes
- Programmable I/O ports ..... 25
- Interrupts ..... 12 sources, 12 vectors
- Timers ..... 8-bit × 2
  ..... 16-bit × 1
- Serial interface ..... 8-bit × 1 (UART or Clock-synchronized)
- A/D converter ..... 8-bit × 6 channels
- Clock generating circuit ..... Built-in type
  (low-power dissipation by an on-chip oscillator enabled)
  (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer ..... 16-bit × 1
- Power source voltage
  XIN oscillation frequency at ceramic/quartz-crystal oscillation, in double-speed mode
  At 8 MHz ..... 4.5 to 5.5 V
  At 4 MHz ..... 4.0 to 5.5 V
  At 2 MHz ..... 2.4 to 5.5 V
  At 1 MHz ..... 2.2 to 5.5 V
  XIN oscillation frequency at ceramic/quartz-crystal oscillation, in high-speed mode
  At 8 MHz ..... 4.0 to 5.5 V
  At 4 MHz ..... 2.4 to 5.5 V
  At 2 MHz ..... 2.2 to 5.5 V
  XIN oscillation frequency at RC oscillation
  At 4 MHz ..... 4.0 to 5.5 V
  At 2 MHz ..... 2.4 to 5.5 V
  At 1 MHz ..... 2.2 to 5.5 V
  XIN oscillation frequency at on-chip oscillator ..... 1.8 to 5.5 V
- Power dissipation ..... 22.5mW(standard)
- Operating temperature range ..... –20 to 85 °C

## APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, etc.

## FUNCTIONAL BLOCK

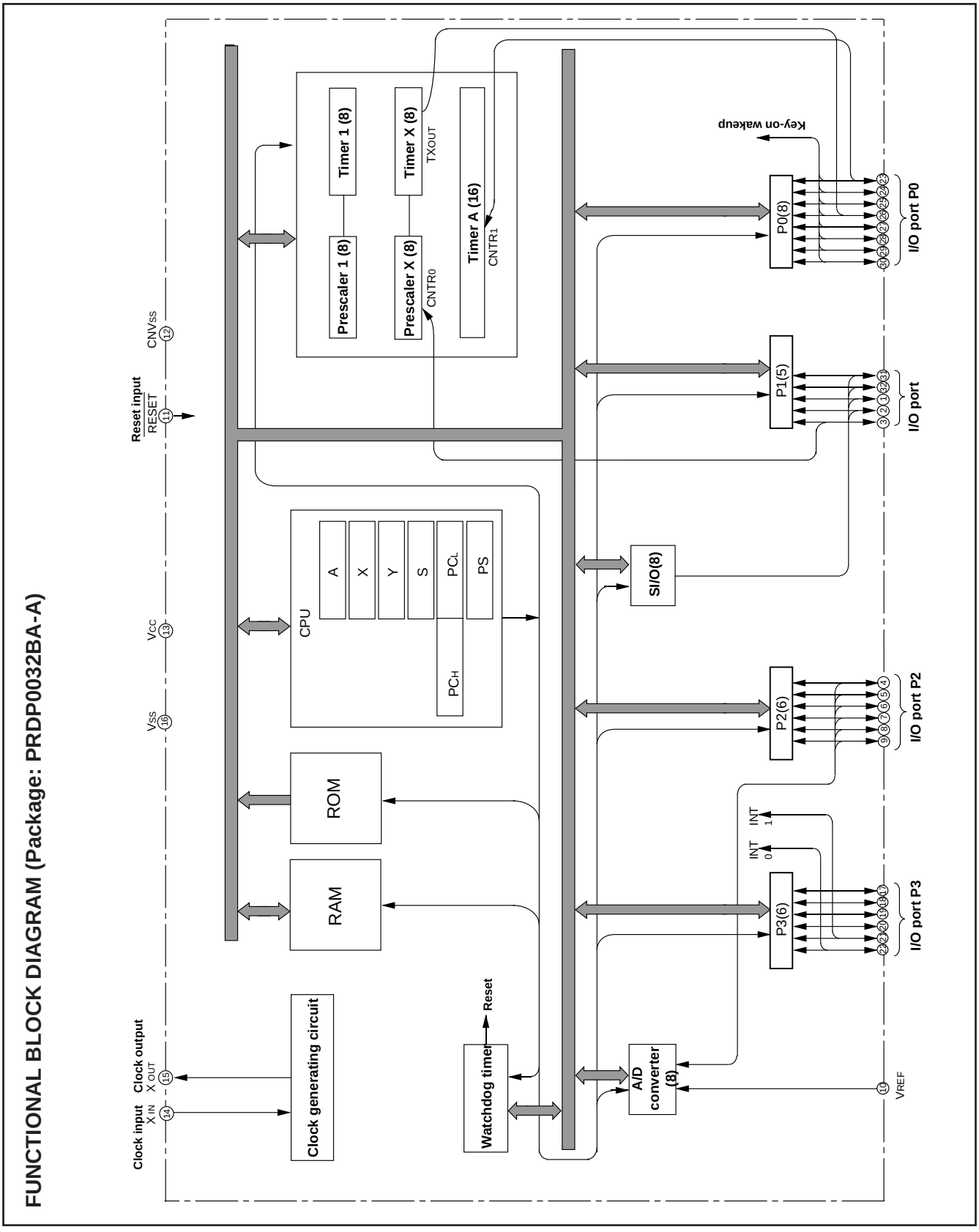



**Fig. 4 Functional block diagram (PRDP0032BA-A package)**

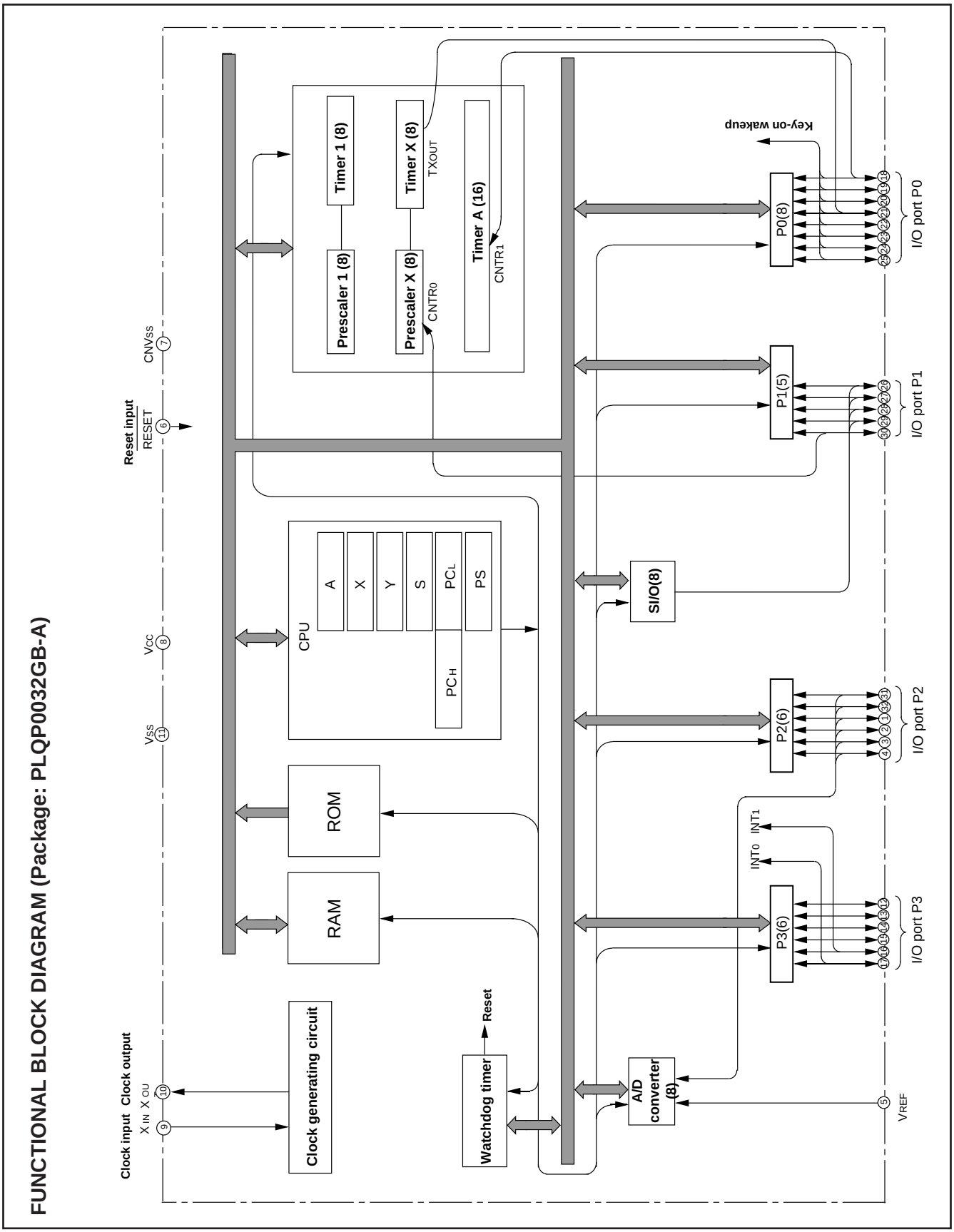



**Fig. 5 Functional block diagram (PLQP0032GB-A package)**

## PIN DESCRIPTION

**Table 2 Pin description**

| Pin | Name | Function | Function expect a port function |
|---|---|---|---|
| Vcc, Vss | Power source | •Apply voltage of 1.8 to 5.5 V to Vcc, and 0 V to Vss. | |
| VREF | Analog reference voltage | •Reference voltage input pin for A/D converter | |
| CNVss | CNVss | •Chip operating mode control pin, which is always connected to Vss. | |
| $\overline{\text{RESET}}$ | Reset input | •Reset input pin for active “L” | |
| XIN | Clock input | •Input and output pins for main clock generating circuit<br>•Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins.<br>•For using RC oscillator, short between the XIN and XOUT pins, and connect the capacitor and resistor.<br>•If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.<br>• When the on-chip oscillator is selected as the main clock, connect XIN pin to VCC and leave XOUT open. | |
| XOUT | Clock output | | |
| P00/CNTR1<br>P01<br>P02<br>P03/TXOUT<br>P04–P07 | I/O port P0 | •8-bit I/O port.<br>•I/O direction register allows each pin to be individually programmed as either input or output.<br>•CMOS compatible input level<br>•CMOS 3-state output structure<br>•P0 can output a large current for driving LED.<br>•Whether a built-in pull-up resistor is to be used or not can be determined by program. | • Key-input (key-on wake up interrupt input) pins<br>• Timer X and timer A function pin |
| P10/RxD<br>P11/TxD | I/O port P1 | •5-bit I/O port<br>•I/O direction register allows each pin to be individually programmed as either input or output.<br>•CMOS compatible input level<br>•CMOS 3-state output structure<br>•CMOS/TTL level can be switched for P10 and P12 | • Serial I/O function pin |
| P12/SCLK<br>P13/$\overline{\text{SRDY}}$ | | | |
| P14/CNTR0 | | | • Timer X function pin |
| P20/AN0–P25/AN5 | I/O port P2 | •6-bit I/O port having almost the same function as P0<br>•CMOS compatible input level<br>•CMOS 3-state output structure | • Input pins for A/D converter |
| P30–P33 | I/O port P3 | •6-bit I/O port<br>•I/O direction register allows each pin to be individually programmed as either input or output.<br>•CMOS compatible input level (CMOS/TTL level can be switched for P34 and P37).<br>•CMOS 3-state output structure<br>•P3 can output a large current for driving LED. | |
| P34/INT1<br>P37/INT0 | | •Whether a built-in pull-up resistor is to be used or not can be determined by program. | • Interrupt input pins |

## I/O Ports

**[Direction registers] PiD**

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.

When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

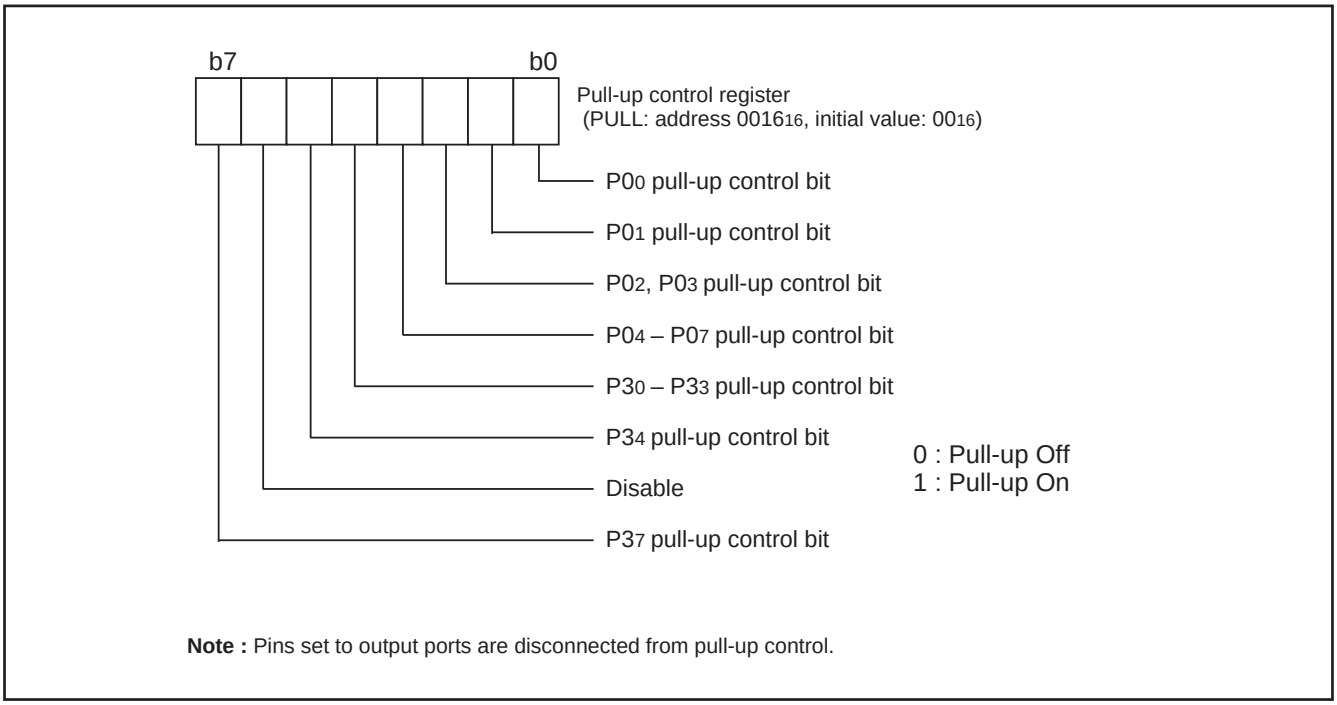
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

**[Pull-up control register] PULL**

By setting the pull-up control register (address $0016_{16}$), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

**[Port P1P3 control register] P1P3C**

By setting the port P1P3 control register (address $0017_{16}$), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P3_4$, and $P3_7$ by program.




**Note :** Pins set to output ports are disconnected from pull-up control.

**Fig. 13 Structure of pull-up control register**

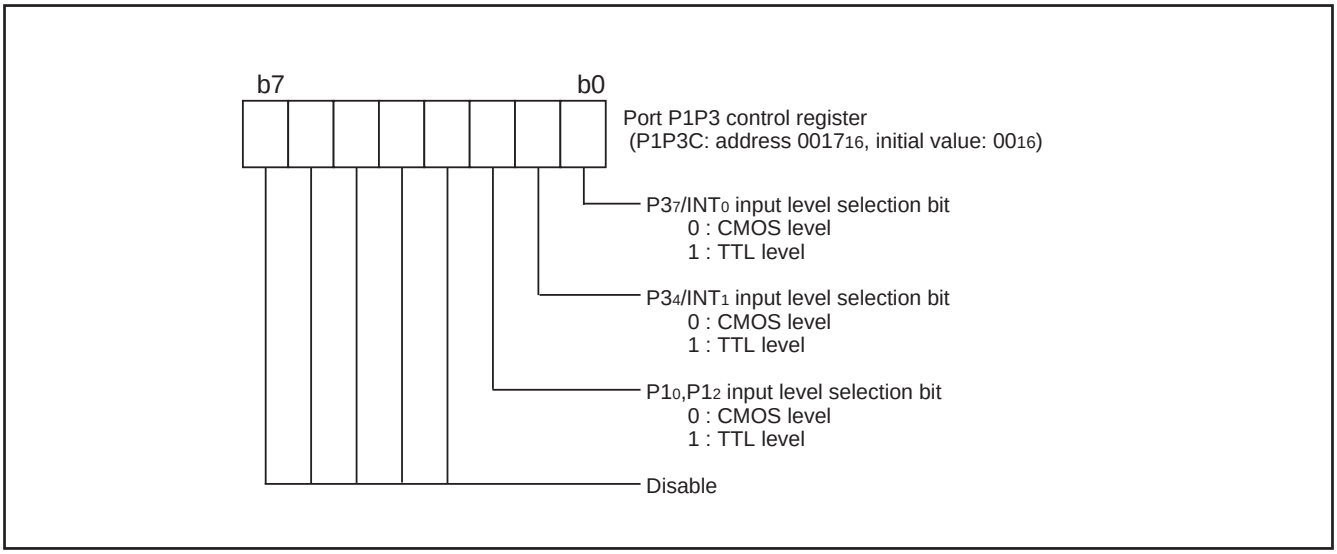


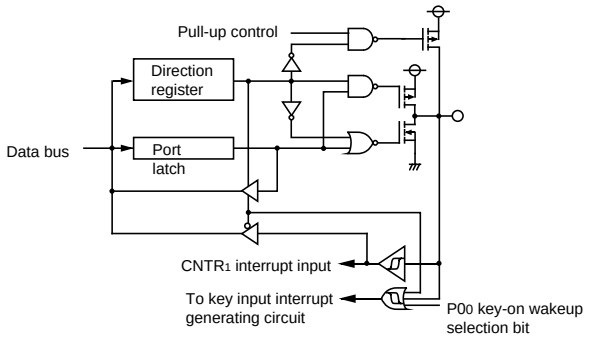

**Fig. 14 Structure of port P1P3 control register**

**Table 6 I/O port function table**

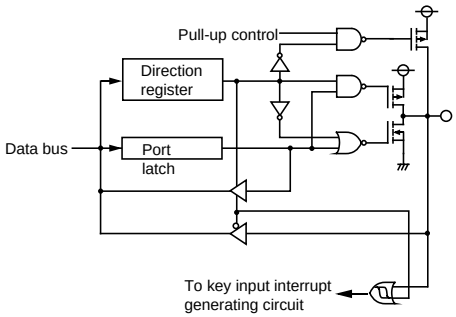
| Pin | Name | Input/output | I/O format | Non-port function | Related SFRs | Diagram No. |
|---|---|---|---|---|---|---|
| $P0_0$/CNTR$_1$<br>$P0_1$<br>$P0_2$<br>$P0_3$/TX$_{OUT}$<br>$P0_4$–$P0_7$ | I/O port P0 | I/O individual bits | •CMOS compatible input level<br>•CMOS 3-state output (**Note**) | Key input interrupt<br>Timer X function output<br>Timer A function input | Pull-up control register<br>Timer X mode register<br>Timer A mode register<br>Interrupt edge selection register | (1)<br>(2)<br>(3) |
| $P1_0$/RxD<br>$P1_1$/TxD<br>$P1_2$/S$_{CLK}$<br>$P1_3$/$\overline{S_{RDY}}$ | I/O port P1 | | | Serial I/O function input/output | Serial I/O control register<br>Port P1,P3 control register | (4)<br>(5)<br>(6)<br>(7) |
| $P1_4$/CNTR$_0$ | | | | Timer X function input/output | Timer X mode register | (8) |
| $P2_0$/AN$_0$–<br>$P2_5$/AN$_5$ | I/O port P2 | | | A/D conversion input | A/D control register | (9) |
| $P3_0$–$P3_3$ | I/O port P3 | | | | Pull-up control register | (10) |
| $P3_4$/INT$_1$<br>$P3_7$/INT$_0$ | | | | External interrupt input | Interrupt edge selection register<br>Pull-up control register<br>Port P1,P3 control register | (11) |

**Note :** Ports $P1_0$, $P1_2$, $P3_4$, and $P3_7$ are CMOS/TTL level.

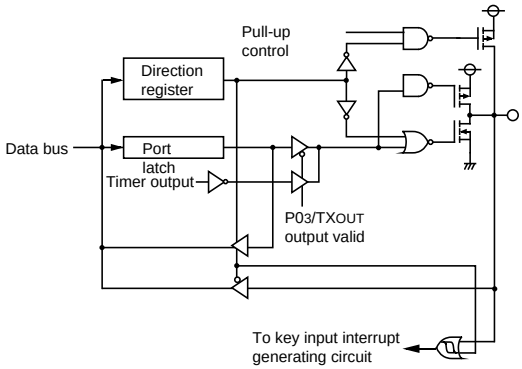
(1)Port P0$_0$



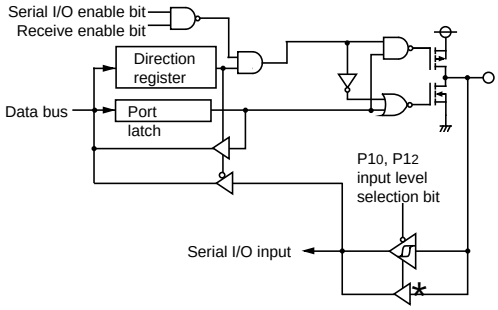

(2)Ports P0$_1$,P0$_2$,P0$_4$–P0$_7$



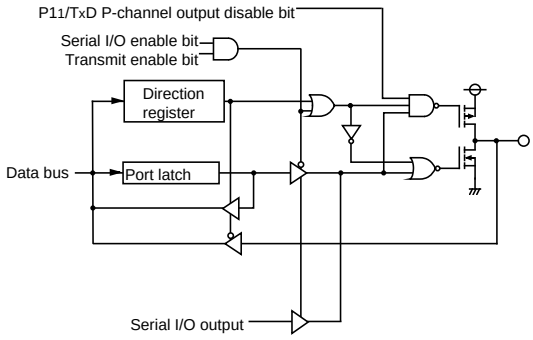

(3)Port P0$_3$



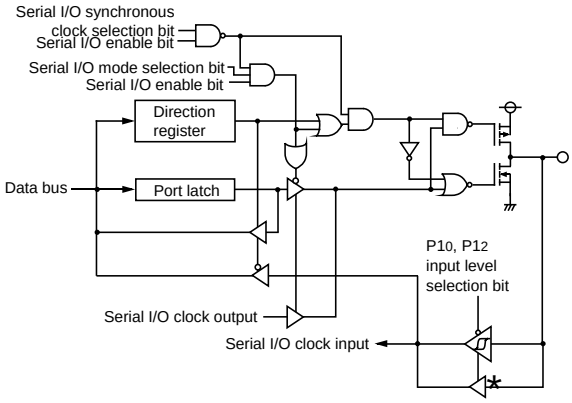

(4)Port P1$_0$




(5)Port P1$_1$




(6)Port P1$_2$




* P10, P12, P34, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

**Fig. 15 Block diagram of ports (1)**

## Timers

The 7544 Group has 3 timers: timer 1, timer A and timer X.
The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.
All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

## ●Timer 1

Timer 1 is an 8-bit timer and counts the prescaler output.
When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".
Prescaler 1 is an 8-bit prescaler and counts the signal selected by the timer 1 count source selection bit.
Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows. The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.
When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.
When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.
When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.
Timer 1 always operates in the timer mode.
Prescaler 1 counts the signal selected by the timer 1 count source selection bit. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "$00_{16}$", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is 1/(n+1) provided that the value of Prescaler 1 is n.
The contents of Timer 1 is decremented by 1 each time the underflow signal of Prescaler 1 is input. When the contents of Timer 1 reach "$00_{16}$", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is 1/(m+1) provided that the value of Timer 1 is m. Accordingly, the division ratio of Prescaler 1 and Timer 1 is 1/((n+1)×(m+1)) provided that the value of Prescaler 1 is n and the value of Timer 1 is m.
Timer 1 cannot stop counting by software.

## ●Timer A

Timer A is a 16-bit timer and counts the signal selected by the timer A count source selection bit. When Timer A underflows, the timer A interrupt request bit is set to "1".
Timer A consists of the low-order of Timer A (TAL) and the high-order of Timer A (TAH).
Timer A has the timer A latch to retain the reload value. The value of timer A latch is set to Timer A at the timing shown below.
• When Timer A underflows.
• When an active edge is input from $CNTR_1$ pin (valid only when period measurement mode and pulse width HL continuously measurement mode).
When writing to both the low-order of Timer A (TAL) and the high-order of Timer A (TAH) is executed, the value is written to both the timer A latch and Timer A.
When reading from the low-order of Timer A (TAL) and the high-order of Timer A (TAH) is executed, the following values are read out according to the operating mode.
• In timer mode, event counter mode:
The count value of Timer A is read out.
• In period measurement mode, pulse width HL continuously measurement mode:
The measured value is read out.

Be sure to write to/read out the low-order of Timer A (TAL) and the high-order of Timer A (TAH) in the following order;
Read
Read the high-order of Timer A (TAH) first, and the low-order of Timer A (TAL) next and be sure to read out both TAH and TAL.
Write
Write to the low-order of Timer A (TAL) first, and the high-order of Timer A (TAH) next and be sure to write to both TAL and TAH.

Timer A can be selected in one of 4 operating modes by setting the timer A mode register.

**(1) Timer mode**

Timer A counts the selected by the timer A count source selection bit. Each time the count clock is input, the contents of Timer A is decremented by 1. When the contents of Timer A reach "$0000_{16}$", an underflow occurs at the next count clock, and the timer A latch is reloaded into Timer A. The division ratio of Timer A is 1/(n+1) provided that the value of Timer A is n.

**(2) Period measurement mode**

In the period measurement mode, the pulse period input from the $P0_0$/$CNTR_1$ pin is measured.
$CNTR_1$ interrupt request is generated at rising/falling edge of $CNTR_1$ pin input signal. Simultaneously, the value in the timer A latch is reloaded in Timer A and count continues. The active edge of $CNTR_1$ pin input signal can be selected from rising or falling by the $CNTR_1$ active edge switch bit .The count value when trigger input from $CNTR_1$ pin is accepted is retained until Timer A is read once.

**(2) Asynchronous Serial I/O (UART) Mode**

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

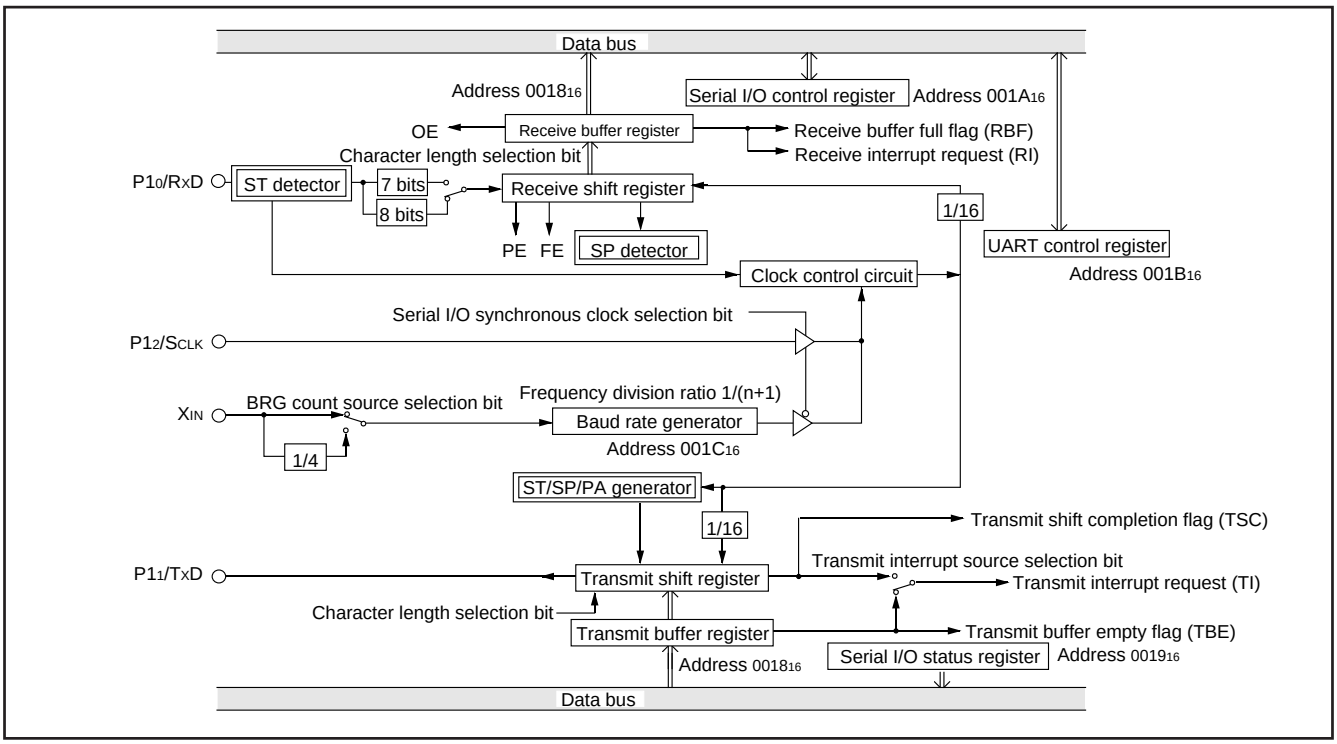
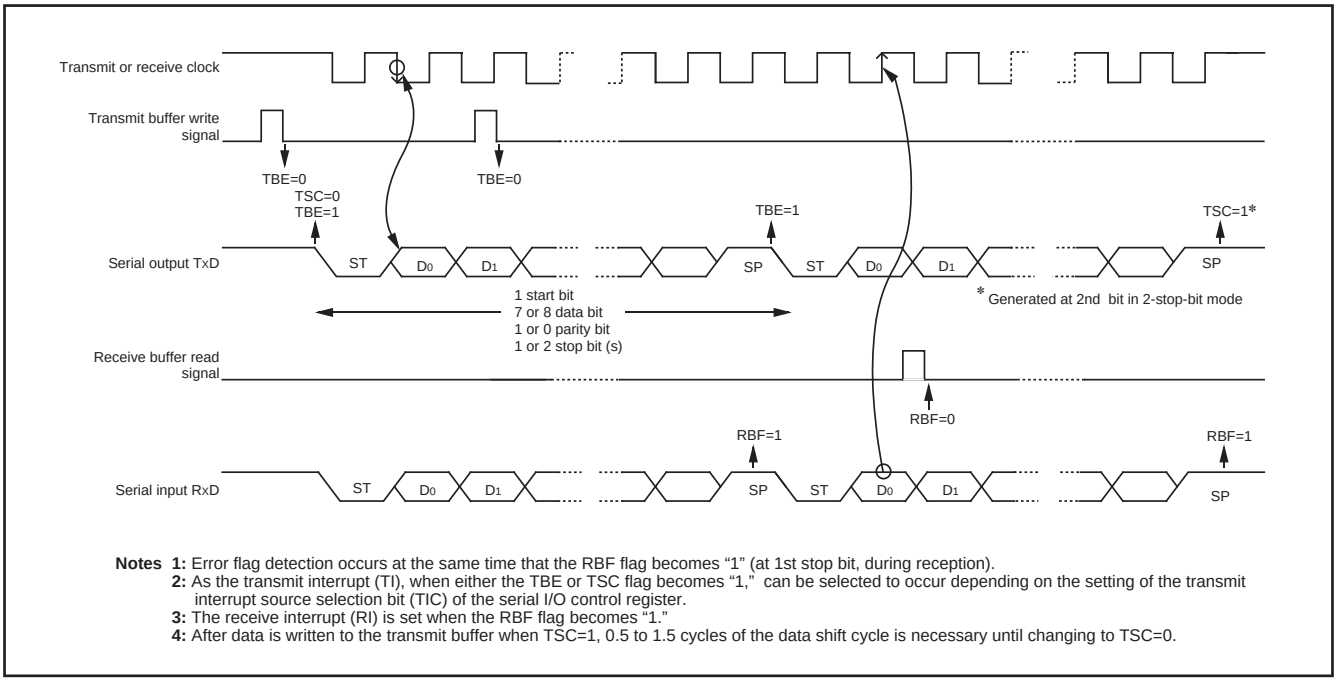



**Fig. 31 Block diagram of UART serial I/O**




**Notes 1:** Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
**2:** As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
**3:** The receive interrupt (RI) is set when the RBF flag becomes “1.”
**4:** After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

**Fig. 32 Operation of UART serial I/O function**

## A/D Converter

The functional blocks of the A/D converter are described below.

**[A/D conversion register] AD**

The A/D conversion register is a read-only register that stores the result of A/D conversion. Do not read out this register during an A/D conversion.

**[A/D control register] ADCON**

The A/D control register controls the A/D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at “0” during A/D conversion, and changes to “1” at completion of A/D conversion.
A/D conversion is started by setting this bit to “0”.

**[Comparison voltage generator]**

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

**[Channel selector]**

The channel selector selects one of ports P25/AN5 to P20/AN0, and inputs the voltage to the comparator.

**[Comparator and control circuit]**

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A/D conversion register. When A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”. Because the comparator is constructed linked to a capacitor, set f(XIN) to 500 kHz or more during A/D conversion.

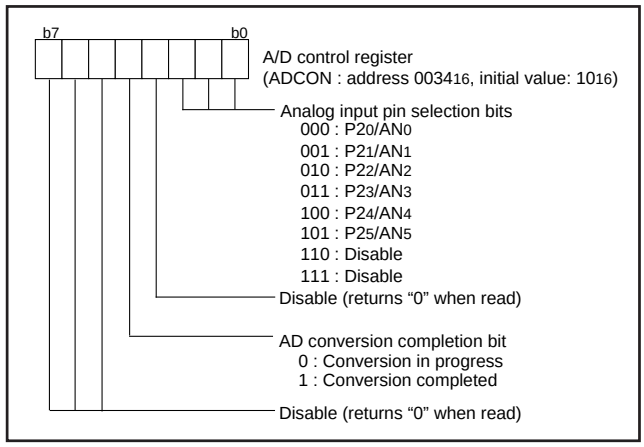



**Fig. 34 Structure of A/D control register**

**■ Notes on A/D converter**

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(XIN) is 500 kHz or more during A/D conversion.
As for AD translation accuracy, on the following operating conditions, accuracy may become low.

(1) Since the analog circuit inside a microcomputer becomes sensitive to noise when VREF voltage is set up lower than Vcc voltage, accuracy may become low rather than the case where VREF voltage and Vcc voltage are set up to the same value..

(2) When VREF voltage is lower than [ 3.0 V ], the accuracy at the low temperature may become extremely low compared with that at room temperature. When the system would be used at low temperature, the use at VREF=3.0 V or more is recommended.

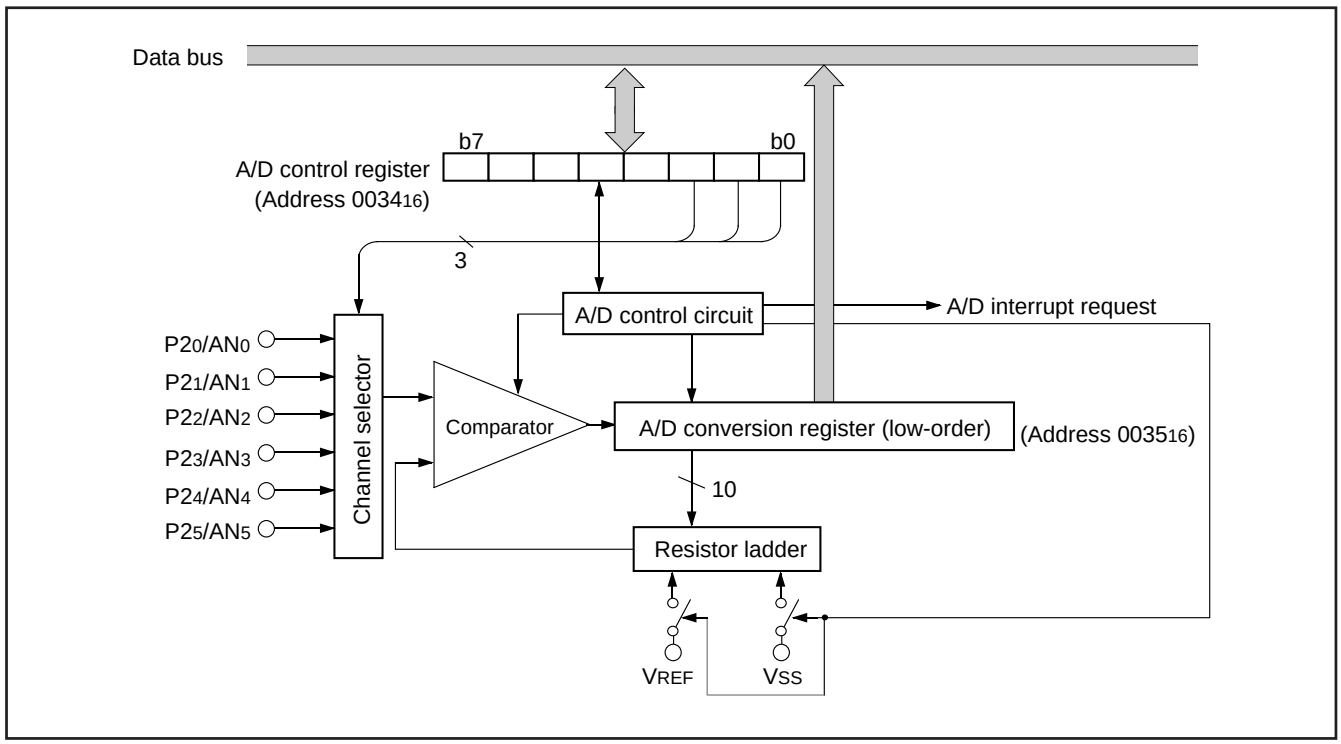



**Fig. 35 Block diagram of A/D converter**

## Reset Circuit

The 7544 group starts operation by the on-chip oscillator after system is released from reset.
Accordingly, when the rising of power supply voltage passes 2.2V, set the reset input voltage to become below 0.2Vcc (0.44V).
Moreover, switch CPU clock to the external oscillator after the rising of power supply voltage passes the minimum operation voltage and after an oscillation is stabilized.

Note: The minimum operation voltage is decided by the division ratio of an external oscillator's frequency and a CPU clock. Decide on an external oscillator's oscillation stabilizing time after fully evaluating an oscillator's stabilizing time used.

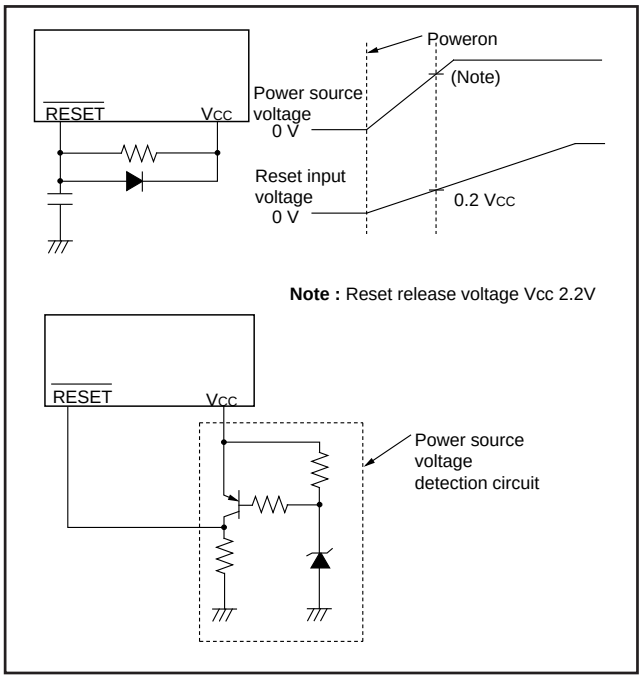



**Fig. 38 Example of reset circuit**

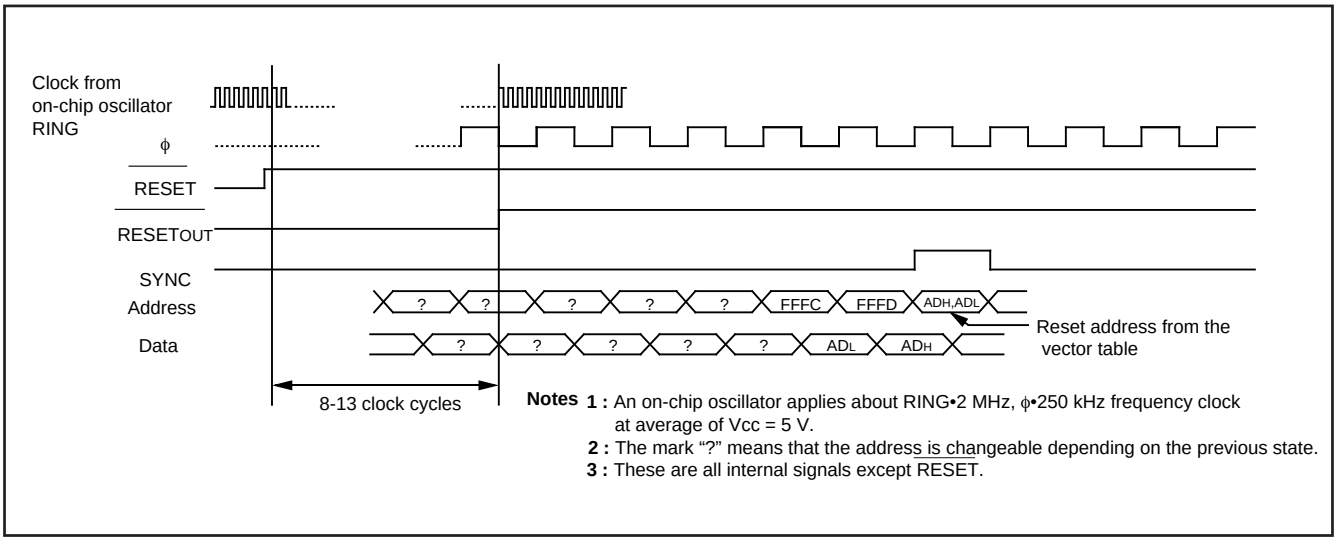



**Fig. 39 Timing diagram at reset**

## Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.
Use the circuit constants in accordance with the resonator manufacturer's recommended values.
No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.)

**(1) On-chip oscillator operation**

When the MCU operates by the on-chip oscillator for the main clock, connect XIN pin to VCC and leave XOUT pin open.
The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies when designing application products.

**(2) Ceramic resonator and quartz-crystal oscillator**

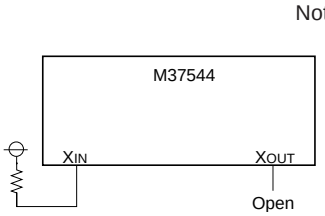
When the ceramic resonator and quartz-crystal oscillator is used for the main clock, connect the ceramic/quartz-crystal oscillator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT.

**(3) RC oscillation**

When the RC oscillation is used for the main clock, connect the XIN pin and XOUT pin to the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

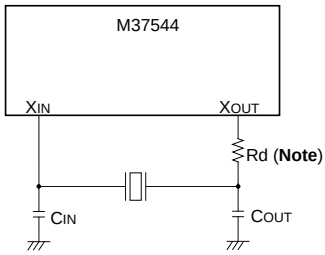
**(4) External clock**

When the external signal clock is used for the main clock, connect the XIN pin to the clock source and leave XOUT pin open.



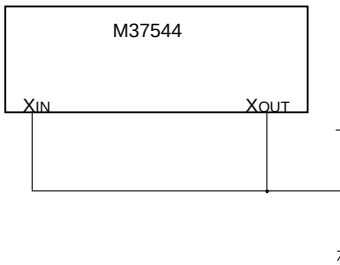

Note: The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies and obtain the sufficient margin.

**Fig. 41 Processing of XIN and XOUT pins at on-chip oscillator operation**




Note: Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip through a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

**Fig. 42 External circuit of ceramic resonator and quartz-crystal oscillator**




Note: Connect the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

**Fig. 43 External circuit of RC oscillation**

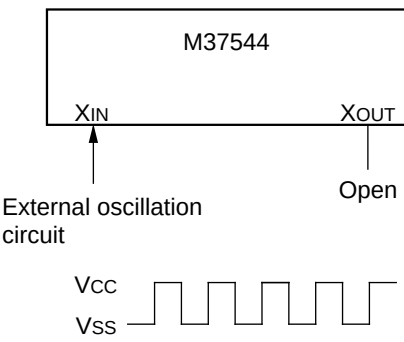



**Fig. 44 External clock input circuit**

**(1) Oscillation control**

**• Stop mode**

When the STP instruction is executed, the internal clock φ stops at an "H" level and the XIN oscillator stops. At this time, timer 1 is set to "01$_{16}$" and prescaler 1 is set to "FF$_{16}$" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. Single selected by the timer 1 count source selection bit is connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock φ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock φ is supplied. This is because when a ceramic/quartz-crystal oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable. Also, the STP instruction cannot be used while CPU is operating by an on-chip oscillator.

**• Wait mode**

If the WIT instruction is executed, the internal clock φ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

**■ Notes on clock generating circuit**

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Switch of ceramic/quartz-crystal and RC oscillations

After releasing reset the operation starts by starting an on-chip oscillator. Then, a ceramic/quartz-crystal oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

• Double-speed mode

When a ceramic/quartz-crystal oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

• CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37544RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

• Clock division ratio, XIN oscillation control, on-chip oscillator control

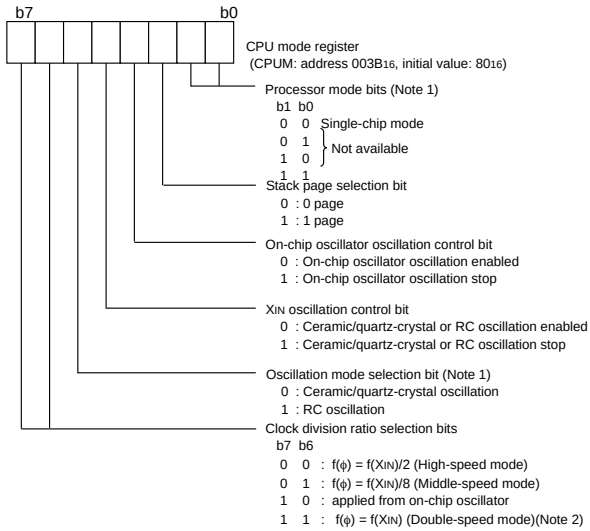
The state transition shown in Fig. 49 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), on-chip oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 49.

• Count source (Timer 1, Timer A, Timer X, Serial I/O, A/D converter, Watchdog timer)

The count sources of these functions are affected by the clock division selection bit of the CPU mode register.

The f(XIN) clock is supplied to the watchdog timer when selecting f(XIN) as the CPU clock.

The on-chip oscillator output is supplied to these functions when selecting the on-chip oscillator output as the CPU clock.




**Note 1:** The bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. However, by reset the bit is initialized and can be rewritten, again.
(It is not disable to write any data to the bit for emulator MCU "M37544RSS".)

**2:** These bits are used only when a ceramic/quartz-crystal oscillation is selected. Do not use these when an RC oscillation is selected.

**Fig. 45 Structure of CPU mode register**

## NOTES ON USE

## Countermeasures against noise

**1. Shortest wiring length**

(1) Package

Select the smallest possible package to make the total wiring length short.

<Reason>

The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

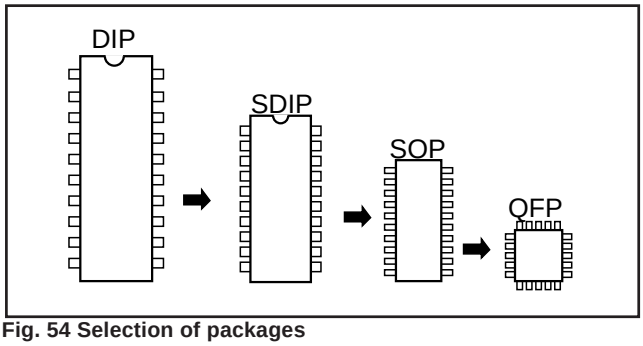



**Fig. 54 Selection of packages**

(2) Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20 mm).

<Reason>

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

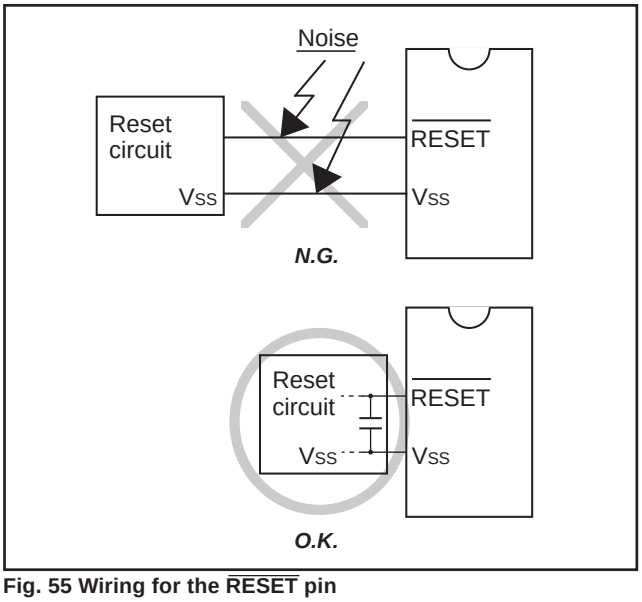



**Fig. 55 Wiring for the $\overline{\text{RESET}}$ pin**

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

<Reason>

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

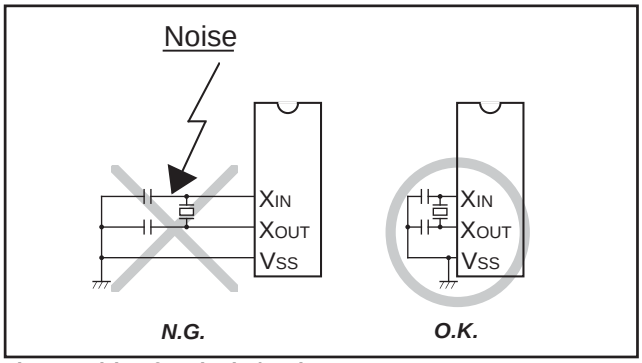



**Fig. 56 Wiring for clock I/O pins**

(4) Wiring to CNVss pin

Connect CNVss pin to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

In order to improve the noise reduction, to connect a 5 kΩ resistor serially to the CNVss pin - GND line may be valid.

As well as the above-mentioned, in this case, connect to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

<Reason>

The CNVss pin of the QzROM is the power source input pin for the built-in QzROM. When programming in the built-in QzROM, the impedance of the CNVss pin is low to allow the electric current for writing flow into the QzROM. Because of this, noise can enter easily. If noise enters the CNVss pin, abnormal instruction codes or data are read from the built-in QzROM, which may cause a program runaway.

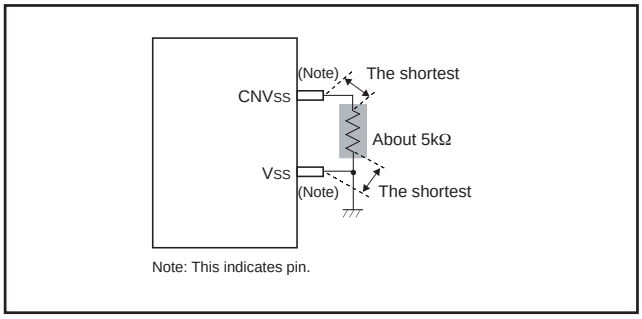



**Fig. 57 Wiring for the CNVss pin of the QzROM**

5. Setup for I/O ports
Setup I/O ports using hardware and software as follows:

<Hardware>
• Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>
• As for an input port, read data several times by a program for checking whether input levels are equal or not.
• As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
• Rewrite data to direction registers and pull-up control registers at fixed periods.

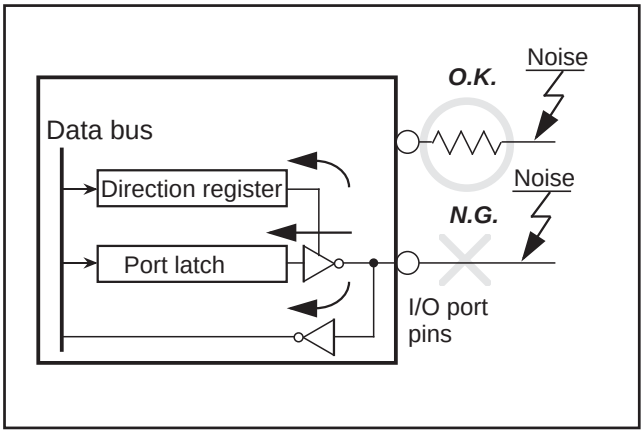



**Fig. 62 Setup for I/O ports**

6. Providing of watchdog timer function by software
If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.
In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.
This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>
• Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:
N+1 ≥ (Counts of interrupt processing executed in each main routine)
As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.
• Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
• Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>
• Decrements the SWDT contents by 1 at each interrupt processing.
• Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
• Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

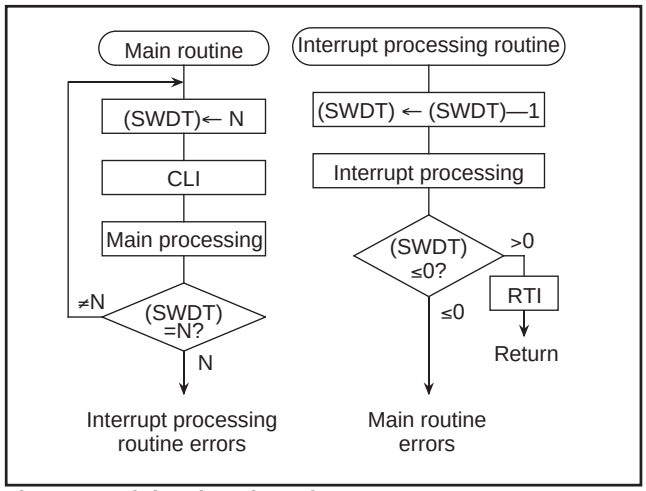



**Fig. 63 Watchdog timer by software**

# NOTES ON QzROM

## Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

## Precautions Regarding Overvoltage

Make sure that voltage exceeding the $V_{CC}$ pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for $CNV_{SS}$ pin ($V_{PP}$ power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

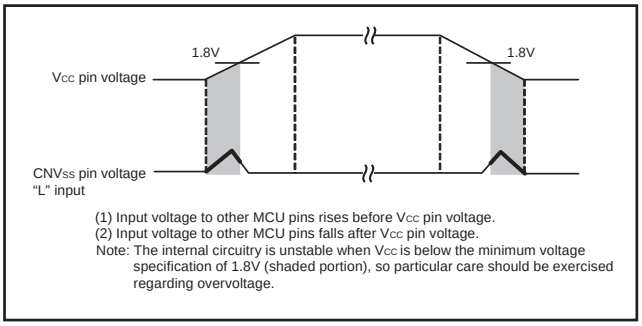



**Fig. 64 Timing Diagram (bold-lined periods are applicable)**

## Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "$00_{16}$" and "$FF_{16}$" can not be accepted.
- Set "$FF_{16}$" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "$FF_{16}$" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

## Data Required For QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

## Electrical Characteristics

**Table 13 Electrical characteristics (1) ($V_{CC}$ = 1.8 to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to 85 °C, unless otherwise noted)**

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{OH}$ | "H" output voltage<br>$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$ (**Note 1**) | $I_{OH}$ = –5 mA<br>$V_{CC}$ = 4.0 to 5.5 V | $V_{CC}$–1.5 | | | V |
| | | $I_{OH}$ = –1.0 mA<br>$V_{CC}$ = 1.8 to 5.5 V | $V_{CC}$–1.0 | | | V |
| $V_{OL}$ | "L" output voltage<br>$P1_0$–$P1_4$, $P2_0$–$P2_5$ | $I_{OL}$ = 5 mA<br>$V_{CC}$ = 4.0 to 5.5 V | | | 1.5 | V |
| | | $I_{OL}$ = 1.5 mA<br>$V_{CC}$ = 4.0 to 5.5 V | | | 0.3 | V |
| | | $I_{OL}$ = 1.0 mA<br>$V_{CC}$ = 1.8 to 5.5 V | | | 1.0 | V |
| $V_{OL}$ | "L" output voltage<br>$P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$ | $I_{OL}$ = 15 mA<br>$V_{CC}$ = 4.0 to 5.5 V | | | 2.0 | V |
| | | $I_{OL}$ = 1.5 mA<br>$V_{CC}$ = 4.0 to 5.5 V | | | 0.3 | V |
| | | $I_{OL}$ = 10 mA<br>$V_{CC}$ = 1.8 to 5.5 V | | | 1.0 | V |
| $V_{T+}$–$V_{T-}$ | Hysteresis<br>$CNTR_0$, $CNTR_1$, $INT_0$, $INT_1$ (**Note 2**)<br>$P0_0$–$P0_7$ (**Note 3**) | | | 0.4 | | V |
| $V_{T+}$–$V_{T-}$ | Hysteresis<br>RxD, SCLK (**Note 2**) | | | 0.5 | | V |
| $V_{T+}$–$V_{T-}$ | Hysteresis<br>$\overline{RESET}$ | | | 0.9 | | V |
| $I_{IH}$ | "H" input current<br>$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$ | $V_I$ = $V_{CC}$<br>(Pin floating. Pull up transistors "off") | | | 5.0 | µA |
| $I_{IH}$ | "H" input current<br>$\overline{RESET}$ | $V_I$ = $V_{CC}$ | | | 5.0 | µA |
| $I_{IH}$ | "H" input current<br>$X_{IN}$ | $V_I$ = $V_{CC}$ | | 4.0 | | µA |
| $I_{IL}$ | "L" input current<br>$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$ | $V_I$ = $V_{SS}$<br>(Pin floating. Pull up transistors "off") | | | –5.0 | µA |
| $I_{IL}$ | "L" input current<br>$\overline{RESET}$, $CNV_{SS}$ | $V_I$ = $V_{SS}$ | | | –5.0 | µA |
| $I_{IL}$ | "L" input current<br>$X_{IN}$ | $V_I$ = $V_{SS}$ | | –4.0 | | µA |
| $I_{IL}$ | "L" input current<br>$P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$ | $V_I$ = $V_{SS}$<br>(Pull up transistors "on") | | –0.2 | –0.5 | mA |
| $V_{RAM}$ | RAM hold voltage | When clock stopped | 1.6 | | 5.5 | V |
| ROSC | On-chip oscillator oscillation frequency | $V_{CC}$ = 5.0 V, Ta = 25 °C | 1000 | 2000 | 3000 | kHz |
| DOSC | Oscillation stop detection circuit detection frequency | $V_{CC}$ = 5.0 V, Ta = 25 °C | 62.5 | 125 | 187.5 | kHz |

**Notes 1:** $P1_1$ is measured when the $P1_1$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
**2:** RxD, SCLK, $INT_0$, and $INT_1$ have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
**3:** It is available only when operating key-on wake up.

## Notes on Oscillation Stop Detection Circuit

1. Oscillation stop detection status bit is initialized by the following operation.
(1) External reset
(2) Write "0" data to the ceramic or RC oscillation stop detection function active bit.

2. The oscillation stop detection circuit is not included in the emulator MCU "M37544RSS".

## Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

## NOTES ON HARDWARE

1. Handling of Power Source Pin
In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.

2. Handling of CNVss Pin
The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin ($V_{PP}$ pin) as well.
To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.

## NOTES ON QzROM

## Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

## Precautions Regarding Overvoltage

Make sure that voltage exceeding the $V_{CC}$ pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for $CNV_{SS}$ pin ($V_{PP}$ power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

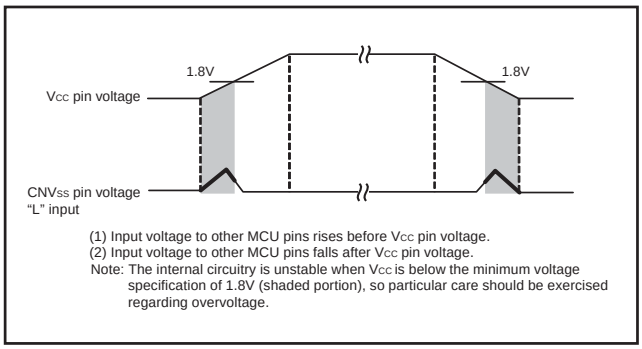



**Fig. 7 Timing Diagram (bold-lined periods are applicable)**

## Notes on QzROM Writing Orders

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- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "$00_{16}$" and "$FF_{16}$" can not be accepted.
- Set "$FF_{16}$" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "$FF_{16}$" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

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* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

| REVISION HISTORY | 7544 Group (QzROM version) Data Sheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Oct 26, 2004 | – | First edition issued |
| 1.01 | Nov 24, 2004 | 46<br>48-50 | Table 12 Electrical characteristics: Minimum value of $V_{RAM}$ revised.<br>The followings are added;<br>- A/D Converter characteristics<br>- Timing requirements<br>- Switching Characteristics<br>- Timing chart |
| 1.02 | Jul 20, 2005 | All pages<br>2, 4, 5, 7<br>3<br>7<br>12<br><br>18<br>41<br><br><br>45<br>53<br>61 | Delete the following: "PRELIMINARY".<br>Package names are revised.<br>Table 1 Performance overview is added.<br>Table 2 is deleted.<br>ROM code protect is added.<br>Fig.10 is partly revised.<br>Termination of unused pins is added.<br>(4)Wiring to $CNV_{SS}$ pin is deleted.<br>(4)Wiring to $V_{PP}$ pin is revised.<br>Fig.49 is partly revised.<br>Table 8 is partly revised.<br>PACKAGE OUTLINE is revised.<br>Product shipped in blank, NOTES ON QzROM, DATA REQUIRED FOR QzROM WRITING ORDERS are added. |
| 1.03 | Mar 31, 2009 | 3,8<br>13<br>17<br>18<br>19<br>20-25<br>36, 70, 71<br><br>36<br><br><br><br>37<br><br>41<br>45-49<br>50<br>51<br>54<br>55<br>65<br><br><br>66<br>70 | 42S1M package added<br>Fig. 11 Memory map diagram revised<br>Fig. 15 (5)Port $P1_1$ revised<br>Fig. 16 (8)Port $P1_4$ revised<br>Table 7 $X_{IN}$, $X_{OUT}$ added<br>“Interrupts” revised<br>Operation of STP instruction disable bit<br>→ Operation of STP instruction function selection bit<br>Watchdog Timer<br>“Operation of watchdog timer H count source selection bit” revised<br>“Operation of STP instruction function selection bit” revised<br>“Notes on watchdog timer” added<br>-Fig. 36 Block diagram of watchdog timer revised<br>-Fig. 37 Structure of watchdog timer control register revised<br>“-Clock division ratio, $X_{IN}$ oscillation control, on-chip oscillator control” added<br>“QzROM Writing Mode”added<br>“Processor Status Register”revised<br>Fig. 57 $V_{PP}$ → $CNV_{SS}$<br>5. Setup for I/O ports “Note” deleted<br>“NOTES ON QzROM” added<br>-“1. Processor Status Register”revised<br>APPENDIX “Fig. 2 Sequence of PLP Instruction execution deleted.<br>-Figure title of Fig. 3 revised<br>“3. Modifying output data with bit managing instruction” revised<br>Notes on A/D conversion 1. Analog input pin revised<br>Notes on Watchdog Timer revised |