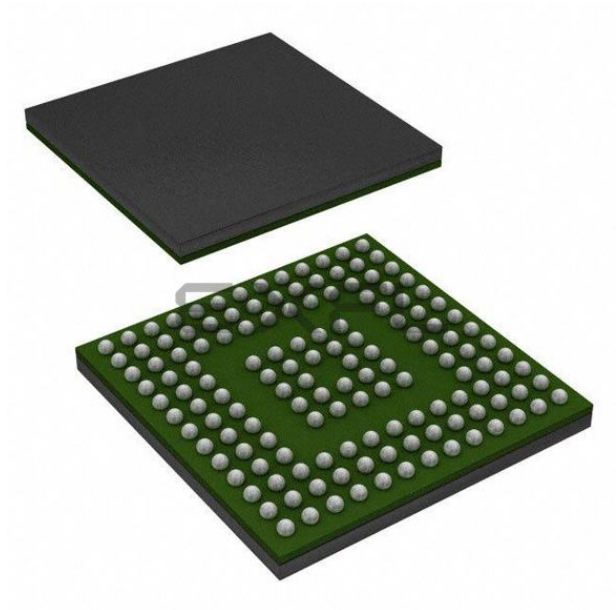

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

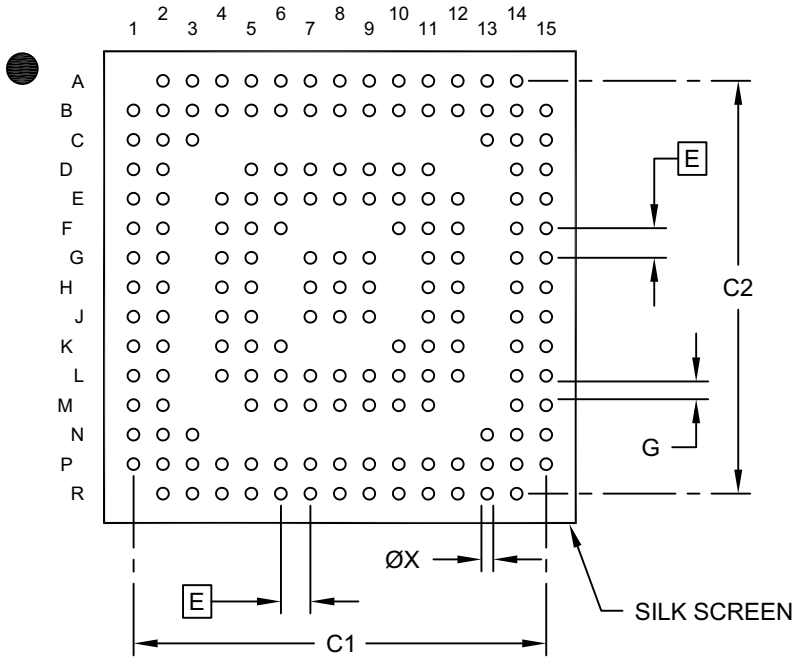
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	ARM® Cortex®-M4
Program Memory Type	-
Controller Series	MEC170x
RAM Size	256KB
Interface	ACPI, EBI/EMI, eSPI, I²C, LPC, PECI, PS/2, QSPI, SPI
Number of I/O	123
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	144-WFBGA
Supplier Device Package	144-WFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1701h-c1-sz

169-Ball Very Very Thin Fine Pitch Ball Grid Array (XYX) - 8x8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Overall Contact Pad Spacing	C1		7.00	
Overall Contact Pad Spacing	C2		7.00	
Contact Pad Width (X169)	X			0.20
Contact Pad to Contact Pad	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2470 Rev. A

TABLE 3-2: GPIO PIN CONTROL REGISTERS DEFAULTS (CONTINUED)

GPIO Name	Pin Control Register Offset (Hex)	Pin Control Register Default Value (Hex)	Pin Control Register Default Function	Pin Control 2 Register Offset (Hex)	Pin Control 2 Register Default Value (Hex)
GPIO065	00D4	00000040	GPIO065	5D4	000
GPIO066	00D8	00000040	GPIO066	5D8	000
GPIO067	00DC	00000040	GPIO067	5DC	000
GPIO070	00E0	00000040	GPIO070	5E0	000
GPIO071	00E4	00000040	GPIO071	5E4	000
GPIO072	00E8	00000040	GPIO072	5E8	000
GPIO073	00EC	00000040	GPIO073	5EC	000
GPIO100	0100	00000040	GPIO100	600	000
GPIO101	0104	00000040	GPIO101	604	000
GPIO102	0108	00000040	GPIO102	608	000
GPIO104	0110	00000040	GPIO104	610	000
GPIO105	0114	00000040	GPIO105	614	000
GPIO106	0118	00000040	GPIO106	618	000
GPIO107	011C	00000040	GPIO107	61C	000
GPIO110	0120	00000040	GPIO110	620	000
GPIO111	0124	00000040	GPIO111	624	000
GPIO112	0128	00000040	GPIO112	628	000
GPIO113	012C	00000040	GPIO113	62C	000
GPIO114	0130	00000040	GPIO114	630	000
GPIO115	0134	00000040	GPIO115	634	000
GPIO120	0140	00000040	GPIO120	640	000
GPIO121	0144	00000040	GPIO121	644	000
GPIO122	0148	00000040	GPIO122	648	000
GPIO123	014C	00000040	GPIO123	64C	000
GPIO124	0150	00000040	GPIO124	650	000
GPIO125	0154	00000040	GPIO125	654	000
GPIO126	0158	00000040	GPIO126	658	000
GPIO127	015C	00000040	GPIO127	65C	000
GPIO130	0160	00000040	GPIO130	660	000
GPIO131	0164	00000040	GPIO131	664	000
GPIO132	0168	00000040	GPIO132	668	000
GPIO133	016C	00000040	GPIO133	66C	000
GPIO134	0170	00000040	GPIO134	670	000
GPIO135	0174	00000040	GPIO135	674	000
GPIO140	0180	00000040	GPIO140	680	000
GPIO141	0184	00000040	GPIO141	684	000
GPIO142	0188	00000040	GPIO142	688	000
GPIO143	018C	00000040	GPIO143	68C	000
GPIO144	0190	00000040	GPIO144	690	000
GPIO145	0194	00000040	GPIO145	694	000
GPIO146	0198	00000040	GPIO146	698	000
GPIO147	019C	00000040	GPIO147	69C	000

Block	Instance	Register	Register Address
16-bit PWM	4	TEST	4000584Ch
16-bit PWM	5	PWMx Counter ON Time Register	40005850h
16-bit PWM	5	PWMx Counter OFF Time Register	40005854h
16-bit PWM	5	PWMx Configuration Register	40005858h
16-bit PWM	5	TEST	4000585Ch
16-bit PWM	6	PWMx Counter ON Time Register	40005860h
16-bit PWM	6	PWMx Counter OFF Time Register	40005864h
16-bit PWM	6	PWMx Configuration Register	40005868h
16-bit PWM	6	TEST	4000586Ch
16-bit PWM	7	PWMx Counter ON Time Register	40005870h
16-bit PWM	7	PWMx Counter OFF Time Register	40005874h
16-bit PWM	7	PWMx Configuration Register	40005878h
16-bit PWM	7	TEST	4000587Ch
16-bit PWM	8	PWMx Counter ON Time Register	40005880h
16-bit PWM	8	PWMx Counter OFF Time Register	40005884h
16-bit PWM	8	PWMx Configuration Register	40005888h
16-bit PWM	8	TEST	4000588Ch
16-bit PWM	9	PWMx Counter ON Time Register	40005890h
16-bit PWM	9	PWMx Counter OFF Time Register	40005894h
16-bit PWM	9	PWMx Configuration Register	40005898h
16-bit PWM	9	TEST	4000589Ch
16-bit PWM	10	PWMx Counter ON Time Register	400058A0h
16-bit PWM	10	PWMx Counter OFF Time Register	400058A4h
16-bit PWM	10	PWMx Configuration Register	400058A8h
16-bit PWM	10	TEST	400058ACh
16-bit Tach	0	TACHx Control Register	40006000h
16-bit Tach	0	TACHx Status Register	40006004h
16-bit Tach	0	TACHx High Limit Register	40006008h
16-bit Tach	0	TACHx Low Limit Register	4000600Ch
16-bit Tach	1	TACHx Control Register	40006010h
16-bit Tach	1	TACHx Status Register	40006014h
16-bit Tach	1	TACHx High Limit Register	40006018h
16-bit Tach	1	TACHx Low Limit Register	4000601Ch
16-bit Tach	2	TACHx Control Register	40006020h
16-bit Tach	2	TACHx Status Register	40006024h
16-bit Tach	2	TACHx High Limit Register	40006028h
16-bit Tach	2	TACHx Low Limit Register	4000602Ch
PECI	0	Write Data Register	40006400h
PECI	0	Read Data Register	40006404h
PECI	0	Control Register	40006408h
PECI	0	Status Register 1	4000640Ch
PECI	0	Status Register 2	40006410h
PECI	0	Error Register	40006414h

7.9.13 DMA CHANNEL N FILL ENABLE REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	FILL_MODE_ENABLE 1=Enable the calculation of CRC-32 for DMA Channel N 0=Disable the calculation of CRC-32 for DMA Channel N	R/W	0h	RESET

7.9.14 DMA CHANNEL N FILL DATA REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	DATA This is the data pattern used to fill memory.	R/W	0h	RESET

7.9.15 DMA CHANNEL N FILL STATUS REGISTER

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	Reserved	R	-	-
1	FILL_RUNNING This bit is ‘1b’ when the Fill operation starts and is cleared to ‘0b’ when the Fill operation completes.	R	0h	RESET
0	FILL_DONE This bit is set to ‘1b’ when the Fill operation has completed from either normal or forced termination. It is cleared to ‘0b’ when the DMA controller starts a new transfer on the channel.	R	0h	RESET