Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	ARM® Cortex®-M4
Program Memory Type	-
Controller Series	MEC170x
RAM Size	480KB
Interface	ACPI, EBI/EMI, eSPI, I²C, LPC, PECI, PS/2, QSPI, SPI
Number of I/O	148
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	169-WFBGA
Supplier Device Package	169-WFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1701q-c2-tn

MEC1705/MEC1704-144-SZ	MEC1701/MEC1703-144-SZ	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
C7	C7	GPIO147/I2C08_SDA/JTAG_CLK	VTR1	PIO	X		X	X
C8	C8	GPIO243	VTR1	PIO	X		X	X
C9	C9	GPIO155/I2C02_SCL/PS2_DAT1B	VTR1	PIO	X	X	X	X
C10	C10	GPIO010/I2C03_SCL/PS2_DAT0B	VTR1	PIO	X	X	X	X
C11	C11	GPIO124/GPTP-OUT6/PVT_CS#/KSO11	VTR1	PIO	X		X	X
C12		GPIO156/LED0	VTR1	PIO	X	X	X	X
	C12	GPIO153/LED2	VTR1	PIO	X	X	X	X
C13	C13	GPIO175/KSO17	VTR1	PIO	X		X	X
D1	D1	GPIO057/VCC_PWRGD	VTR1	PIO	X		X	X
D2	D2	GPIO060/KBRST/48MHZ_OUT	VTR1	PIO	X		X	X
D3	D3	RESETI#	VTR1	In	X		X	X
D11	D11	GPIO125/GPTP-OUT5/PVT_CLK/KSO12	VTR1	PIO	X		X	X
D12	D12	GPIO126/PVT_IO3/KSO13	VTR1	PIO	X		X	X
D13	D13	GPIO127/A20M/UART0_CTS#	VTR1	PIO	X		X	X
E1	E1	VTR_PLL		PWR				
E2	E2	GPIO022/GPTP-IN0	VTR1	PIO	X		X	X
E3	E3	GPIO106/PWROK	VTR1	PIO	X		X	X
E5	E5	VBAT		PWR				
E6	E6	GPIO163/VCI_IN0#	VBAT	PIO	X		X	X
E7	E7	GPIO144/I2C04_SCL/SPI1_CS#/UART0_RI#/TRACEDAT3	VTR1	PIO	X		X	X
E8	E8	GPIO045/KSO01	VTR1	PIO	X		X	X
E9	E9	GPIO046/BCM1_DAT/KSO02	VTR1	PIO	X		X	X
E11	E11	GPIO122/BCM0_DAT/PVT_IO1/KSO09	VTR1	PIO	X		X	X
E12	E12	GPIO123/BCM0_CLK/PVT_IO2/KSO10	VTR1	PIO	X		X	X
E13		GPIO134/PWM10/UART1_RTS#	VTR1	PIO	X		X	X
	E13	GPIO035/PWM8/CTOUT1	VTR1	PIO	X	X	X	X
F1	F1	VFLT_PLL		PWR				
F2	F2	GPIO226/LED3	VTR1	PIO	X	X	X	X
F3	F3	GPIO050/FAN_TACH0/GTACH0	VTR1	PIO	X	X	X	X
F5	F5	GPIO003/I2C00_SDA/SPI0_CS#	VTR1	PIO	X		X	X
F6	F6	VSS1		PWR				
F7	F7	GPIO142/I2C05_SCL/SPI1_MOSI/UART0_DSR#/TRACEDAT1	VTR1	PIO	X		X	X
F8	F8	GPIO150/I2C08_SCL/JTAG_TMS	VTR1	PIO	X		X	X
F9	F9	GPIO105/UART0_RX	VTR1	PIO	X		X	X
F11	F11	GPIO104/UART0_TX	VTR1	PIO	X		X	X
F12	F12	GPIO121/PVT_IO0/KSO08	VTR1	PIO	X		X	X

Signal	Emulated Power Rail	Gated State	Notes
TIN2	VTR	Low	
TIN3	VTR	Low	
TOUT0	VTR	Low	
TOUT1	VTR	Low	
TOUT2	VTR	Low	
TOUT3	VTR	Low	
TRACECLK	VTR	Low	
TRACEDAT0	VTR	Low	
TRACEDAT1	VTR	Low	
TRACEDAT2	VTR	Low	
TRACEDAT3	VTR	Low	
UART_CLK	VTR	Low	
UART0_CTS#	VTR	Low	Note 4
UART0_DCD#	VTR	High	Note 4
UART0_DSR#	VTR	High	Note 4
UART0_DTR#	VTR	High	Note 4
UART0_RI#	VTR	High	Note 4
UART0_RTS#	VTR	Low	Note 4
UART0_RX	VTR	Low	Note 4
UART0_TX	VTR	Low	Note 4
UART1_CTS#	VTR	Low	Note 4
UART1_RTS#	VTR	Low	Note 4
UART1_RX	VTR	Low	Note 4
UART1_TX	VTR	Low	Note 4
VBAT			
VCC_PWRGD	VTR	High	
VCI_IN0#	VTR	No Gate	Note 13
VCI_IN1#	VTR	No Gate	Note 13
VCI_IN2#	VTR	No Gate	Note 13
VCI_IN3#	VTR	No Gate	Note 13
VCI_IN4#	VTR	No Gate	Note 13
VCI_OUT	VTR	Low	
VFLT_PLL			
VR_CAP			Note 15
VREF_ADC			
VREF_VTT			
VSS_ADC			
VSS_ANALOG			
VSS_REG			
VSS1			
VSS2			
VSS3			
VTR_ANALOG			

Feature	Instance	Logical Device Number (LDN)	Base Address
Embedded Memory Interface (EMI)	2	12h	400F_4800h
Real Time Clock		14h	400F_5000h
BIOS Debug Port (Port 80)	0	20h	400F_8000h
BIOS Debug Port (Port 80)	1	21h	400F_8400h
eSPI Virtual Wires			400F_9C00h
Global Configuration		3Fh	400F_FF00h
Note 1: The eSPI block occupies two logical devices, Dh and Eh			

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ22	0	LPC Interface	LPC_WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - LPC Traffic Detected	N/A	N/A
	1	SMB-I2C Controller 0	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.0 START Detected		
	2	SMB-I2C Controller 1	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.1 START Detected		
	3	SMB-I2C Controller 2	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.2 START Detected		
	4	SMB-I2C Controller 3	SMB-I2C _WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - SMB-I2C.3 START Detected		
	5-8	Reserved					
	9	ESPI Interface	ESPI_WAKE_ONLY	Yes	Wake-Only Event (No Interrupt Generated) - ESPI Traffic Detected		
	10-31	Reserved					

TABLE 4-7: DEFINITION OF RESET SIGNALS (CONTINUED)

Reset	Description	Source
RESET_VTR	Internal VTR Reset signal.	This internal reset signal is asserted as long as the reset generator determines that the output of the internal regulator is stable at its target voltage and that the voltage rail supplying the main clock PLL is at 3.3V. Although most VTR-powered registers are reset on RESET_SYS, some registers are only reset on this reset.
RESET_SYS	Internal Reset signal. This signal is used to reset VTR powered registers.	RESET_SYS is the main global reset signal. This reset signal will be asserted if: • RESET_VTR is asserted • The RESETI# pin asserted • A WDT Event event is asserted • A soft reset is asserted by the SOFT_SYS_RESET bit in the System Reset Register • ARM M4 SYSRESETREQ
RESET_eSPI	System reset signal connected to the eSPI ESPI_RESET# pin.	Pin Interface, ESPI_RESET# pin.
RESET_VCC	Performs a reset when Host power (VCC) is turned off	This signal is asserted if • RESET_SYS is asserted • VCC_PWRGD is low • The PWR_INV bit in the Power Reset Control Register is ‘1b’ The PWROK output pin is an inverted version of this reset; it is asserted when VCC_PWRGD is high and the PWR_INV bit is ‘0b’. **Note:** This reset is referred to as RESET_SIO in the eSPI Block Specification.
RESET_HOST	Performs a reset when VCC_PWRGD is low or when the system host resets the Host Interface.	This signal is asserted if • RESET_SYS is asserted • VCC_PWRGD is low • The PWR_INV bit in the Power Reset Control Register is ‘1b’ • The HOST_RESET_SELECT bit in the Power Reset Control Register is configured for LRESET# and the LRESET# signal is asserted • The HOST_RESET_SELECT bit in the Power Reset Control Register is configured for eSPI_PLTRST# and the eSPI_PLTRST# signal from the eSPI block is asserted.
WDT Event	A WDT Event generates the RESET_SYS event. This signal resets VTR powered registers with the exception of the WDT Event Count Register register. Note that the glitch protect circuits do not activate on a WDT reset. WDT Event does not reset VBAT registers or logic.	This reset signal will be asserted if: • A WDT Event event is asserted This event is indicated by the WDT bit in the Power-Fail and Reset Status Register

TABLE 7-10: CHANNEL REGISTER SUMMARY (CONTINUED)

Offset	Register Name (Note 1)
04h	DMA Channel N Memory Start Address Register
08h	DMA Channel N Memory End Address Register
0Ch	DMA Channel N Device Address
10h	DMA Channel N Control Register
14h	DMA Channel N Interrupt Status Register
18h	DMA Channel N Interrupt Enable Register
1Ch	TEST
20h (Note 2)	DMA Channel N CRC Enable Register
24h (Note 2)	DMA Channel N CRC Data Register
28h (Note 2)	DMA Channel N CRC Post Status Register
2Ch (Note 2)	TEST
20h (Note 3)	DMA Channel N Fill Enable Register
24h (Note 3)	DMA Channel N Fill Data Register
28h (Note 3)	DMA Channel N Fill Status Register
2Ch (Note 3)	TEST

Note 1: The letter 'N' following DMA Channel indicates the Channel Number. Each Channel implemented will have these registers to determine that channel's operation.

2: These registers are only present on DMA Channel 0. They are reserved on all other channels.

3: These registers are only present on DMA Channel 1. They are reserved on all other channels.

7.9.3 DMA CHANNEL N ACTIVATE REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	CHANNEL_ACTIVATE Enable this channel for operation. The DMA Main Control:Activate must also be enabled for this channel to be operational.	R/W	0h	RESET

9.8.1.1 LPC I/O Cycles

The system host may use LPC I/O cycles to read/write the I/O mapped configuration and runtime registers implemented in this device. See the Intel® Low Pin Count (LPC) Interface Specification, v1.1, Section 5.2 for definition of LPC I/O Cycles.

9.8.1.2 LPC Memory Cycles

The system host may use LPC memory cycles to access memory mapped registers and internal RAMs implemented in this device. See the Intel® Low Pin Count (LPC) Interface Specification, v1.1, Section 5.1 for definition of LPC Memory Cycles.

9.8.1.3 LAD[3:0] Fields

The LAD[3:0] signals support multiple fields for each protocol as defined in section 4.2.1 LAD[3:0] of the Intel® Low Pin Count (LPC) Interface Specification, v1.1. The following sections further qualify the fields supported.

9.8.1.4 SYNCs on LPC

LPC transactions that access registers located on the device will require a minimum of two wait SYNCs on the LPC bus. The number of SYNCs may be larger if the internal bus is in use by the embedded controller, of if the data referenced by the host is not present in a register. The device always uses Long Wait SYNCs, rather than Short Wait SYNCs, when responding to an LPC bus request.

Note:	All LPC transactions are synchronized to the LCLK and will complete with a maximum of 8 wait states, unless otherwise noted.

The device does not issue ERROR SYNC cycles.

9.8.2 LPC POWER DOWN

The MEC170x tolerates the LPCPD# signal going active and then inactive again without LRESET# going active. This is a requirement for notebook power management functions.

The Intel® Low Pin Count (LPC) Interface Specification, v1.1, Section 8.2 states that “After LPCPD# goes back inactive, the LPC interface will always be reset using LRESET#”. This text must be qualified for mobile systems where it is possible that when exiting a “light” sleep state (ACPI S1, APM POS), LPCPD# may be asserted but the LPC Bus power may not be removed, in which case LRESET# will not occur. When exiting a “deeper” sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRESET# will occur.

The LPCPD# pin is implemented as a “local” powergood for the LPC bus. It is not to be used as a global powergood for the chip. It is used to minimize the LPC power dissipation.

Prior to going to a low-power state, the system asserts the LPCPD# signal. LPCPD# goes active at least 30 microseconds prior to the LCLK signal stopping low and power being shut to the other LPC interface signals. Upon recognizing LPCPD# active, there are no further transactions on the LPC interface.

9.8.3 LPC CLOCK RUN

The CLKRUN# pin is an open drain output and input. The CLKRUN# function is described in the PCI Mobile Design Guide Rev 1.0. CLKRUN# is used to indicate the status of the LPC bus clock LCLK, as well as to request that LCLK be started if it is stopped. The following figure shows a typical system implementation incorporating CLKRUN#.

Logical Device. The Configuration Registers are accessed through the Configuration Port. Registers located at offsets 330h through 3FFh are mapped to Configuration Port offsets 30h through FFh. Configuration Port offsets 00h through 2Fh, for all Host Logical Devices, are mapped to the Global Configuration Registers.

10.7.1 ESPI I/O COMPONENT

TABLE 10-3: ESPI I/O COMPONENT REGISTER SUMMARY

Host Offset	EC Offset	Register Name
RUNTIME REGISTERS		
Peripheral Channel		
00h	00h	INDEX Register
01h	01h	DATA Register
EC PRIVATE REGISTERS		
Peripheral Channel		
-	100h	Peripheral Channel Last Cycle Register
-	10Ch	Peripheral Channel Error Address Register
-	114h	Peripheral Channel Status Register
-	118h	Peripheral Channel Interrupt Enable Register
-	11Ch	Reserved
-	120h	BAR Inhibit Register
-	128h	eSPI BAR Init Register
-	12Ch	EC IRQ Register
-	130h	TEST
-	134h - 1A7h	I/O Base Address Register Format, Internal Component See Table 10-5, "ESPI I/O Base Address Register Default Values"
-	220h	LTR Peripheral Status Register
-	224h	LTR Peripheral Enable Register
-	228h	LTR Peripheral Control Register
-	22Ch	LTR Peripheral Message Register
OOB Channel		
-	240h	OOB Channel Receive Address Register
-	248h	OOB Channel Transmit Address Register
-	250h	OOB Channel Receive Length Register
-	254h	OOB Channel Transmit Length Register
-	258h	OOB Channel Receive Control Register
-	25Ch	OOB Channel Receive Interrupt Enable Register
-	260h	OOB Channel Receive Status Register
-	264h	OOB Channel Transmit Control Register
-	268h	OOB Channel Transmit Interrupt Enable Register
-	26Ch	OOB Channel Transmit Status Register
Flash Channel		
-	280h	Flash Access Channel Flash Address Register
-	288h	Flash Access Channel Buffer Address Register
-	290h	Flash Access Channel Transfer Length Register
-	294h	Flash Access Channel Control Register
-	298h	Flash Access Channel Interrupt Enable Register
-	29Ch	Flash Access Channel Configuration Register

3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 17-12). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Offset	02h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	FIFO_EN These two bits are set when the FIFO CONTROL Register bit 0 equals 1.	R	0h	RESET
5:4	Reserved	R	-	-
3:1	INTID These bits identify the highest priority interrupt pending as indicated by Table 17-12, "Interrupt Control Table". In non-FIFO mode, Bit[3] is a logic “0”. In FIFO mode Bit[3] is set along with Bit[2] when a timeout interrupt is pending.	R	0h	RESET
0	IPEND This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic ‘0’ an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic ‘1’ no interrupt is pending.	R	1h	RESET

23.0 HIBERNATION TIMER

23.1 Introduction

The Hibernation Timer can generate a wake event to the Embedded Controller (EC) when it is in a hibernation mode. This block supports wake events up to 2 hours in duration. The timer is a 16-bit binary count-down timer that can be programmed in 30.5µs and 0.125 second increments for period ranges of 30.5µs to 2s or 0.125s to 136.5 minutes, respectively. Writing a non-zero value to this register starts the counter from that value. A wake-up interrupt is generated when the count reaches zero.

23.2 References

No references have been cited for this chapter

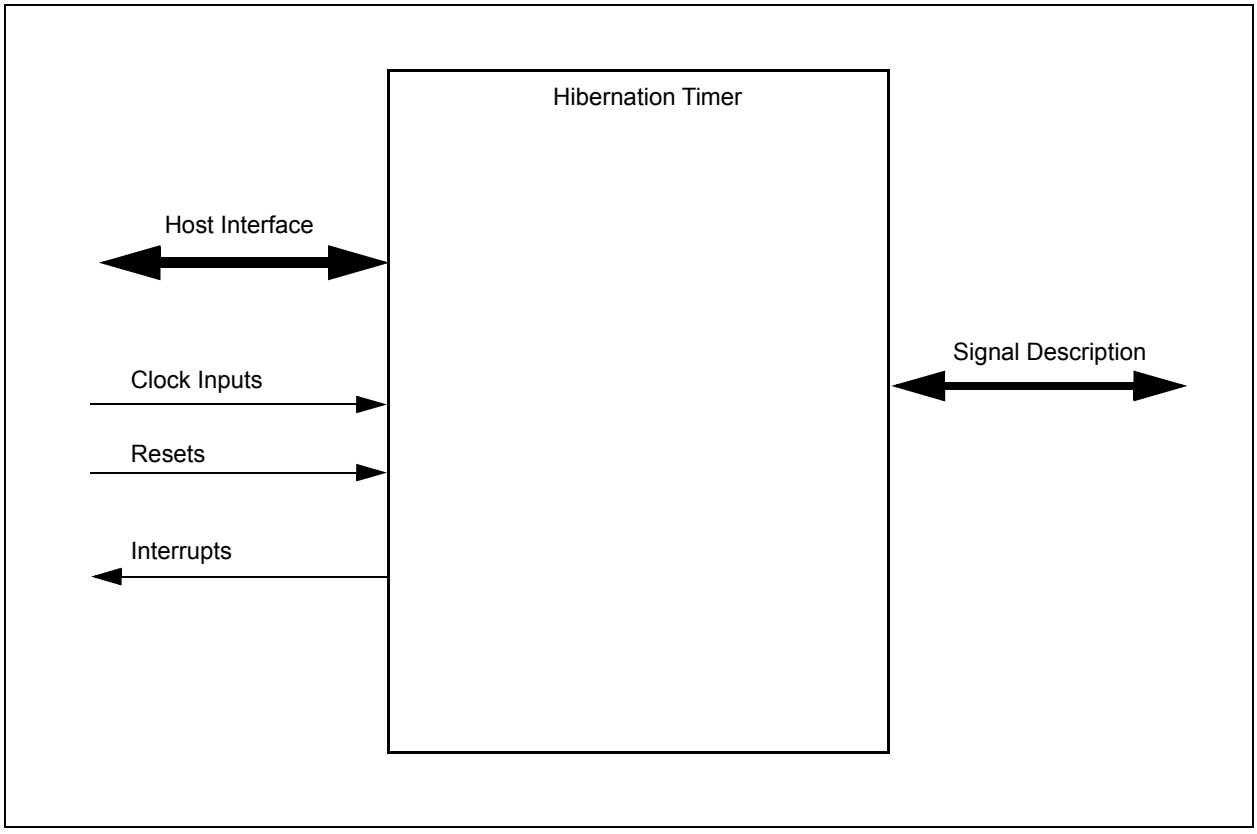
23.3 Terminology

No terms have been cited for this chapter.

23.4 Interface

This block is an IP block designed to be incorporated into a chip. It is designed to be accessed externally via the pin interface and internally via a registered host interface. The following diagram illustrates the various interfaces to the block.

FIGURE 23-1: HIBERNATION TIMER INTERFACE DIAGRAM



23.5 Signal Description

There are no external signals for this block.

33.0 BLINKING/BREATHING PWM

33.1 Introduction

LEDs are used in computer applications to communicate internal state information to a user through a minimal interface. Typical applications will cause an LED to blink at different rates to convey different state information. For example, an LED could be full on, full off, blinking at a rate of once a second, or blinking at a rate of once every four seconds, in order to communicate four different states.

As an alternative to blinking, an LED can “breathe”, that is, oscillate between a bright state and a dim state in a continuous, or apparently continuous manner. The rate of breathing, or the level of brightness at the extremes of the oscillation period, can be used to convey state information to the user that may be more informative, or at least more novel, than traditional blinking.

The blinking/breathing hardware is implemented using a PWM. The PWM can be driven either by the Main system clock or by a 32.768 KHz clock input. When driven by the Main system clock, the PWM can be used as a standard 8-bit PWM in order to control a fan. When used to drive blinking or breathing LEDs, the 32.768 KHz clock source is used.

Features:

- Each PWM independently configurable
- Each PWM configurable for LED blinking and breathing output
- Highly configurable breathing rate from 60ms to 1min
- Non-linear brightness curves approximated with 8 piece wise-linear segments
- All LED PWMs can be synchronized
- Each PWM configurable for 8-bit PWM support
- Multiple clock rates
- Configurable Watchdog Timer

33.2 Interface

This block is designed to drive a pin on the pin interface and to be accessed internally via a registered host interface.

37.0 GENERAL PURPOSE SERIAL PERIPHERAL INTERFACE

37.1 Overview

The General Purpose Serial Peripheral Interface (GP-SPI) may be used to communicate with various peripheral devices, e.g., EEPROMS, DACs, ADCs, that use a standard Serial Peripheral Interface.

.Characteristics of the GP-SPI Controller include:

- 8-bit serial data transmitted and received simultaneously over two data pins in Full Duplex mode with options to transmit and receive data serially on one data pin in Half Duplex (Bidirectional) mode.
- An internal programmable clock generator and clock polarity and phase controls allowing communication with various SPI peripherals with specific clocking requirements.
- SPI cycle completion that can be determined by status polling or interrupts.
- The ability to read data in on both SPDIN and SPDOUT in parallel. This allows this SPI Interface to support dual data rate read accesses for emerging double rate SPI flashes
- Support of back-to-back reads and writes without clock stretching, provided the host can read and write the data registers within one byte transaction time.

37.2 References

No references have been cited for this feature.

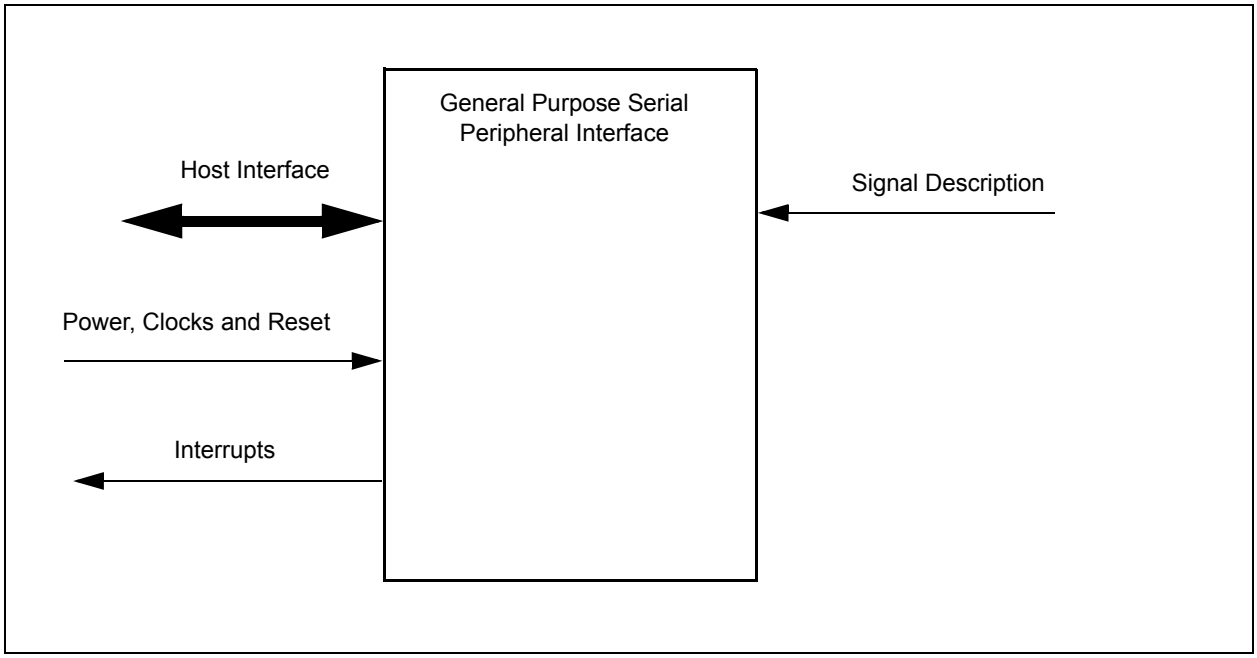
37.3 Terminology

No terminology for this block.

37.4 Interface

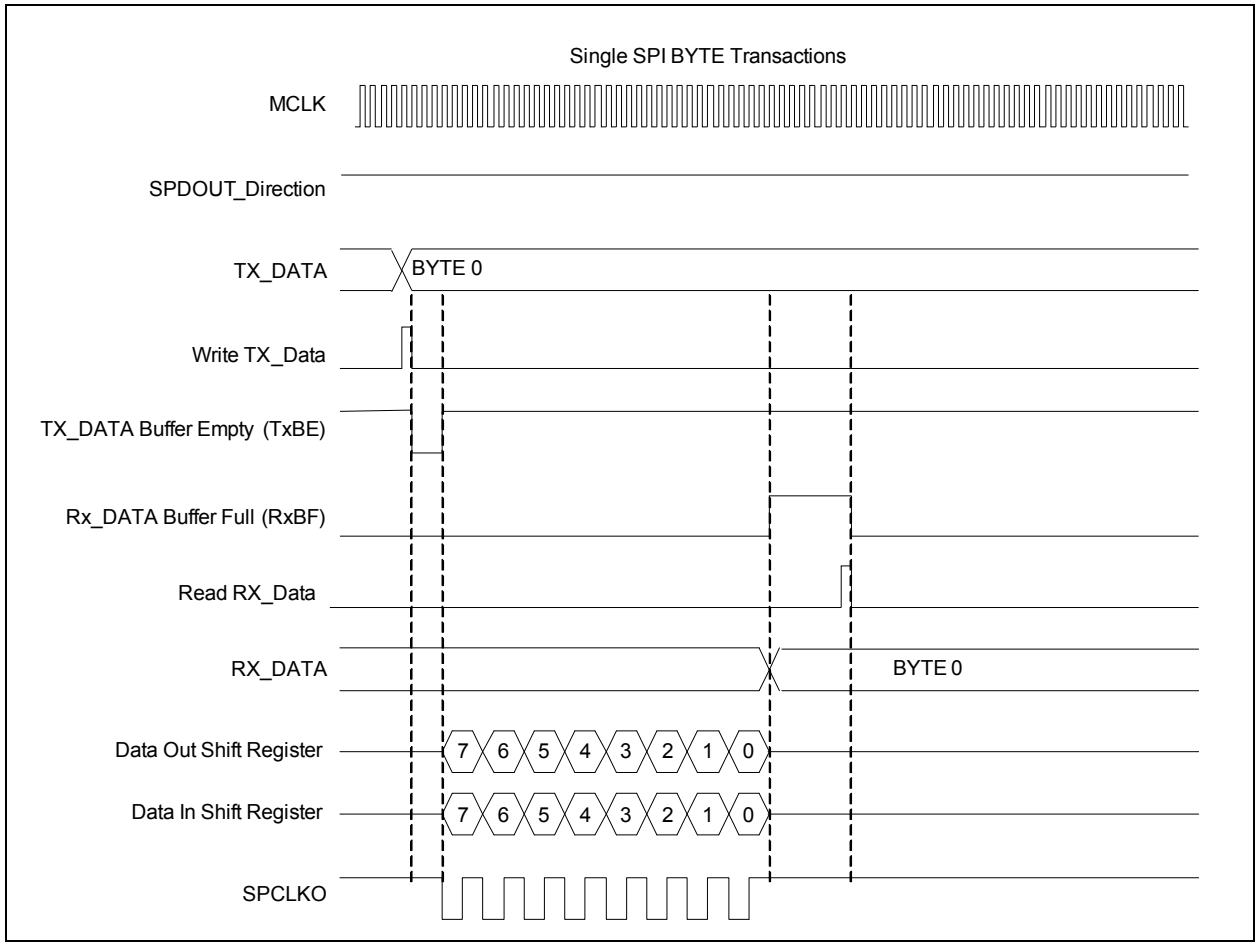
This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 37-1: I/O DIAGRAM OF BLOCK



The following diagrams show sample single byte and multi-byte SPI Transactions.

FIGURE 37-2: SINGLE BYTE SPI TX/RX TRANSACTIONS (FULL DUPLEX MODE)



39.6 Host Interface

The registers defined for the PS/2 Interface are accessible by the various hosts as indicated in Section 39.14, "EC Registers".

39.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

39.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

39.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for PS/2 Interface logic.
2 MHz Clock	The PS/2 state machine is clocked using the 2 MHz clock.

39.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

39.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
PS2_x	Interrupt request to the Interrupt Aggregator for PS2 controller instance *x*, based on PS2 controller activity. Section 39.14.4, "PS2 Status Register" defines the sources for the interrupt request.
PS2_*x*_WK	Wake-up request to the Interrupt Aggregator's wake-up interface for PS2 port *x*. In order to enable PS2 wakeup interrupts, the pin control registers for the PS2DAT pin must be programmed to Input, Falling Edge Triggered, non-inverted polarity detection.

39.9 Low Power Modes

The PS/2 Interface may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

The PS2 interface will only sleep while the PS2 is disabled or in Rx mode with no traffic on the bus.

39.10 Description

Each EC PS/2 serial channels use a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has Clock and Data signal lines. The signal lines are bi-directional and employ open drain outputs capable of sinking 12m, as required by the PS/2 specification. A pull-up resistor, typically 10K, is connected to both lines. This allows either the EC PS/2 logic or the auxiliary device to drive the lines. Regardless of the drive source, the auxiliary device always provides the clock for transmit and receive operations. The serial packet is made up of eleven bits, listed in the order they appear on the data line: start bit, eight data bits (least significant bit first), odd parity, and stop bit. Each bit cell is from 60μS to 100μS long.

All PS/2 Serial Channel signals (PS2CLK and PS2DAT) are driven by open drain drivers which can be pulled to VTR or the main power rail (+3.3V nominal) through 10K-ohm resistors.

40.0 BC-LINK MASTER

40.1 Overview

This block provides BC-Link™ connectivity to a slave device. The BC-Link™ protocol includes a start bit to signal the beginning of a message and a turnaround (TAR) period for bus transfer between the Master and Companion devices.

40.2 References

No references have been cited for this feature.

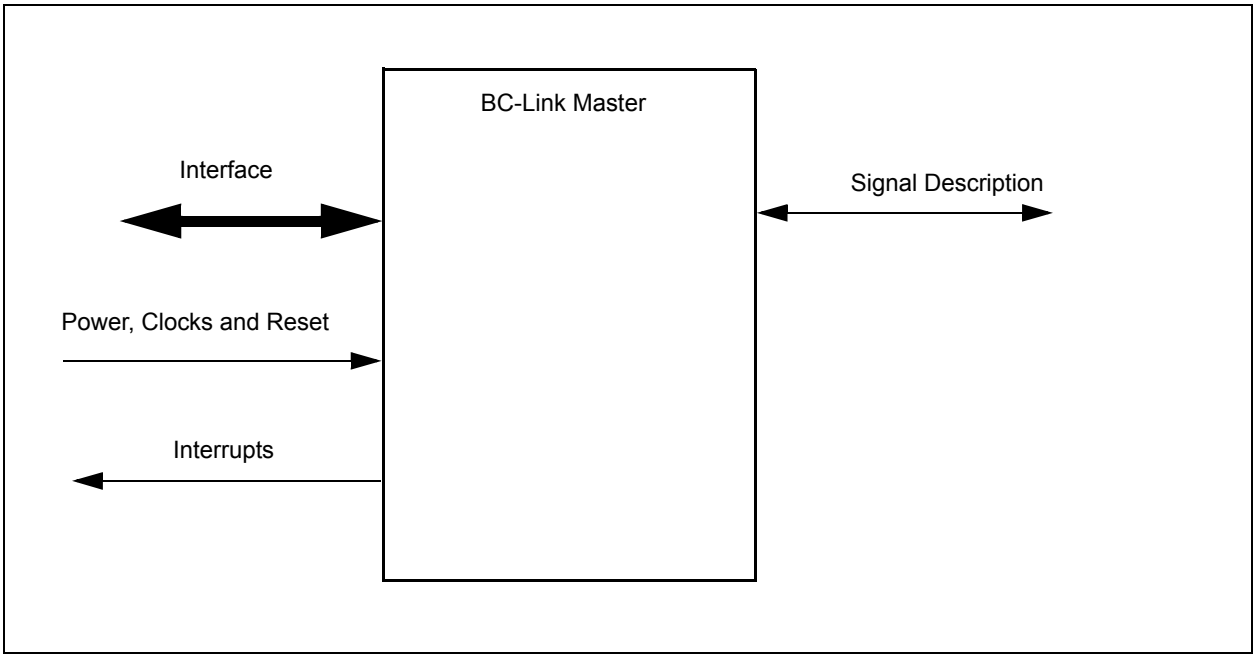
40.3 Terminology

There is no terminology defined for this section.

40.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 40-1: I/O DIAGRAM OF BLOCK



40.5 Signal Description

TABLE 40-1: SIGNAL DESCRIPTION

Name	Direction	Description
BCM_CLK	Output	BC-Link output clock
BCM_DAT	Input/Output	Bidirectional data line

Note: A weak pull-up resistor is recommended on the data line (100KW).

The maximum speed at which the BC-Link Master Interface can operate reliably depends on the drive strength of the BC-Link BCM_CLK and BCM_DAT pins, as well as the nature of the connection to the Companion device (over ribbon cable or on a PC board). The following table shows the recommended maximum speeds over a PC board as well as a 12 inch ribbon cable for selected drive strengths. The frequency is set with the BC-Link Clock Select Register.

42.6 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

42.6.1 POWER DOMAINS

Name	Description
VTR	This Power Well is used to power the registers and logic in this block.

42.6.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for Port 80 block logic.

42.6.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

42.7 Interrupts

This section defines the Interrupt Sources generated from this block.

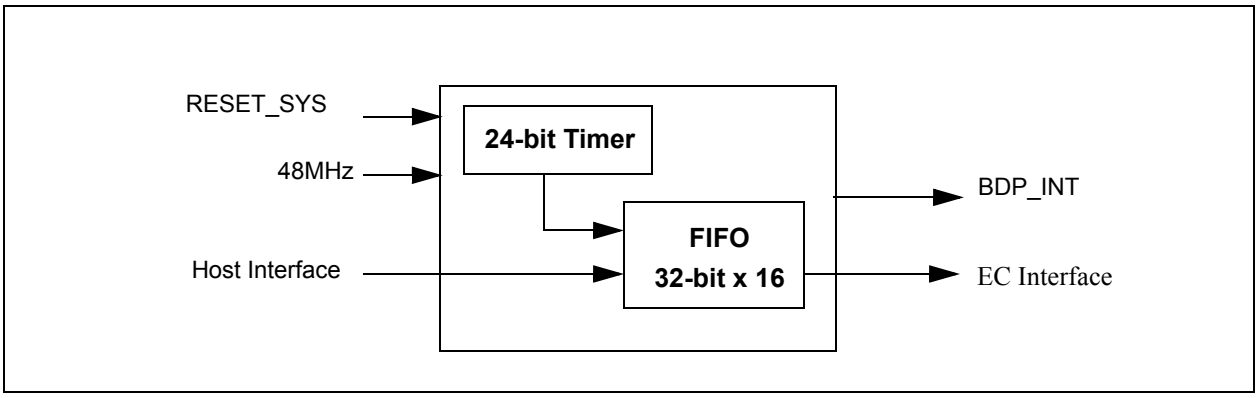
Source	Description
BDP_INT	The Port 80 BIOS Debug Port generates an EC interrupt when the amount of data in the Port 80 FIFO equals or exceeds the FIFO Threshold defined in the Configuration Register. The interrupt signal is always generated by the Port 80 block if the block is enabled; the interrupt is enabled or disabled in the Interrupt Aggregator.

42.8 Low Power Modes

The Port 80 block may be put into a low power state by the chip's Power, Clocks, and Reset (PCR) circuitry.

42.9 Description

FIGURE 42-2: PORT 80 BLOCK DIAGRAM



46.8.13 JTAG MASTER TDO REGISTER

Offset	78h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	JTM_TDO When the JTAG Master Command Register is written, from 1 to 32 bits are shifted into this register, starting with bit 0, from the JTAG_TDO pin. Shifting is at the rate determined by the JTM_-CLK field in the JTAG Master Configuration Register	R/W	0h	RESET_SYS

46.8.14 JTAG MASTER TDI REGISTER

Offset	7Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	JTM_TDI When the JTAG Master Command Register is written, from 1 to 32 bits are shifted out of this register, starting with bit 0, onto the JTAG_TDI pin. Shifting is at the rate determined by the JTM_CLK field in the JTAG Master Configuration Register	R/W	0h	RESET_SYS

46.8.15 JTAG MASTER TMS REGISTER

Offset	80h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	JTM_TMS When the JTAG Master Command Register is written, from 1 to 32 bits are shifted out of this register, starting with bit 0, onto the JTAG_TMS pin. Shifting is at the rate determined by the JTM_-CLK field in the JTAG Master Configuration Register	R/W	0h	RESET_SYS

TABLE 51-2: POWER SEQUENCING PARAMETERS (CONTINUED)

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{3b}	If VTR1=1.8V and VTR1 rises after VR_CAP assertion then: VR_CAP assertion to VTR1 above minimum operating threshold.	0		1	ms	5, 9
t_{4a}	If VTR2=3.3V or 1.8V and VTR2 rises before VR_CAP assertion then: VTR2 above minimum operating threshold to VR_CAP assertion.	0		1	ms	4, 6, 9
t_{4b}	If VTR2=1.8V and VTR2 rises after VR_CAP assertion then: VR_CAP assertion to VTR2 above minimum operating threshold.	0		1	ms	6, 9
t_{5a}	If VTR3=3.3V or 1.8V and VTR3 rises before VR_CAP assertion then: VTR3 above minimum operating threshold to VR_CAP assertion.	0		1	ms	9
t_{5b}	FOR ESPI BOOT If VTR3=1.8V and VTR3 rises after VR_CAP assertion then: VR_CAP assertion to VTR3 above minimum operating threshold.	0		30	sec	7, 9
	FOR NON-ESPI BOOT If VTR3=1.8V and VTR3 rises after VR_CAP assertion then VR_CAP assertion to VTR3 above minimum operating threshold.	0			ms	9
	FOR NON-ESPI BOOT If VTR3=3.3V and VTR3 rises after VR_CAP assertion then: VR_CAP assertion to VTR3 above minimum operating threshold.	0			ms	8, 9

Note 1: VBAT must rise no later than VTR_ANALOG and VTR_REG. This relationship is ensured by the recommended battery circuit.

2: VR_CAP output is asserted by the regulator when VR_REG is on and stable for at least the minimum defined time. All other signal timing requirements are relative to VR_CAP assertion.

3: VTR_PLL Must be connected to 3.3V VTR_ANALOG power supply.

4: VTR1 and VTR2 cannot be connected to VTR_REG for 3.3V operation. If VTR1 or VTR2 is powered by 3.3V, they must be connected to the 3.3V VTR_ANALOG supply. This is to ensure they power up before VR_CAP is asserted so that the auto voltage detection circuit that sets the bits in the GPIO Bank Power bits functions correctly.

5: The JTAG_STRAP pin is powered by VTR1 and is sampled when the RESET_EC signal goes inactive following POR event. Subsequent EC resets will not sample the JTAG_STRAP pin. VTR1 must be powered prior to RESET_EC signal going inactive.

6: The SHD_CS# pin, which is powered by VTR2, must be powered before the Boot ROM samples this pin.

7: If booting over eSPI, the EC boot ROM code monitors GPIO227/SHD_IO2, which is a VTR2 signal, to determine that VTR3 is active. The maximum time is the time after which the code abandons the boot.

8: Software must program 3.3V VTR_LEVEL3 bit in GPIO Bank Power register to 0 for 3.3V operation.

TABLE 51-19: PS/2 CHANNEL RECEIVE TIMING DIAGRAM PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	The PS/2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			1000	ns
t2	Period of CLK	60		302	µs
t3	Duration of CLK high (active)	30		151	
t4	Duration of CLK low (inactive)				
t5	DATA setup time to falling edge of CLK. MEC170x samples the data line on the falling CLK edge.	1			
t6	DATA hold time from falling edge of CLK. MEC170x samples the data line on the falling CLK edge.	2			
t7	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t8	Falling edge of 11th CLK to RDATA_RDY asserted.			1.6	µs
t9	Trailing edge of the EC's RD signal of the Receive Register to RDATA_RDY bit de-asserted.			500	ns
t10	Trailing edge of the EC's RD signal of the Receive Register to the CLK line released to high-Z.				
t11	PS2_CLK is "Low" and PS2_DATA is "Hi-Z" when PS2_EN is de-asserted.				
t12	RDATA_RDY asserted an interrupt is generated.				

51.17 PWM Timing

FIGURE 51-22: PWM OUTPUT TIMING

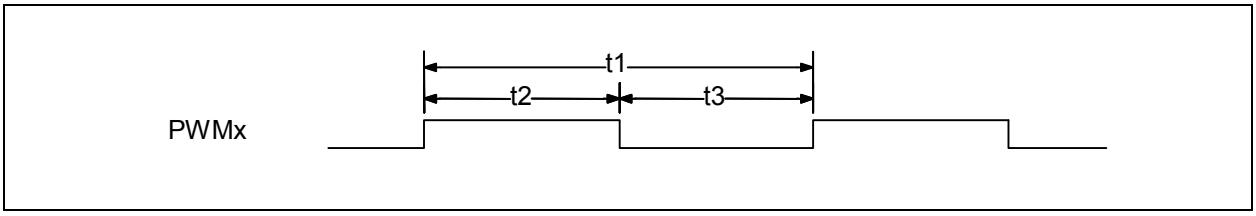


TABLE 51-20: PWM TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
t1	Period	42ns		23.3sec	
t_f	Frequency	0.04Hz		24MHz	
t2	High Time	0		11.65	sec
t3	Low Time	0		11.65	sec
t_d	Duty cycle	0		100	%