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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	ARM® Cortex®-M4
Program Memory Type	-
Controller Series	MEC170x
RAM Size	480KB
Interface	ACPI, EBI/EMI, eSPI, I²C, LPC, PECI, PS/2, QSPI, SPI
Number of I/O	123
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	144-WFBGA
Supplier Device Package	144-WFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1704q-c2-i-sz

MEC1701-169 WFBGA-TN	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
A12	GPIO047/BCM1_CLK/KSO03	VTR1	PIO	X		X	X
A13	GPIO104/UART0_TX	VTR1	PIO	X		X	X
B1	GPIO234/VCI_IN4#	VBAT	PIO	X		X	X
B2	VCI_OUT	VBAT	O2ma			X	X
B3	GPIO102/BGPO2	VBAT	PIO	X		X	X
B4	BGPO0	VBAT	O2ma	X		X	X
B5	GPIO004/I2C00_SCL/SPI0_MOSI	VTR1	PIO	X		X	X
B6	GPIO006/I2C01_SCL/GPTP-OUT7	VTR1	PIO	X		X	X
B7	GPIO165/32KHZ_IN/CTOUT0/TRACECLK	VTR1	PIO	X		X	X
B8	GPIO244	VTR1	PIO	X		X	X
B9	GPIO246	VTR1	PIO	X		X	X
B10	GPIO007/I2C03_SDA/PS2_CLK0B	VTR1	PIO	X	X	X	X
B11	GPIO157/LED1	VTR1	PIO	X	X	X	X
B12	GPIO125/GPTP-OUT5/PVT_CLK/KSO12	VTR1	PIO	X		X	X
B13	GPIO124/GPTP-OUT6/PVT_CS#/KSO11	VTR1	PIO	X		X	X
C1	GPIO033/RC_ID0	VTR1					
	GPIO033		PIO	X		X	
	RC_ID0		I_AN	X		X	
C2	GPIO000/VCI_IN3#	VBAT	PIO	X		X	X
C3	GPIO161/VCI_IN2#	VBAT	PIO	X		X	X
C4	VSS_ANALOG		PWR				
C5	GPIO101/BGPO1	VBAT	PIO	X		X	X
C6	GPIO003/I2C00_SDA/SPI0_CS#	VTR1	PIO	X		X	X
C7	GPIO147/I2C08_SDA/JTAG_CLK	VTR1	PIO	X		X	X
C8	GPIO245	VTR1	PIO	X		X	X
C9	GPIO155/I2C02_SCL/PS2_DAT1B	VTR1	PIO	X	X	X	X
C10	GPIO010/I2C03_SCL/PS2_DAT0B	VTR1	PIO	X	X	X	X
C11	GPIO133/PWM9	VTR1	PIO	X	X	X	X
C12	GPIO126/PVT_IO3/KSO13	VTR1	PIO	X		X	X
C13	GPIO123/BCM0_CLK/PVT_IO2/KSO10	VTR1	PIO	X		X	X
D1	VTR_PLL		PWR				
D2	GPIO022/GPTP-IN0	VTR1	PIO	X		X	X
D3	GPIO062/(RESETO#)	VTR1	PIO	X		X	
D4	GPIO144/I2C04_SCL/SPI1_CS#/UART0_RI#/TRACEDAT3	VTR1	PIO	X		X	X
D5	GPIO242	VTR1	PIO	X		X	X
D6	GPIO241	VTR1	PIO	X		X	X
D7	GPIO145/I2C09_SDA/JTAG_TDI	VTR1	PIO	X		X	X

Note: Gated state is only meaningful to the operation of input signals. A gated state on an output pin defines the internal behavior of the GPIO MUX and does not imply pin behavior.

Signal	Emulated Power Rail	Gated State	Notes
32KHZ_IN	VTR	Low	
32KHZ_OUT	VTR	Low	
48MHZ_OUT	VTR	Low	
A20M	VTR	Low	
ADC00	VTR	Low	
ADC01	VTR	Low	
ADC02	VTR	Low	
ADC03	VTR	Low	
ADC04	VTR	Low	
ADC05	VTR	Low	
ADC06	VTR	Low	
ADC07	VTR	Low	
ADC08	VTR	Low	
ADC09	VTR	Low	
ADC10	VTR	Low	
ADC11	VTR	Low	
ADC12	VTR	Low	
ADC13	VTR	Low	
ADC14	VTR	Low	
ADC15	VTR	Low	
BCM0_CLK	VTR	Low	
BCM0_DAT	VTR	Low	Note 3
BCM1_CLK	VTR	Low	
BCM1_DAT	VTR	Low	Note 3
BGPO0	VTR	Low	
BGPO1	VTR	Low	Note 8
BGPO2	VTR	Low	Note 8
BGPO3	VTR	Low	Note 8
BGPO4	VTR	Low	Note 8
BGPO5	VTR	Low	Note 8
CLKRUN#	VTR	High	
CTOUT0	VTR	Low	
CTOUT1	VTR	Low	
ESPI_ALERT#	VTR	High	
ESPI_CLK	VTR	Low	
ESPI_CS#	VTR	High	
ESPI_IO0	VTR	Low	
ESPI_IO1	VTR	Low	
ESPI_IO2	VTR	Low	

MEC1701/MEC1703-128 WFBGA-TF	MEC1704-144 WFBGA-SZ	MEC1705-144 WFBGA-SZ	MEC1701/MEC1703-144 WFBGA-SZ	MEC1701-169 WFBGA-TN	MEC1703-169 WFBGA-TN	MEC1703-169 WFBGA-XY	Interface		Notes
				C11	C11	C14	GPIO133	General Purpose Input/Output Port	
	E13	E13		D11	E13	G14	GPIO134	General Purpose Input/Output Port	
	G9	G9		E12	G13	G9	GPIO135	General Purpose Input/Output Port	
M13	L11	L11	L11	K13	M13	J11	GPIO140	General Purpose Input/Output Port	
A6	B7	B7	B7	A7	A7	B8	GPIO141	General Purpose Input/Output Port	
B6	F7	F7	F7	F7	A5	D8	GPIO142	General Purpose Input/Output Port	
A5	A7	A7	A7	A6	B7	A8	GPIO143	General Purpose Input/Output Port	
D8	E7	E7	E7	D4	B5	E8	GPIO144	General Purpose Input/Output Port	
A8	A8	A8	A8	D7	C8	G8	GPIO145	General Purpose Input/Output Port	
A7	G8	G8	G8	F8	D8	B9	GPIO146	General Purpose Input/Output Port	
B7	C7	C7	C7	C7	B8	D9	GPIO147	General Purpose Input/Output Port	
D9	F8	F8	F8	E7	E7	A9	GPIO150	General Purpose Input/Output Port	
J7	L9	L9	L9	H9	K9	K10	GPIO151	General Purpose Input/Output Port	
N10	N10	N10	N10	N12	M10	R13	GPIO152	General Purpose Input/Output Port	
A11			C12	E9	D10	B14	GPIO153	General Purpose Input/Output Port	
A10	A12	A12	A12	A9	A12	B13	GPIO154	General Purpose Input/Output Port	
B9	C9	C9	C9	C9	A11	E10	GPIO155	General Purpose Input/Output Port	
B12	C12	C12	A13	D9	D11	B15	GPIO156	General Purpose Input/Output Port	
A12	B13	B13	B13	B11	B12	C15	GPIO157	General Purpose Input/Output Port	
B3	C4	C4	C4	C3	D5	E5	GPIO161	General Purpose Input/Output Port	
D5	A6	A6	A6	A4	C4	A6	GPIO162	General Purpose Input/Output Port	
D6	E6	E6	E6	F6	C7	B6	GPIO163	General Purpose Input/Output Port	
B8	A9	A9	A9	B7	A8	A10	GPIO165	General Purpose Input/Output Port	
				G1	B2	E2	GPIO166	General Purpose Input/Output Port	
G10	G13	G13	G12	F11	G11	H12	GPIO170	General Purpose Input/Output Port	
G9	G12	G12	G9	E11	G9	H9	GPIO171	General Purpose Input/Output Port	
	B6	B6	B6	F5	D6	E6	GPIO172	General Purpose Input/Output Port	
				A2	C3	B5	GPIO173	General Purpose Input/Output Port	
				E4	A3	B3	GPIO174	General Purpose Input/Output Port	
D10	C13	C13	C13	D10	E10	E11	GPIO175	General Purpose Input/Output Port	
H2	H3	H3	H3	G3	G3	J2	GPIO200	General Purpose Input/Output Port	
H1	J3	J3	J3	H4	G2	K4	GPIO201	General Purpose Input/Output Port	
J2	J2	J2	J2	H3	H4	L4	GPIO202	General Purpose Input/Output Port	
J1	J1	J1	J1	K2	J1	K2	GPIO203	General Purpose Input/Output Port	

MEC1701/MEC1703-128 WFBGA-TF	MEC1704-144 WFBGA-SZ	MEC1705-144 WFBGA-SZ	MEC1701/MEC1703-144 WFBGA-SZ	MEC1701-169 WFBGA-TN	MEC1703-169 WFBGA-TN	MEC1703-169 WFBGA-XY	Interface		Notes
K1	H2	H2	H2	J3	J2	L1	GPIO204	General Purpose Input/Output Port	
K2	K3	K3	K3	L2	J4	M2	GPIO205	General Purpose Input/Output Port	
L2	L1	L1	L1	M2	K2	P1	GPIO206	General Purpose Input/Output Port	
L1	K2	K2	K2	L3	K1	N3	GPIO207	General Purpose Input/Output Port	
				H2	H3	J4	GPIO210	General Purpose Input/Output Port	
				J2	H2	H1	GPIO211	General Purpose Input/Output Port	
				K1	H1	J1	GPIO212	General Purpose Input/Output Port	
				J4	H5	K1	GPIO213	General Purpose Input/Output Port	
				J5	J3	L2	GPIO214	General Purpose Input/Output Port	
				K3	J5	N1	GPIO215	General Purpose Input/Output Port	
				K4	K3	N2	GPIO216	General Purpose Input/Output Port	
				K5	K4	P2	GPIO217	General Purpose Input/Output Port	
C1	C1	C1	C1	G7	D3	E1	GPIO221	General Purpose Input/Output Port	
	L5	L5	L5	L6	L6	L7	GPIO222	General Purpose Input/Output Port	
N5	M6	M6	M6	M7	K7	R7	GPIO223	General Purpose Input/Output Port	
M7	M5	M5	M5	N6	N3	R6	GPIO224	General Purpose Input/Output Port	
	A13	A13		A10	E9	C13	GPIO225	General Purpose Input/Output Port	
	F2	F2	F2	E3	C2	F1	GPIO226	General Purpose Input/Output Port	
M6	L6	L6	L6	N7	M4	P7	GPIO227	General Purpose Input/Output Port	
				L8	N8	R11	GPIO230	General Purpose Input/Output Port	
				K7	M7	J8	GPIO231	General Purpose Input/Output Port	
				G8	K8	L10	GPIO233	General Purpose Input/Output Port	
				B1	A1	E4	GPIO234	General Purpose Input/Output Port	
			G13	G10	G10	H14	GPIO240	General Purpose Input/Output Port	
	B8	B8	B8	D6	D9	B10	GPIO241	General Purpose Input/Output Port	
	A10	A10	A10	D5	A9	A12	GPIO242	General Purpose Input/Output Port	
	C8	C8	C8	D8	C9	E9	GPIO243	General Purpose Input/Output Port	
	A11	A11	A11	B8	B10	A13	GPIO244	General Purpose Input/Output Port	
	B11	B11	B11	C8	A10	B12	GPIO245	General Purpose Input/Output Port	
	B10	B10	B10	B9	C10	D10	GPIO246	General Purpose Input/Output Port	
	B9	B9	B9	A8	B9	B11	GPIO254	General Purpose Input/Output Port	
General Purpose Pass-Through Ports									
	E2	E2	E2	D2	F1	D2	GPTP-IN0	General Purpose Pass Through Port Input 0	
	C3	C3	C3	F4	E5	F5	GPTP-IN1	General Purpose Pass Through Port Input 1	

Feature	Instance	Logical Device Number (LDN)	Base Address
PS-2	0		4000_9000h
PS-2	1		4000_9040h
PS-2	2		4000_9080h
GP-SPI	0		4000_9400h
GP-SPI	1		4000_9480h
Hibernation Timer	0		4000_9800h
Hibernation Timer	1		4000_9820h
Keyboard Matrix Scan			4000_9C00h
RPM to PWM Fan Controller	0		4000_A000h
RPM to PWM Fan Controller	1		4000_A080h
VBAT Register Bank			4000_A400h
VBAT Powered RAM			4000_A800h
Week Timer			4000_AC80h
VBAT-Powered Control Interface			4000_AE00h
Blinking-Breathing LED	0		4000_B800h
Blinking-Breathing LED	1		4000_B900h
Blinking-Breathing LED	2		4000_BA00h
Blinking-Breathing LED	3		4000_BB00h
BC-Link Master	0		4000_CD00h
BC-Link Master	1		4000_CD20h
Interrupt Aggregator			4000_E000h
EC Subsystem Registers			4000_FC00h
JTAG			4008_0000h
Power, Clocks and Resets			4008_0100h
GPIOs			4008_1000h
eFuse			4008_2000h
Mailbox		0h	400F_0000h
8042 Emulated Keyboard Controller		1h	400F_0400h
ACPI EC Channel	0	2h	400F_0800h
ACPI EC Channel	1	3h	400F_0C00h
ACPI EC Channel	2	4h	400F_1000h
ACPI EC Channel	3	5h	400F_1400h
ACPI EC Channel	4	6h	400F_1800h
ACPI PM1		7h	400F_1C00h
Port 92-Legacy		8h	400F_2000h
UART	0	9h	400F_2400h
UART	1	Ah	400F_2800h
LPC Interface		Ch	400F_3000h
eSPI Interface IO Component	Note 1	Dh	400F_3400h
eSPI Interface Memory Component	Note 1	Eh	400F_3800h
Embedded Memory Interface (EMI)	0	10h	400F_4000h
Embedded Memory Interface (EMI)	1	11h	400F_4400h
Note 1: The eSPI block occupies two logical devices, Dh and Eh			

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ10	0	GPIO040	GPIO Event	Yes	GPIO Interrupt Event	2	N/A
	1	GPIO041	GPIO Event	Yes	GPIO Interrupt Event		
	2	GPIO042	GPIO Event	Yes	GPIO Interrupt Event		
	3	GPIO043	GPIO Event	Yes	GPIO Interrupt Event		
	4	GPIO044	GPIO Event	Yes	GPIO Interrupt Event		
	5	GPIO045	GPIO Event	Yes	GPIO Interrupt Event		
	6	GPIO046	GPIO Event	Yes	GPIO Interrupt Event		
	7	GPIO047	GPIO Event	Yes	GPIO Interrupt Event		
	8	GPIO050	GPIO Event	Yes	GPIO Interrupt Event		
	9	GPIO051	GPIO Event	Yes	GPIO Interrupt Event		
	10	GPIO052	GPIO Event	Yes	GPIO Interrupt Event		
	11	GPIO053	GPIO Event	Yes	GPIO Interrupt Event		
	12	GPIO054	GPIO Event	Yes	GPIO Interrupt Event		
	13	GPIO055	GPIO Event	Yes	GPIO Interrupt Event		
	14	GPIO056	GPIO Event	Yes	GPIO Interrupt Event		
	15	GPIO057	GPIO Event	Yes	GPIO Interrupt Event		
	16	GPIO060	GPIO Event	Yes	GPIO Interrupt Event		
	17	GPIO061	GPIO Event	Yes	GPIO Interrupt Event		
	18	GPIO062	GPIO Event	Yes	GPIO Interrupt Event		
	19	GPIO063	GPIO Event	Yes	GPIO Interrupt Event		
	20	GPIO064	GPIO Event	Yes	GPIO Interrupt Event		
	21	GPIO065	GPIO Event	Yes	GPIO Interrupt Event		
	22	GPIO066	GPIO Event	Yes	GPIO Interrupt Event		
	23	GPIO067	GPIO Event	Yes	GPIO Interrupt Event		
	24	GPIO070	GPIO Event	Yes	GPIO Interrupt Event		
	25	GPIO071	GPIO Event	Yes	GPIO Interrupt Event		
	26	GPIO072	GPIO Event	Yes	GPIO Interrupt Event		
	27	GPIO073	GPIO Event	Yes	GPIO Interrupt Event		
	28	Reserved	-	-			
	29	Reserved	-	-			
	30	Reserved	-	-			
	31	Reserved					

Agg IRQ	Agg Bit	HWB Instance Name	Interrupt Event	Wake Event	Source Description	Agg NVIC	Direct NVIC
GIRQ25	0	eSPI_Slave	MSVW07_SRC0	Yes	M-to-S VW Interrupt Event	16	N/A
	1	eSPI_Slave	MSVW07_SRC1	Yes	M-to-S VW Interrupt Event		
	2	eSPI_Slave	MSVW07_SRC2	Yes	M-to-S VW Interrupt Event		
	3	eSPI_Slave	MSVW07_SRC3	Yes	M-to-S VW Interrupt Event		
	4	eSPI_Slave	MSVW08_SRC0	Yes	M-to-S VW Interrupt Event		
	5	eSPI_Slave	MSVW08_SRC1	Yes	M-to-S VW Interrupt Event		
	6	eSPI_Slave	MSVW08_SRC2	Yes	M-to-S VW Interrupt Event		
	7	eSPI_Slave	MSVW08_SRC3	Yes	M-to-S VW Interrupt Event		
	8	eSPI_Slave	MSVW09_SRC0	Yes	M-to-S VW Interrupt Event		
	9	eSPI_Slave	MSVW09_SRC1	Yes	M-to-S VW Interrupt Event		
	10	eSPI_Slave	MSVW09_SRC2	Yes	M-to-S VW Interrupt Event		
	11	eSPI_Slave	MSVW09_SRC3	Yes	M-to-S VW Interrupt Event		
	12	eSPI_Slave	MSVW10_SRC0	Yes	M-to-S VW Interrupt Event		
	13	eSPI_Slave	MSVW10_SRC1	Yes	M-to-S VW Interrupt Event		
	14	eSPI_Slave	MSVW10_SRC2	Yes	M-to-S VW Interrupt Event		
	15	eSPI_Slave	MSVW10_SRC3	Yes	M-to-S VW Interrupt Event		
	16-31	Reserved					

Block	Instance	Register	Register Address
PS2	1	PS2 Control Register	40009044h
PS2	1	PS2 Status Register	40009048h
PS2	2	PS2 Transmit Buffer Register	40009080h
PS2	2	PS2 Receive Buffer Register	40009080h
PS2	2	PS2 Control Register	40009084h
PS2	2	PS2 Status Register	40009088h
GP-SPI	0	SPI Enable Register	40009400h
GP-SPI	0	SPI Control Register	40009404h
GP-SPI	0	SPI Status Register	40009408h
GP-SPI	0	SPI TX_Data Register	4000940Ch
GP-SPI	0	SPI RX_Data Register	40009410h
GP-SPI	0	SPI Clock Control Register	40009414h
GP-SPI	0	SPI Clock Generator Register	40009418h
GP-SPI	0	TESET	40009420h
GP-SPI	1	SPI Enable Register	40009480h
GP-SPI	1	SPI Control Register	40009484h
GP-SPI	1	SPI Status Register	40009488h
GP-SPI	1	SPI TX_Data Register	4000948Ch
GP-SPI	1	SPI RX_Data Register	40009490h
GP-SPI	1	SPI Clock Control Register	40009494h
GP-SPI	1	SPI Clock Generator Register	40009498h
GP-SPI	1	TESET	400094A0h
Hibernation Timer	0	HTimer Preload Register	40009800h
Hibernation Timer	0	HTimer Control Register	40009804h
Hibernation Timer	0	HTimer Count Register	40009808h
Hibernation Timer	1	HTimer Preload Register	40009820h
Hibernation Timer	1	HTimer Control Register	40009824h
Hibernation Timer	1	HTimer Count Register	40009828h
Keyscan	0	KSO Select Register	40009C04h
Keyscan	0	KSI INPUT Register	40009C08h
Keyscan	0	KSI STATUS Register	40009C0Ch
Keyscan	0	KSI INTERRUPT ENABLE Register	40009C10h
Keyscan	0	Keyscan Extended Control Register	40009C14h
RPM2PWM	0	Fan Setting Register	4000A000h
RPM2PWM	0	PWM Divide Register	4000A001h
RPM2PWM	0	Fan Configuration 1 Register	4000A002h
RPM2PWM	0	Fan Configuration 2 Register	4000A003h
RPM2PWM	0	Reserved	4000A004h
RPM2PWM	0	Gain Register	4000A005h
RPM2PWM	0	Fan Spin Up Configuration Register	4000A006h
RPM2PWM	0	Fan Step Register	4000A007h
RPM2PWM	0	Fan Minimum Drive Register	4000A008h
RPM2PWM	0	Valid TACH Count Register	4000A009h

Block	Instance	Register	Register Address
ACPI EC Channel	1	EC2OS Data EC Byte 3 Register	400F0D03h
ACPI EC Channel	1	EC STATUS Register	400F0D04h
ACPI EC Channel	1	EC Byte Control Register	400F0D05h
ACPI EC Channel	1	Reserved	400F0D06h
ACPI EC Channel	1	Reserved	400F0D07h
ACPI EC Channel	1	OS2EC Data EC Byte 0 Register	400F0D08h
ACPI EC Channel	1	OS2EC Data EC Byte 1 Register	400F0D09h
ACPI EC Channel	1	OS2EC Data EC Byte 2 Register	400F0D0Ah
ACPI EC Channel	1	OS2EC Data EC Byte 3 Register	400F0D0Bh
ACPI EC Channel	2	ACPI OS Data Register Byte 0 Register	400F1000h
ACPI EC Channel	2	ACPI OS Data Register Byte 1 Register	400F1001h
ACPI EC Channel	2	ACPI OS Data Register Byte 2 Register	400F1002h
ACPI EC Channel	2	ACPI OS Data Register Byte 3 Register	400F1003h
ACPI EC Channel	2	ACPI OS COMMAND Register	400F1004h
ACPI EC Channel	2	OS STATUS OS Register	400F1004h
ACPI EC Channel	2	OS Byte Control Register	400F1005h
ACPI EC Channel	2	Reserved	400F1006h
ACPI EC Channel	2	Reserved	400F1007h
ACPI EC Channel	2	EC2OS Data EC Byte 0 Register	400F1100h
ACPI EC Channel	2	EC2OS Data EC Byte 1 Register	400F1101h
ACPI EC Channel	2	EC2OS Data EC Byte 2 Register	400F1102h
ACPI EC Channel	2	EC2OS Data EC Byte 3 Register	400F1103h
ACPI EC Channel	2	EC STATUS Register	400F1104h
ACPI EC Channel	2	EC Byte Control Register	400F1105h
ACPI EC Channel	2	Reserved	400F1106h
ACPI EC Channel	2	Reserved	400F1107h
ACPI EC Channel	2	OS2EC Data EC Byte 0 Register	400F1108h
ACPI EC Channel	2	OS2EC Data EC Byte 1 Register	400F1109h
ACPI EC Channel	2	OS2EC Data EC Byte 2 Register	400F110Ah
ACPI EC Channel	2	OS2EC Data EC Byte 3 Register	400F110Bh
ACPI EC Channel	3	ACPI OS Data Register Byte 0 Register	400F1400h
ACPI EC Channel	3	ACPI OS Data Register Byte 1 Register	400F1401h
ACPI EC Channel	3	ACPI OS Data Register Byte 2 Register	400F1402h
ACPI EC Channel	3	ACPI OS Data Register Byte 3 Register	400F1403h
ACPI EC Channel	3	ACPI OS COMMAND Register	400F1404h
ACPI EC Channel	3	OS STATUS OS Register	400F1404h
ACPI EC Channel	3	OS Byte Control Register	400F1405h
ACPI EC Channel	3	Reserved	400F1406h
ACPI EC Channel	3	Reserved	400F1407h
ACPI EC Channel	3	EC2OS Data EC Byte 0 Register	400F1500h
ACPI EC Channel	3	EC2OS Data EC Byte 1 Register	400F1501h
ACPI EC Channel	3	EC2OS Data EC Byte 2 Register	400F1502h
ACPI EC Channel	3	EC2OS Data EC Byte 3 Register	400F1503h

Block	Instance	Register	Register Address
EMI	1	EC Address LSB Register	400F4402h
EMI	1	EC Address MSB Register	400F4403h
EMI	1	EC Data Byte 0 Register	400F4404h
EMI	1	EC Data Byte 1 Register	400F4405h
EMI	1	EC Data Byte 2 Register	400F4406h
EMI	1	EC Data Byte 3 Register	400F4407h
EMI	1	Interrupt Source LSB Register	400F4408h
EMI	1	Interrupt Source MSB Register	400F4409h
EMI	1	Interrupt Mask LSB Register	400F440Ah
EMI	1	Interrupt Mask MSB Register	400F440Bh
EMI	1	Application ID Register	400F440Ch
EMI	1	HOST-to-EC Mailbox Register	400F4500h
EMI	1	EC-to-HOST Mailbox Register	400F4501h
EMI	1	Memory Base Address 0 Register	400F4504h
EMI	1	Memory Read Limit 0 Register	400F4508h
EMI	1	Memory Write Limit 0 Register	400F450Ah
EMI	1	Memory Base Address 1 Register	400F450Ch
EMI	1	Memory Read Limit 1 Register	400F4510h
EMI	1	Memory Write Limit 1 Register	400F4512h
EMI	1	Interrupt Set Register	400F4514h
EMI	1	Host Clear Enable Register	400F4516h
EMI	2	HOST-to-EC Mailbox Register	400F4800h
EMI	2	EC-to-HOST Mailbox Register	400F4801h
EMI	2	EC Address LSB Register	400F4802h
EMI	2	EC Address MSB Register	400F4803h
EMI	2	EC Data Byte 0 Register	400F4804h
EMI	2	EC Data Byte 1 Register	400F4805h
EMI	2	EC Data Byte 2 Register	400F4806h
EMI	2	EC Data Byte 3 Register	400F4807h
EMI	2	Interrupt Source LSB Register	400F4808h
EMI	2	Interrupt Source MSB Register	400F4809h
EMI	2	Interrupt Mask LSB Register	400F480Ah
EMI	2	Interrupt Mask MSB Register	400F480Bh
EMI	2	Application ID Register	400F480Ch
EMI	2	HOST-to-EC Mailbox Register	400F4900h
EMI	2	EC-to-HOST Mailbox Register	400F4901h
EMI	2	Memory Base Address 0 Register	400F4904h
EMI	2	Memory Read Limit 0 Register	400F4908h
EMI	2	Memory Write Limit 0 Register	400F490Ah
EMI	2	Memory Base Address 1 Register	400F490Ch
EMI	2	Memory Read Limit 1 Register	400F4910h
EMI	2	Memory Write Limit 1 Register	400F4912h
EMI	2	Interrupt Set Register	400F4914h

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	PWR_INV This bit allows firmware to control when the Host receives an indication that the VCC power is valid, by controlling the state of the PWROK pin. This bit is used by firmware to control the internal RESET_VCC signal function and the external PWROK pin. This bit is read-only when VCC_PWRGD is de-asserted low. The internal RESET_VCC signal is asserted when this bit is asserted even if the PWROK pin is configured as an alternate function.	R / R/W	1h	RESET_SYS

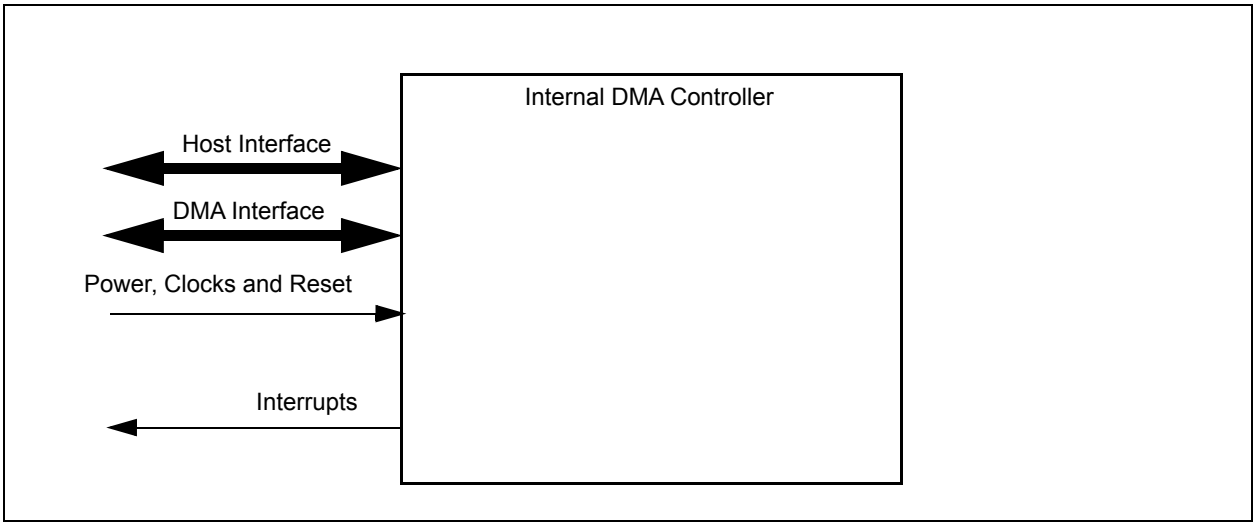
4.9.10 SYSTEM RESET REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:9	Reserved	R	-	-
8	SOFT_SYS_RESET A write of a ‘1’ to this bit will force an assertion of the RESET_SYS reset signal, resetting the device. A write of a ‘0’ has no effect. Reads always return ‘0’.	W	-	-
7:0	Reserved	R	-	-

7.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 7-1: INTERNAL DMA CONTROLLER I/O DIAGRAM



7.4.1 SIGNAL DESCRIPTION

This block doesn't have any external signals that may be routed to the pin interface. This DMA Controller is intended to be used internally to transfer large amounts of data without the embedded controller being actively involved in the transfer.

7.4.2 HOST INTERFACE

The registers defined for the Internal DMA Controller are accessible by the various hosts as indicated in Section 7.9, "EC Registers".

7.4.3 DMA INTERFACE

Each DMA Master Device that may engage in a DMA transfer must have a compliant DMA interface. The following table lists the DMA Devices in the MEC170x.

TABLE 7-2: DMA CONTROLLER DEVICE SELECTION

Device Name	Device Number (Note 1)	Controller Source
SMB-I2C 0 Controller	0	Slave
	1	Master
SMB-I2C 1 Controller	2	Slave
	3	Master
SMB-I2C 2 Controller	4	Slave
	5	Master
SMB-I2C 3 Controller	6	Slave
	7	Master
SPI 0 Controller	8	Transmit
	9	Receive
SPI 1 Controller	10	Transmit
	11	Receive

Note 1: The Device Number is programmed into field HARDWARE_FLOW_CONTROL_DEVICE of the DMA Channel N Control Register register.

TABLE 7-3: DMA CONTROLLER MASTER DEVICES SIGNAL LIST (CONTINUED)

Device Name	Dev Num	Device Signal Name	Direction	Description
SMB-I2C 3 Controller	6	SMB-I2C_SDMA_Req	INPUT	DMA request control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Term	INPUT	DMA termination control from SMB-I2C Slave channel.
		SMB-I2C_SDMA_Done	OUTPUT	DMA termination control from DMA Controller to Slave channel.
	7	SMB-I2C_MDMA_Req	INPUT	DMA request control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Term	INPUT	DMA termination control from SMB-I2C Master channel.
		SMB-I2C_MDMA_Done	OUTPUT	DMA termination control from DMA Controller to Master channel.
SPI 0 Controller	8	SPI_TDMA_Req	INPUT	DMA request control from GP-SPI TX channel.
	9	SPI_RDMA_Req	INPUT	DMA request control from GP-SPI RX channel.
SPI 1 Controller	10	SPI_TDMA_Req	INPUT	DMA request control from GP-SPI TX channel.
	11	SPI_RDMA_Req	INPUT	DMA request control from GP-SPI RX channel.
Quad SPI Controller	12	QSPI_TDMA_Req	INPUT	DMA request control from Quad SPI TX channel.
	13	QSPI_RDMA_Req	INPUT	DMA request control from Quad SPI RX channel.

7.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

7.5.1 POWER DOMAINS

TABLE 7-4: POWER SOURCES

Name	Description
VTR	This power well sources the registers and logic in this block.

7.5.2 CLOCK INPUTS

TABLE 7-5: CLOCK INPUTS

Name	Description
48MHz	This clock signal drives selected logic (e.g., counters).

7.5.3 RESETS

TABLE 7-6: RESET SIGNALS

Name	Description
RESET_SYS	This reset signal resets all of the registers and logic in this block.
RESET	This reset is generated if either the RESET_SYS is asserted or the SOFT_RESET bit is asserted.

12.14.2 EC_HOST DATA / AUX DATA REGISTER

Offset	0h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	READ_DATA This 8-bit register is read-only. When read by the Host, the PCOBF and/or AUXOBF interrupts are cleared and the OBF flag in the status register is cleared.	R	0h	RESET_SYS

12.14.3 KEYBOARD STATUS READ REGISTER

This register is a read-only alias of the EC Keyboard Status Register.

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	UD2 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R	0h	RESET_SYS
5	AUXOBF Auxiliary Output Buffer Full. This bit is set to “1” whenever the EC writes the EC AUX Data Register. This flag is reset to “0” whenever the EC writes the EC Data Register.	R	0h	RESET_SYS
4	UD1 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R	0h	RESET_SYS
3	C/D Command Data. This bit specifies whether the input data register contains data or a command (“0” = data, “1” = command). During a Host command write operation (when the Host writes the HOST_EC Data / CMD Register at offset 04h), this bit is set to “1”. During a Host data write operation (when the Host writes the HOST_EC Data / CMD Register at offset 0h), this bit is set to “0”.	R	0h	RESET_SYS
2	UD0 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R	0h	RESET_HOST
1	IBF Input Buffer Full. This bit is set to “1” whenever the Host writes data or a command into the HOST_EC Data / CMD Registerr. When this bit is set, the EC's IBF interrupt is asserted, if enabled. When the EC reads the HOST_EC Data/CMD Register, this bit is automatically reset and the interrupt is cleared. This bit is not reset on RESET_VCC. To clear this bit, firmware must read the HOST2EC Data Register in the EC-Only address space.	R	0h	RESET_SYS

Offset	See Section 18.8			
Bits	**Description**	**Type**	**Default**	**Reset Event**
23:17	Reserved	R	-	-
16	ALTERNATE_GPIO_DATA Reads of this bit always return the last data written to the GPIO output data register bit; reads do not return the current output value of the GPIO pin if it is configured as an output. If the GPIO_OUTPUT_SELECT bit in this register is '1', then this bit is Read Only and the GPIO output data register bit is only written by the GPIO Output Register. If the GPIO_OUTPUT_SELECT bit in this register is '0', then this bit is R/W, and the bit corresponding to this GPIO in the GPIO Output Register is Read Only.	R or R/W	See Section 18.8	RESET_SYS
15:14	Reserved	R	-	-
13:12	MUX_CONTROL The Mux Control field determines the active signal function for a pin. 11b=Signal Function 3 Selected 10b=Signal Function 2 Selected 01b=Signal Function 1 Selected 00b=GPIO Function Selected	R/W	See Section 18.8	RESET_SYS
11	POLARITY When the Polarity bit is set to '1' and the MUX_CONTROL bits are greater than '00,' the selected signal function outputs are inverted and Interrupt Detection sense defined in Table 18-6, "Edge Enable and Interrupt Detection Bits Definition" is inverted. When the MUX_CONTROL field selects the GPIO signal function (Mux='00'), the Polarity bit does not effect the output. Regardless of the state of the MUX_CONTROL field and the Polarity bit, the state of the pin is always reported without inversion in the GPIO input register. 1=Inverted 0=Non-inverted	R/W	See Section 18.8	RESET_SYS
10	GPIO_OUTPUT_SELECT This control bit determines which register is used to update the data register for GPIO outputs. See Section 18.4, "Description" 1=GPIO output data for this GPIO come from the bit representing this GPIO in the GPIO Output Register; writes to the ALTERNATE_GPIO_DATA field of this register do not affect the GPIO 0=GPIO output data for this GPIO come from the ALTERNATE_GPIO_DATA field of this register; writes to the bit representing this GPIO in the GPIO Output Register do not affect the GPIO	R/W	See Section 18.8	RESET_SYS
9	GPIO_DIRECTION This bit controls the buffer direction only when the MUX_CONTROL field is '00' selecting the pin signal function to be GPIO. When the MUX_CONTROL field is greater than '00' (i.e., a non-GPIO signal function is selected) this bit has no affect and the selected signal function logic directly controls the pin direction. 1=Output 0=Input	R/W	See Section 18.8	RESET_SYS

22.12.10 CAPTURE 5 REGISTER

Offset	24h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	CAPTURE_5 This register saves the value copied from the Free Running timer on a programmed edge of ICT5.	R	0h	RESET_SYS

22.12.11 COMPARE 0 REGISTER

Offset	28h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COMPARE_0 A COMPARE 0 interrupt is generated when this register matches the value in the Free Running Timer.	R/W	0h	RESET_SYS

22.12.12 COMPARE 1 REGISTER

Offset	2Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:0	COMPARE_1 A COMPARE 1 interrupt is generated when this register matches the value in the Free Running Timer.	R/W	0h	RESET_SYS

26.9.1 INTERNAL COUNTERS

The Week Timer includes 3 counters:

26.9.1.1 28-bit Week Alarm Counter

This counter is 28 bits wide. The clock for this counter is the overflow of the Clock Divider, and as long as the Week Timer is enabled, it is incremented at a 1 Hz rate.

Both an interrupt and a power-up event can be generated when the contents of this counter matches the contents of the Week Timer Compare Register.

26.9.1.2 9-bit Sub-Week Alarm Counter

This counter is 9 bits wide. It is decremented by 1 at each tick of its selected clock. It can be configured either as a one-shot or repeating event generator.

Both an interrupt and a power-up event can be generated when this counter decrements from 1 to 0.

The Sub-Week Alarm Counter can be configured with a number of different clock sources for its time base, derived from either the Week Alarm Counter or the Clock Divider, by setting the SUBWEEK_TICK field of the Sub-Week Control Register.

TABLE 26-7: SUB-WEEK ALARM COUNTER CLOCK

SUBWEEK_ TICK	Source	SPISR	Frequency	Minimum Duration	Maximum Duration
0	Counter Disabled				
1	Sub-Second	0	Counter Disabled		
		1	2 Hz	500 ms	255.5 sec
		2	4 Hz	250 ms	127.8 sec
		3	8 Hz	125 ms	63.9 sec
		4	16 Hz	62.5	31.9 sec
		5	32 Hz	31.25 ms	16.0 sec
		6	64 Hz	15.6 ms	8 sec
		7	128 Hz	7.8 ms	4 sec
		8	256 Hz	3.9 ms	2 sec
		9	512 Hz	1.95 ms	1 sec
		10	1024 Hz	977 µS	499 ms
		11	2048 Hz	488 µS	249.5 ms
		12	4096 Hz	244 µS	124.8 ms
		13	8192 Hz	122 µS	62.4 ms
		14	16.384 KHz	61.1 µS	31.2 ms
		15	32.768 KHz	30.5 µS	15.6 ms
2	Second	n/a	1 Hz	1 sec	511 sec
3	Reserved				
4	Week Counter bit 3	n/a	125 Hz	8 sec	68.1 min
5	Week Counter bit 5	n/a	31.25 Hz	32 sec	272.5 min
6	Week Counter bit 7	n/a	7.8125 Hz	128 sec	18.17 hour
7	Week Counter bit 9	n/a	1.95 Hz	512 sec	72.68 hour

TABLE 26-9: SPISR ENCODING (CONTINUED)

SPISR Value	Sub-Second Interrupt Rate, Hz	Interrupt Period
4	16	62.5 ms
5	32	31.25 ms
6	64	15.63 ms
7	128	7.813 ms
8	256	3.906 ms
9	512	1.953 ms
10	1024	977 µS
11	2048	488 µS
12	4096	244 µS
13	8192	122 µS
14	16384	61 µS
15	32768	30.5 µS

26.11.6 SUB-WEEK CONTROL REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	Reserved	R	-	-
9:7	SUBWEEK_TICK This field selects the clock source for the Sub-Week Counter. See Table 26-7, "Sub-Week Alarm Counter Clock" for the description of the options for this field. See also Note 1.	R/W	0	RESET_VBAT
6	AUTO_RELOAD 1= No reload occurs when the Sub-Week Counter expires 0= Reloads the SUBWEEK_COUNTER_LOAD field into the Sub-Week Counter when the counter expires.	R/W	0	RESET_VBAT
5	TEST Must always be written with 0.	R/W	0	-
4:2	Reserved	R	-	-

26.11.8 BGPO DATA REGISTER

Offset	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:10	Reserved	R	-	-
9:0	BGPO Battery powered General Purpose Output. Each output pin may be individually configured to be either a VBAT-power BGPO or a VTR-powered GPIO, based on the corresponding settings in the BGPO Power Register. Additionally, each output pin may be individually configured to reset to 0 on either RESET_VBAT or RESET_SYS, based on the corresponding settings in the BGPO Reset Register. For each bit [*i*] in the field: 1=BGPO[*i*] output is high 0=BGPO[*i*] output is low If a BGPO[*i*] does not appear in a package, the corresponding bit **must** be written with a 0 or undesirable results will occur.	R/W	0h	RESET_VBAT or RESET_SYS

26.11.9 BGPO POWER REGISTER

Offset	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:6	Reserved	R	-	-
5:1	BGPO_POWER Battery powered General Purpose Output power source. For each bit [*i*] in the field: 1=BGPO[*i*] is powered by VBAT. The BGPO[*i*] pin is always determined by the corresponding bit in the BGPO Data Register. The GPIO Input register for the GPIO that is multiplexed with the BGPO always returns a ‘1b’. 0=The pin for BGPO[*i*] functions as a GPIO. When VTR is powered, the pin associated with BGPO[*i*] is determined by the GPIO associated with the pin. When VTR is unpowered, the pin is tri-stated	R/W	1Fh	RESET_VBAT
0	Reserved	R	-	-

Note: Because BGPO[9:6] and BGPO0 are not multiplexed with GPIOs, bits 9:6 and 0 are reserved.

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	UPDATE_INTERVAL1 The number of PWM periods between updates to current duty cycle when the segment index is equal to 001b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS
3:0	UPDATE_INTERVAL0 The number of PWM periods between updates to current duty cycle when the segment index is equal to 000b. 15=Wait 16 PWM periods … 0=Wait 1 PWM period	R/W	0h	RESET_SYS

33.10.6 LED OUTPUT DELAY

This register permits the transitions for multiple blinking/breathing LED outputs to be skewed, so as not to present too great a current load. The register defines a count for the number of clocks the circuitry waits before turning on the output, either on initial enable, after a resume from Sleep, or when multiple outputs are synchronized through the Sync control in the LED CONFIGURATION (LED_CFG) register.

When more than one LED outputs are used simultaneously, the LED OUTPUT DELAY fields of each should be configured with different values so that the outputs are skewed. When used with the 32KHz clock domain as a clock source, the differences can be as small as 1.

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	OUTPUT_DELAY The delay, in counts of the clock defined in Clock Source (CLKSRC), in which output transitions are delayed. When this field is 0, there is no added transition delay. When the LED is programmed to be Always On or Always Off, the Output Delay field has no effect.	R/W	000h	RESET_SYS