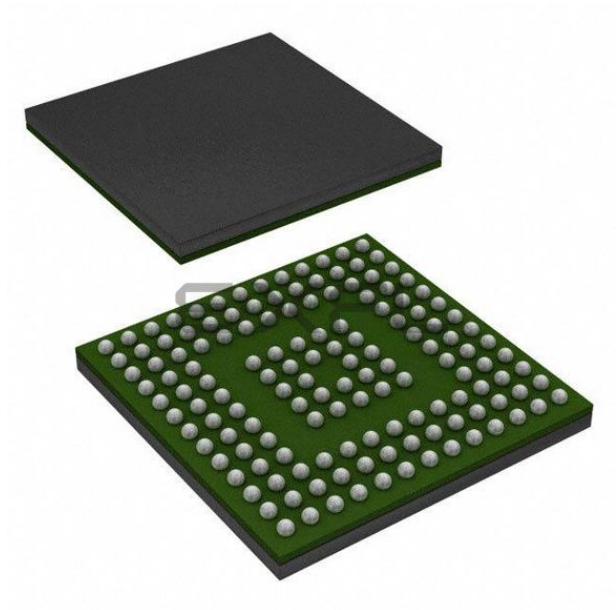


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	ARM® Cortex®-M4
Program Memory Type	-
Controller Series	MEC170x
RAM Size	480KB
Interface	ACPI, EBI/EMI, eSPI, I²C, LPC, PECI, PS/2, QSPI, SPI
Number of I/O	123
Voltage - Supply	1.71V ~ 3.465V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	144-WFBGA
Supplier Device Package	144-WFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/mec1705q-c1-i-sz

MEC1705/MEC1704-144-SZ	MEC1701/MEC1703-144-SZ	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
F13	F13	GPIO047/BCM1_CLK/KSO03	VTR1	PIO	X		X	X
G1	G1	VTR_REG		PWR				
G2	G2	VREF_ADC		PWR			X	
G3	G3	VSS2		PWR				
G5	G5	VTR1		PWR				
G6	G6	VTR_ANALOG		PWR				
G8	G8	GPIO146/I2C09_SCL/JTAG_TDO	VTR1	PIO	X		X	X
G9		GPIO135/UART1_CTS#	VTR1	PIO	X		X	X
	G9	GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)	VTR1	PIO	X		X	X
G11	G11	JTAG_RST#	VTR1	In	X		X	X
G12		GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)	VTR1	PIO	X		X	X
G13	G12	GPIO170/TFCLK/UART1_TX	VTR1	PIO	X		X	X
	G13	GPIO240	VTR1	PIO	X		X	X
H1	H1	VR_CAP		PWR				
H2	H2	GPIO204/ADC04	VTR1					
		GPIO204		PIO	X		X	
		ADC04		I_AN	X		X	
H3	H3	GPIO200/ADC00	VTR1					
		GPIO200		PIO	X		X	
		ADC00		I_AN	X		X	
H5	H5	VSS3		PWR				
H6	H6	VTR3		PWR				
H7	H7	GPIO100/nEC_SCI	VTR3	PIO	X		X	X
H8	H8	VTR2		PWR				
H9	H9	GPIO114/PS2_CLK0A/nEC_SCI	VTR2	PIO	X		X	X
H11	H11	GPIO044/VREF_VTT	VTR1					
		GPIO044		PIO	X		X	
		VREF_VTT		I_AN	X		X	
H12	H12	GPIO034/RC_ID1/SPI0_CLK	VTR1					
		GPIO034,SPI0_CLK		PIO	X		X	
		RC_ID1		I_AN	X		X	
H13	H13	GPIO036/RC_ID2/SPI0_MISO	VTR1					
		GPIO036,SPI0_MISO		PIO	X		X	
		RC_ID2		I_AN	X		X	

MEC1703-169 WFBGA-XY	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
H11	GPIO025/TIN0/nEM_INT/UART_CLK	VTR2	PIO	X		X	X
H12	GPIO170/TFCLK/UART1_TX	VTR1	PIO	X		X	X
H14	GPIO240	VTR1	PIO	X		X	X
H15	GPIO034/RC_ID1/SPI0_CLK	VTR1					
	GPIO034/SPI0_CLK		PIO	X		X	
	RC_ID1		I_AN	X		X	
J1	GPIO212/ADC10	VTR1					
	GPIO212		PIO	X		X	
	ADC10		I_AN	X		X	
J2	GPIO200/ADC00	VTR1					
	GPIO200		PIO	X		X	
	ADC00		I_AN	X		X	
J4	GPIO210/ADC08	VTR1					
	GPIO210		PIO	X		X	
	ADC08		I_AN	X		X	
J5	VREF_ADC		PWR			X	
J7	VSS3		PWR				
J8	GPIO231	VTR2	PIO	X		X	X
J9	GPIO015/PWM7	VTR2	PIO	X		X	X
J11	GPIO140/I2C06_SCL/ICT5	VTR2	PIO	X		X	X
J12	GPIO036/RC_ID2/SPI0_MISO	VTR1					
	GPIO036/SPI0_MISO		PIO	X		X	
	RC_ID2		I_AN	X		X	
J14	GPIO043/SB-TSI_CLK	VTR1					
	GPIO043		PIO	X		X	
	SB-TSI_CLK		PECI	X		X	
J15	GPIO042/PECI_DAT/SB-TSI_DAT	VTR1					
	GPIO042		PIO	X		X	
	PECI_DAT/SB-TSI_DAT		PECI	X		X	
K1	GPIO213/ADC11	VTR1					
	GPIO213		PIO	X		X	
	ADC11		I_AN	X		X	
K2	GPIO203/ADC03	VTR1					
	GPIO203		PIO	X		X	
	ADC03		I_AN	X		X	

MEC1703-169 WFBGA-XY	Signal	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
P9	GPIO130/I2C10_SDA/TOUT1	VTR2	PIO	X		X	X
P10	GPIO021/LPCPD#/KSI2	VTR2	PIO	X		X	X
P11	GPIO014/PWM6/GPTP-IN6	VTR2	PIO	X		X	X
P12	GPIO026/TIN1/KSI3	VTR2	PIO	X		X	X
P13	GPIO115/PS2_DAT0A	VTR2	PIO	X		X	X
P14	GPIO053/PWM0/GPWM0	VTR2	PIO	X	X	X	X
P15	GPIO027/TIN2/KSI4	VTR2	PIO	X		X	X
R2	GPIO065/PCI_CLK/ESPI_CLK	VTR3	PIO	X		X	X
R3	GPIO070/LAD0/ESPI_IO0	VTR3					
	GPIO070/ESPI_IO0		PIO				
	LAD0		PCI				
R4	GPIO071/LAD1/ESPI_IO1	VTR3					
	GPIO071/ESPI_IO1		PIO				
	LAD1		PCI				
R5	GPIO073/LAD3/ESPI_IO3	VTR3					
	GPIO073/ESPI_IO3		PIO				
	LAD3		PCI				
R6	GPIO224/GPTP-IN4/SHD_IO1	VTR2	PIO	X		X	X
R7	GPIO223/SHD_IO0	VTR2	PIO	X		X	X
R8	GPIO013/I2C07_SCL/TOUT2	VTR2	PIO	X		X	X
R9	GPIO020/KSI1	VTR2	PIO	X		X	X
R10	GPIO131/I2C10_SCL/TOUT0	VTR2	PIO	X		X	X
R11	GPIO230	VTR2	PIO	X		X	X
R12	GPIO001/PWM4	VTR2	PIO	X		X	X
R13	GPIO152/GPTP-OUT3/KSO16	VTR2	PIO	X		X	X
R14	GPIO132/I2C06_SDA/KSO14	VTR2	PIO	X		X	X

2.6 Signal Description by Signal

EMULATED POWER WELL

Power well emulation for GPIOs and for signals that are multiplexed with GPIO signals is controlled by the POWER_-GATING field in the GPIO Pin Control Register. Power well emulation for signals that are not multiplexed with GPIO signals is defined by the entries in this column.

GATED STATE

This column defines the internal value of an input signal when either its emulated power well is inactive or it is not selected by the GPIO alternate function MUX. A value of “No Gate” means that the internal signal always follows the pin even when the emulated power well is inactive.

TABLE 2-2: STRAPS AND MEANING

Pin	Function	Definition
GPIO233	UPD[2] RESET_N	Pull-down (0) = UPD Port 2 Not Present Pull-up (1) = UPD Port 2 Present **Note:** 10k to 100k ohm pull-up or pull-down required.
GPIO246	UPD_Enable	Pull-down (0) = No UPD devices are connected Pull-up (1) = One or more UPD devices are connected **Note:** 10k to 100k ohm pull-up or pull-down required.
GPIO045/KSO1	Private SPI Selection	1=Use GPIO055 to select between the Shared SPI pins and the eSPI Flash Channel for Boot 0=Use the Private SPI pins for Boot **Note:** This pin requires an external pull-up for normal operation.
GPIO055/SHD_CS#	Shared SPI vs. eSPI Selection	1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot **Note:** See application specific recommendation in Section 2.9.1, "Shared SPI Flash Chip Select Pull-up Resistor Recommendation " after this table.
GPIO171/TFDATA/ UART1_RX	JTAG Boundary Scan	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug

Note: Please refer to MEC170X_ROM_Description.pdf for more details about UPD strap pins and there functioning.

2.9.1 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/PWM2/SHD_CS#/RSMRST# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/PWM2/SHD_CS#/RSMRST# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS# pin on the board if the Shared SPI flash interface is used so that the SPI_CS# is detected high while RSMRST# is low.

The recommended value of the pull-up resistor on the SHD_CS# pin may vary depending on the version of the Intel PCH that is used.

This is based on information in the current Intel PCH device specifications regarding the SPI0_CS0# pin. This information, as well as the information regarding other PCH devices, must be verified with Intel:

Skylake PCH LP: the signal is tri-stated with no pull-up or pull-down

- Use a resistor in the 4.7K-100K range (pulled-up to the 3.3V rail that powers the SPI device)

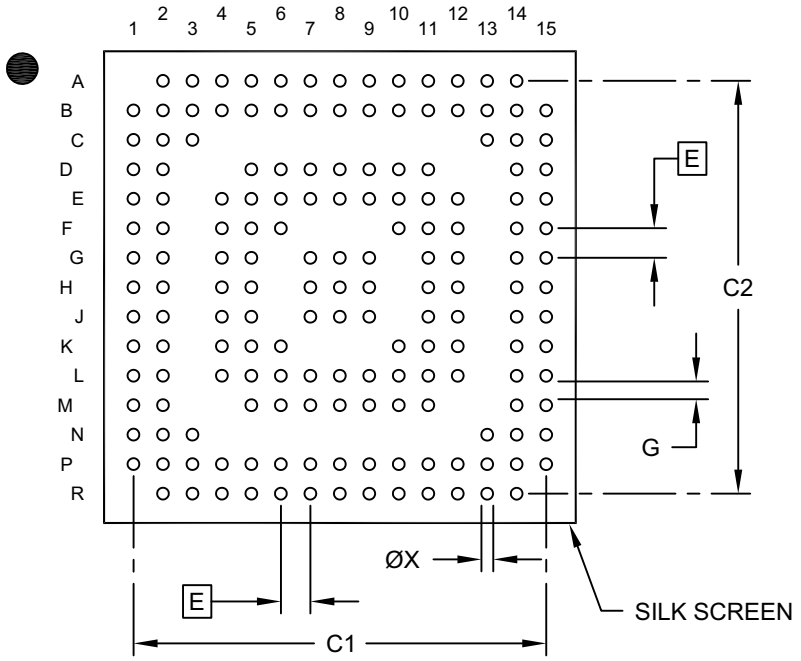
Skylake PCH H: the signal is tri-stated with a weak pull down (~ 20K)

- Use a resistor in the 4.7K-8K range (pulled-up to the 3.3V rail that powers the SPI device).

These pull-up values must ensure the voltage on the pin is detected as a high (i.e., VTR*0.7).

169-Ball Very Very Thin Fine Pitch Ball Grid Array (XYX) - 8x8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Overall Contact Pad Spacing	C1		7.00	
Overall Contact Pad Spacing	C2		7.00	
Contact Pad Width (X169)	X			0.20
Contact Pad to Contact Pad	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2470 Rev. A

TABLE 9-2: SIGNAL DESCRIPTION (CONTINUED)

Name	Direction	Description
LFRAME#	Input	Active low signal indicates start of new cycle and termination of broken cycle.
LRESET#	Input	Active low signal used as LPC Interface Reset. Same as PCI Reset on host. This signal can be monitored using the LPC Bus Monitor Register. **Note:** LRESET# is typically connected to the host PCI RESET (PCIRST#) signal.
LCLK	Input	PCI clock input (PCI_CLK)
SERIRQ	Input/Output	Serial IRQ pin used with the LCLK signal to transfer interrupts to the host.
CLKRUN#	Open-Drain Output	Clock Control for LCLK
LPCPD#	Input	Power Down: Indicates that the device should prepare for power to be removed from the LPC I/F.

9.5 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

9.5.1 POWER DOMAINS

TABLE 9-3: POWER SOURCES

Name	Description
VTR_PLL	Registers and control logic for this block are powered by this rail.

9.5.2 CLOCK INPUTS

TABLE 9-4: CLOCK INPUTS

Name	Description
48MHz	Control logic for the internal logic in this block is clocked by the main clock domain.
LCLK	Host-facing logic for the LPC Interface is clocked on the LPC clock

9.5.3 RESETS

Name	Description
RESET_SYS	Reset signal used to indicate when the main internal power rail is applied. This reset is also asserted on a Watchdog Timer timeout.
RESET_VCC	This signal is used to indicate when the main power rail in the system is reset. It is asserted when: • The internal RESET_SYS reset signal is asserted • The external VCC_PWRGD signal indicates the main system power rail is unpowered
RESET_HOST	This signal is used to indicate when the main power rail in the system is reset. It is asserted when: • The RESET_VCC is asserted • The LPC interface is enabled and the external LRESET# reset signal is asserted

10.4.4 INTERRUPT INTERFACE

This section defines the interrupt Interface signals routed to the chip interrupt aggregator.

Source	Description
Wake Only Event	
ESPI_WAKE_ONLY	This signal is asserted when the eSPI interface detects eSPI traffic. If enabled, it may be used to wake the main clock domain when the chip is in a sleep state.
Peripheral Channel	
INTR_PC	Peripheral Channel Interrupt
INTR_BM1	Bus Mastering Channel 1 Interrupt
INTR_BM2	Bus Mastering Channel 2 Interrupt
INTR_LTR	Peripheral Message (LTR) Interrupt
OOB Channel	
INTR_OOB_UP	Out of Band Channel Up Interrupt
INTR_OOB_DOWN	Out of Band Channel Down Interrupt
Flash Channel	
INTR_FLASH	Flash Channel Interrupt
Virtual Wires Channel	
MSVW[00:09]_SRC[3:0]	Master-to-Slave Virtual Wire Interrupts
eSPI Global	
eSPI_RESET	eSPI Reset Interrupt This interrupt is generated whenever the external eSPI_RESET# pin changes state.

10.5 Low Power Modes

The eSPI block can enter a low power state when it is not in operation. When the eSPI block is operational it will keep the main system clock from shutting down and entering its sleep state. When the eSPI_CS# pin is asserted the eSPI block will wake the main system clock, if it is in a sleep state, and keep the system clock in its active state until the transaction started by the Master has completed.

The low power behavior of the block is controlled by the BAR Inhibit Register. The block is not affected by a SLEEP_ENABLE signal from the chip's Power, Clocks and Resets unit.

10.6 Description

The Intel® eSPI Interface is used by the system host to configure the chip and communicate with the logical devices implemented in the design through a series of read/write registers.

Note: In order to use eSPI, software must individually configure the mux control for every GPIO associated with an eSPI bus signal to the eSPI function. Pins are **not** automatically configured for eSPI operation when the eSPI Controller is enabled.

18.10.4.2 Output GPIO[040:076] Register

Offset	384h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:24	Reserved	R	-	-
30:24	GPIO[076:070] Output	R/W	00h	RESET_SYS
23:16	GPIO[067:060] Output	R/W	00h	RESET_SYS
15:8	GPIO[057:050] Output	R/W	00h	RESET_SYS
7:0	GPIO[047:040] Output	R/W	00h	RESET_SYS

18.10.4.3 Output GPIO[100:136] Register

Offset	388h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	Reserved	R	-	-
30:24	GPIO[136:130] Output	R/W	00h	RESET_SYS
23:16	GPIO[127:120] Output	R/W	00h	RESET_SYS
15:8	GPIO[117:110] Output	R/W	00h	RESET_SYS
7:0	GPIO[107:100] Output	R/W	00h	RESET_SYS

18.10.4.4 Output GPIO[140:176] Register

Offset	38Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:22	Reserved	R	-	-
30:24	GPIO[176:170] Output	R/W	00h	RESET_SYS

22.0 INPUT CAPTURE AND COMPARE TIMER

22.1 Introduction

The Input Capture and Compare Timers block contains a 32-bit timer running at the main system clock frequency. The timer is free-running and is associated with six 32-bit capture registers and two compare registers. Each capture register can record the value of the free-running timer based on a programmable edge of its associated input pin. An interrupt can be generated for each capture register each time it acquires a new timer value. The timer can also generate an interrupt when it automatically resets and can additionally generate two more interrupts when the timer matches the value in either of two 32-bit compare registers.

22.2 References

No references have been cited for this feature.

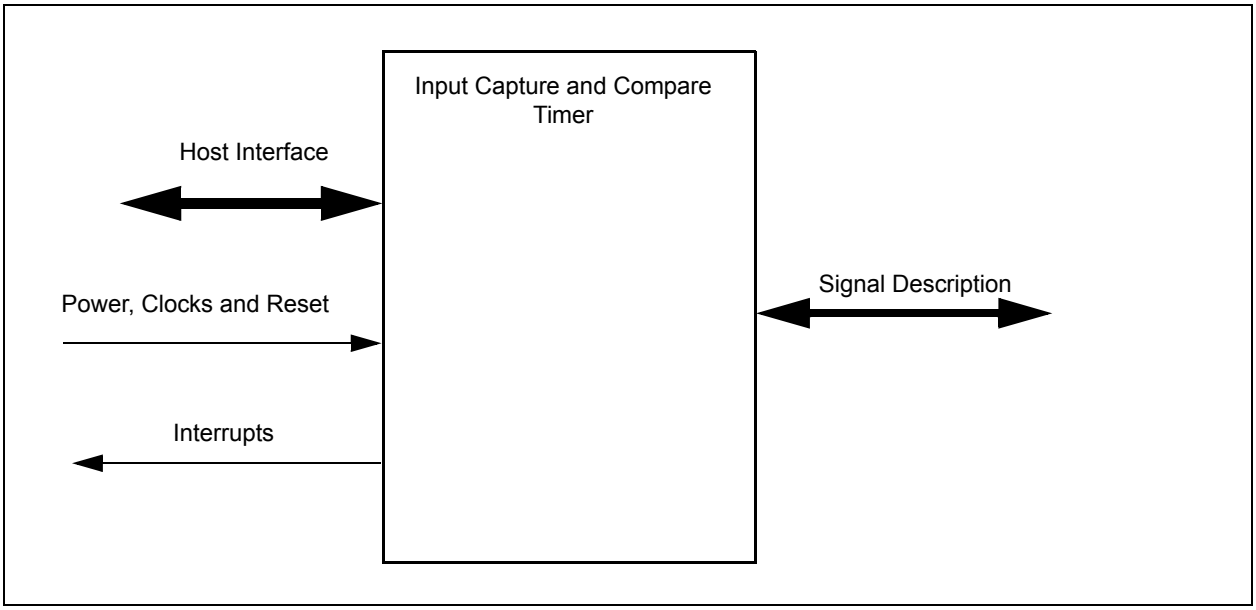
22.3 Terminology

There is no terminology for this block.

22.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 22-1: I/O DIAGRAM OF BLOCK



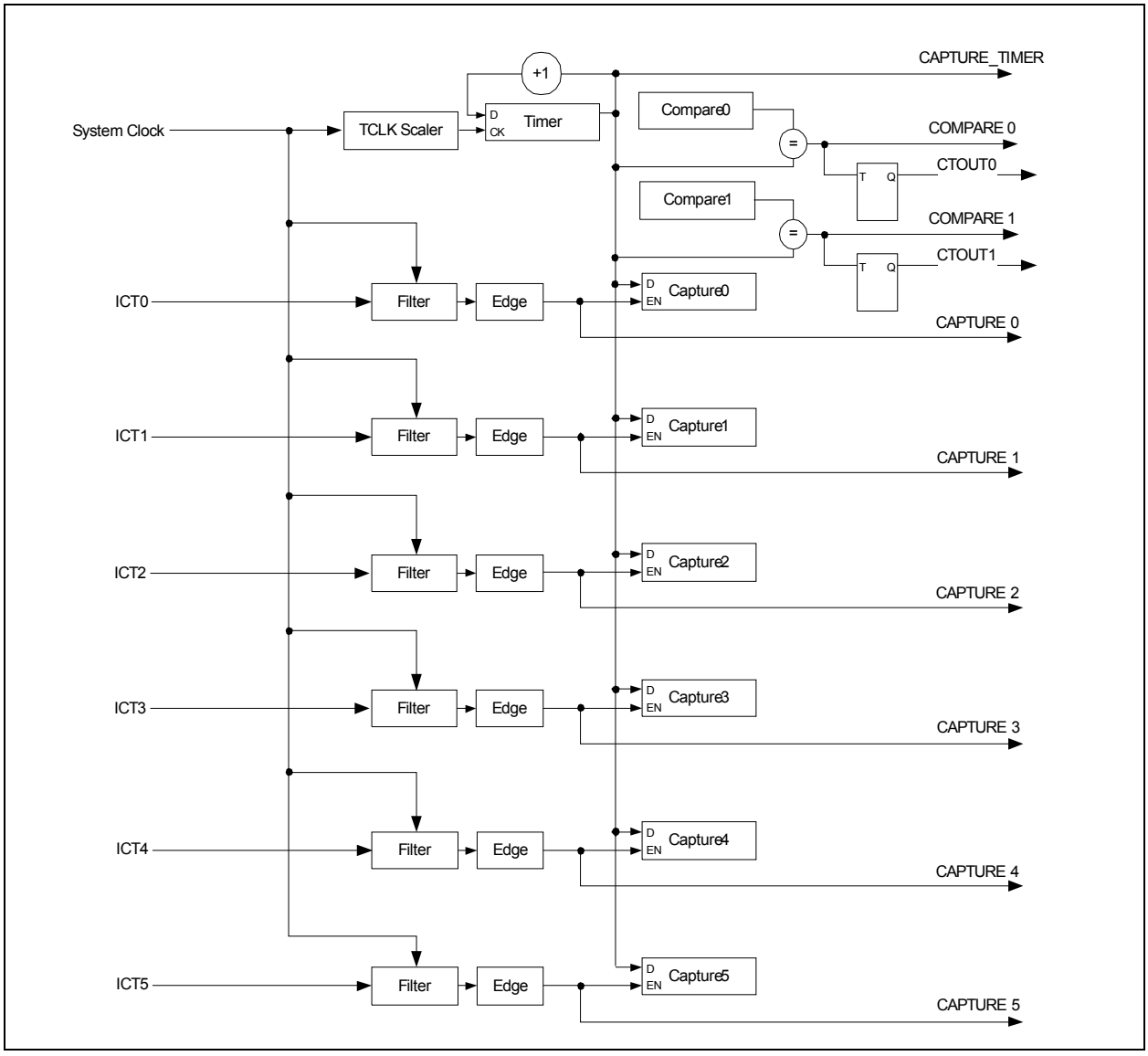
22.5 Signal Description

TABLE 22-1: SIGNAL DESCRIPTION

Name	Direction	Description
ICT0	INPUT	External capture trigger signal for Capture Register 0. Identical to signal FAN_TACH0.
ICT1	INPUT	External capture trigger signal for Capture Register 1. Identical to signal FAN_TACH1.

22.10 Description

FIGURE 22-2: CAPTURE AND COMPARE TIMER BLOCK DIAGRAM



22.10.1 TIMER CLOCK

Any of the frequencies listed in Table 22-2 may be used as the time base for the Free Running Counter.

TABLE 22-2: TIMER CLOCK FREQUENCIES

Timer Clock Select	Frequency Divide Select	Frequency Selected
0000b	Divide by 1	48MHz
0001b	Divide by 2	24MHz
0010b	Divide by 4	12MHz
0011b	Divide by 8	6MHz
0100b	Divide by 16	3MHz
0101b	Divide by 32	1.5MHz

27.0 TACH

27.1 Introduction

This block monitors TACH output signals (or locked rotor signals) from various types of fans, and determines their speed.

27.2 References

No references have been cited for this feature.

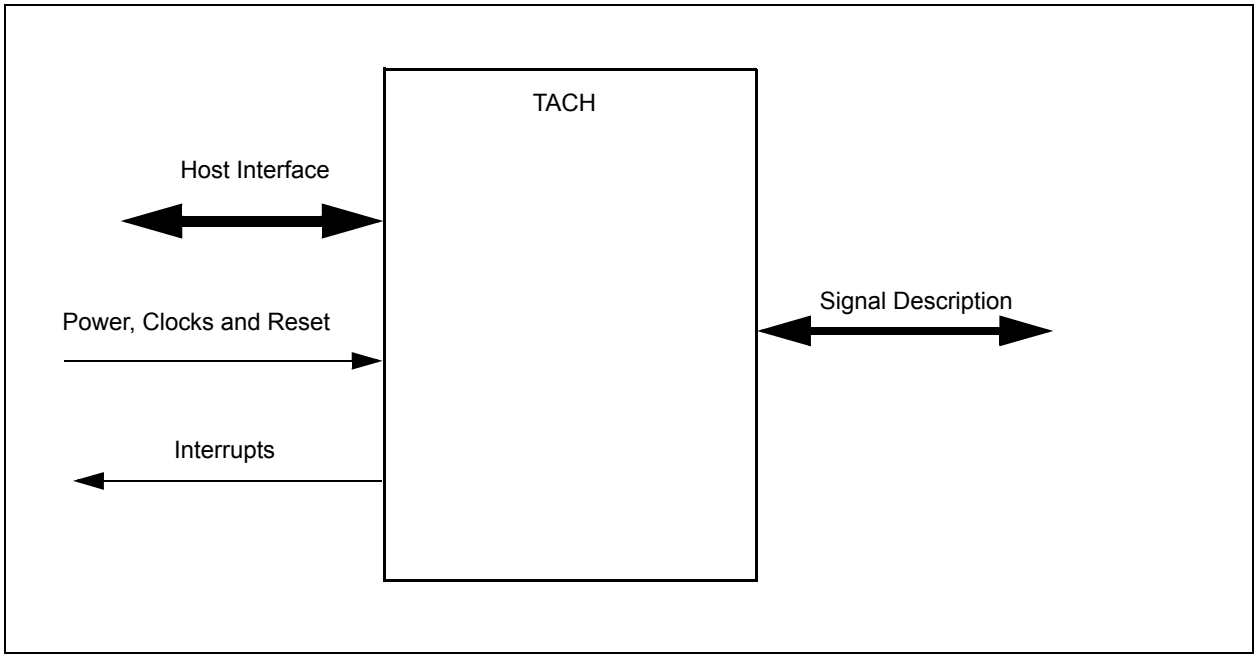
27.3 Terminology

There is no terminology defined for this section.

27.4 Interface

This block is designed to be accessed externally via the pin interface and internally via a registered host interface.

FIGURE 27-1: I/O DIAGRAM OF BLOCK



27.5 Signal Description

TABLE 27-1: SIGNAL DESCRIPTION

Name	Direction	Description
TACH INPUT	Input	Tachometer signal from TACHx Pin.

27.6 Host Interface

The registers defined for the TACH are accessible by the various hosts as indicated in Section 27.11, "EC Registers".

33.9 Implementation

In addition to the registers described in Section 33.10, "EC Registers", the PWM is implemented using a number of components that are interconnected differently when configured for breathing operation and when configured for blinking/PWM operation.

33.9.1 BREATHING CONFIGURATION

The **PSIZE** parameter can configure the PWM to one of three modes: 8-bit, 7-bit and 6-bit. The **PERIOD CTR** counts ticks of its input clock. In 8-bit mode, it counts from 0 to 255 (that is, 256 steps), then repeats continuously. In this mode, a full cycle takes 7.8ms (128Hz). In 7-bit mode it counts from 0 to 127 (128 steps), and a full cycle takes 3.9ms (256Hz). In 6-bit mode it counts from 0 to 63 (64 steps) and a full cycle takes 1.95ms (512Hz).

The output of the LED circuit is asserted whenever the **PERIOD CTR** is less than the contents of the **DUTY CYCLE** register. The appearance of breathing is created by modifying the contents of the **DUTY CYCLE** register in a continuous manner. When the LED control is off the internal counters and registers are all reset to 0 (i.e. after a write setting the RESET bit in the LED Configuration Register Register.) Once enabled, the **DUTY CYCLE** register is increased by an amount determined by the LED_STEP register and at a rate determined by the **DELAY** counter. Once the duty cycle reaches its maximum value (determined by the field MAX), the duty cycle is held constant for a period determined by the field HD. Once the hold time is complete, the **DUTY CYCLE** register is decreased, again by an amount determined by the LED_STEP register and at a rate determined by the **DELAY** counter. When the duty cycle then falls at or below the minimum value (determined by the field MIN), the duty cycle is held constant for a period determined by the field HD. Once the hold time is complete, the cycle repeats, with the duty cycle oscillating between MIN and MAX.

The rising and falling ramp times as shown in Figure 33-2, "Breathing LED Example" can be either symmetric or asymmetric depending on the setting of the SYMMETRY bit in the LED Configuration Register Register. In Symmetric mode the rising and falling ramp rates have mirror symmetry; both rising and falling ramp rates use the same (all) 8 segments fields in each of the following registers (see Table 33-6): the LED Update Stepsize Register register and the LED Update Interval Register register. In Asymmetric mode the rising ramp rate uses 4 of the 8 segments fields and the falling ramp rate uses the remaining 4 of the 8 segments fields (see Table 33-6).

The parameters MIN, MAX, HD, LD and the 8 fields in LED_STEP and LED_INT determine the brightness range of the LED and the rate at which its brightness changes. See the descriptions of the fields in Section 33.10, "EC Registers", as well as the examples in Section 33.9.3, "Breathing Examples" for information on how to set these fields.

TABLE 33-6: SYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 33-3, "Clipping Example"	**Duty Cycle**	**Segment Index**	**Symmetric Mode Register Fields Utilized**	
X	000xxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
X	001xxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
X	010xxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]
X	011xxxxxb	011b	STEP[3]/INT[3]	Bits[15:12]
X	100xxxxxb	100b	STEP[4]/INT[4]	Bits[19:16]
X	101xxxxxb	101b	STEP[5]/INT[5]	Bits[23:20]
X	110xxxxxb	110b	STEP[6]/INT[6]	Bits[27:24]
X	111xxxxxb	111b	STEP[7]/INT[7]	Bits[31:28]
Note: In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]				

TABLE 33-7: ASYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 33-3, "Clipping Example"	**Duty Cycle**	**Segment Index**	**Asymmetric Mode Register Fields Utilized**	
Rising	00xxxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
Rising	01xxxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
Rising	10xxxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]

2, 3: Modify the duty cycle by 2

0, 1: Modify the duty cycle by 1

In 6-bit mode, the two least significant bits of the 4-bit field is ignored, so each field represents 4 possible duty cycle modifications, from 1 to 4 as the duty cycle is modified between 0 and 63:

12, 13, 14, 15: Modify the duty cycle by 4

8, 9, 10, 11: Modify the duty cycle by 3

4, 5, 6, 7: Modify the duty cycle by 2

0, 1, 2, 3: Modify the duty cycle by 1

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:28	UPDATE_STEP7 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 111.	R/W	0h	RESET_SYS
27:24	UPDATE_STEP6 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 110.	R/W	0h	RESET_SYS
23:20	UPDATE_STEP5 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 101	R/W	0h	RESET_SYS
19:16	UPDATE_STEP4 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 100.	R/W	0h	RESET_SYS
15:12	UPDATE_STEP3 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 011.	R/W	0h	RESET_SYS
11:8	UPDATE_STEP2 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 010.	R/W	0h	RESET_SYS
7:4	UPDATE_STEP1 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 001.	R/W	0h	RESET_SYS
3:0	UPDATE_STEP0 Amount the current duty cycle is adjusted at the end of every PWM period when the segment index is equal to 000.	R/W	0h	RESET_SYS

33.10.5 LED UPDATE INTERVAL REGISTER

This register has eight segment fields which provide the number of PWM periods between updates to current duty cycle. Segment field selection is decoded based on the segment index. The segment index equation utilized depends on the SYMMETRY bit in the LED Configuration Register Register)

- In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]
- In Asymmetric Mode the Segment_Index[2:0] is the bit concatenation of following: Segment_Index[2] = (FALLING RAMP TIME in Figure 36-3, "Clipping Example") and Segment_Index[1:0] = Duty Cycle Bits[7:6].

This register may be written at any time. Values written into the register are held in an holding register, which is transferred into the actual register at the end of a PWM period if the Enable Update bit in the LED Configuration register is set to 1. Reads of this register return the current contents and not the value of the holding register.

35.6 Host Interface

The registers defined for the Keyboard Scan Interface are accessible by the various hosts as indicated in Section 35.11, "EC Registers".

35.7 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

35.7.1 POWER DOMAINS

Name	Description
VTR	The logic and registers implemented in this block are powered by this power well.

35.7.2 CLOCK INPUTS

Name	Description
48MHz	This is the clock source for Keyboard Scan Interface logic.

35.7.3 RESETS

Name	Description
RESET_SYS	This signal resets all the registers and logic in this block to their default state.

35.8 Interrupts

This section defines the Interrupt Sources generated from this block.

Source	Description
KSC_INT	Interrupt request to the Interrupt Aggregator.
KSC_INT_WAKE	Wake-up request to the Interrupt Aggregator’s wake-up interface.

35.9 Low Power Modes

The Keyboard Scan Interface automatically enters a low power mode whenever it is not actively scanning the keyboard matrix. The block is also placed in a low-power state when it is disabled by the KSEN bit. When the interface is in a low-power mode it will not prevent the chip from entering a sleep state. When the interface is active it will inhibit the chip sleep state until the interface has re-entered its low power mode.

37.12.1 SPI ENABLE REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:1	Reserved	R	-	-
0	ENABLE 1=Enabled. The device is fully operational 0=Disabled. Clocks are gated to conserve power and the SPDOUT and SPI_CLK signals are set to their inactive state	R/W	0h	RESET_SYS

37.12.2 SPI CONTROL REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:7	Reserved	R	-	-
6	CE SPI Chip Select Enable. 1=SPI_CS# output signal is asserted, i.e., driven to logic ‘0’ 0=SPI_CS# output signal is deasserted, i.e., driven to logic ‘1’	R/W	0h	RESET_SYS
5	AUTO_READ Auto Read Enable. 1=A read of the SPI RX_DATA Register will clear both the RXBF status bit and the TXBE status bit 0=A read of the SPI RX_DATA Register will clear the RXBF status bit. The TXBE status bit will not be modified	R/W	0h	RESET_SYS
4	SOFT_RESET Soft Reset is a self-clearing bit. Writing zero to this bit has no effect. Writing a one to this bit resets the entire SPI Interface, including all counters and registers back to their initial state.	R/W	0h	RESET_SYS
3:2	SPDIN_SELECT The SPDIN Select which SPI input signals are enabled when the BIOEN bit is configured as an input. 1xb=SPDIN1 and SPDIN2. Select this option for Dual Mode 01b=SPDIN2 only. Select this option for Half Duplex 00b=SPDIN1 only. Select this option for Full Duplex	R/W	0h	RESET_SYS

TABLE 51-3: POWER SEQUENCING PARAMETERS (CONTINUED)

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_3	VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR1 above minimum operating threshold. VTR1 at1.8V(nom) or 3.3V(nom)	0		1	ms	13, 17
t_4	VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR2 above minimum operating threshold. VTR2 at1.8V(nom) or 3.3V(nom)	0		1	ms	14, 17
t_{5b}	FOR ESPI BOOT (VTR3=1.8V) VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR3 above minimum operating threshold.	0		30	sec	15, 17
	FOR NON-ESPI BOOT (VTR3 = 1.8V or 3.3V) VTR_ANALOG and VTR_REG are both above minimum operating thresholds to VTR3 above minimum operating threshold.	0			ms	16, 17

10: VTR_ANALOG and VTR_REG may ramp in either order. There is no limit on the time between the ramp of one rail and the ramp of the other.

11: VBAT must rise no later than VTR_ANALOG and VTR_REG. This relationship is ensured by the recommended battery circuit.

12: VTR_ANALOG and VTR_PLL must be connected to the same 3.3V power source.

13: The JTAG_STRAP pin is powered by VTR1 and is sampled on the assertion of the first RESET_EC event following a RESET_VTR. Subsequent EC resets will not sample the JTAG_STRAP pin. VTR1 must be powered prior to the deassertion of RESET_EC.

14: The SHD_CS# pin, which is powered by VTR2, must be powered before the Boot ROM samples this pin.

15: If booting over eSPI, the EC boot ROM code monitors GPIO227/SHD_IO2, which is a VTR2 signal, to determine that VTR3 is active. The maximum time is the time after which the code abandons the boot.

16: In non-eSPI applications, where VTR3 may be either 1.8V or 3.3V, software must program the GPIO Bank Power register for VTR3 pins before any of the VTR3 powered pins are used.

17: minimum operating threshold values for Power Rails are defined in Table 50-1, “Power Supply Operating Conditions,” on page 603.

51.4 RESETI# Timing

FIGURE 51-5: RESETI# TIMING

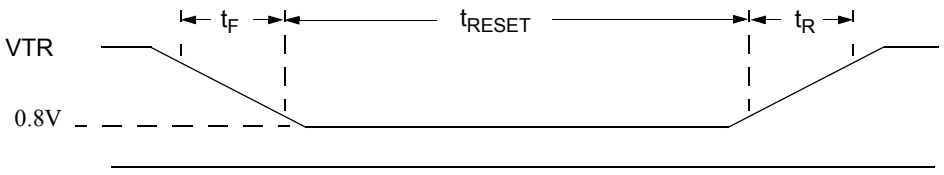


TABLE 51-4: RESETI# TIMING PARAMETERS

Symbol	Parameter	Limits		Units	Comments
		MIN	MAX		
t_F	RESETI# Fall time	0	1	ms	
t_R	RESETI# Rise time	0	1	ms	
t_{RESET}	Minimum Reset Time	1		µs	Note 1

Note 1: The RESETI# input pin can tolerate glitches of no more than 50ns.

51.17 PWM Timing

FIGURE 51-22: PWM OUTPUT TIMING

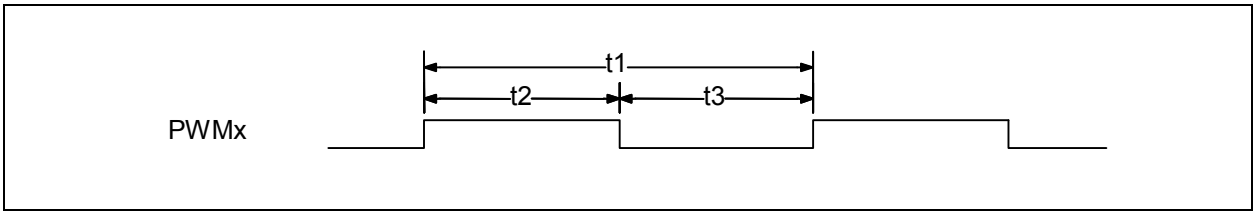
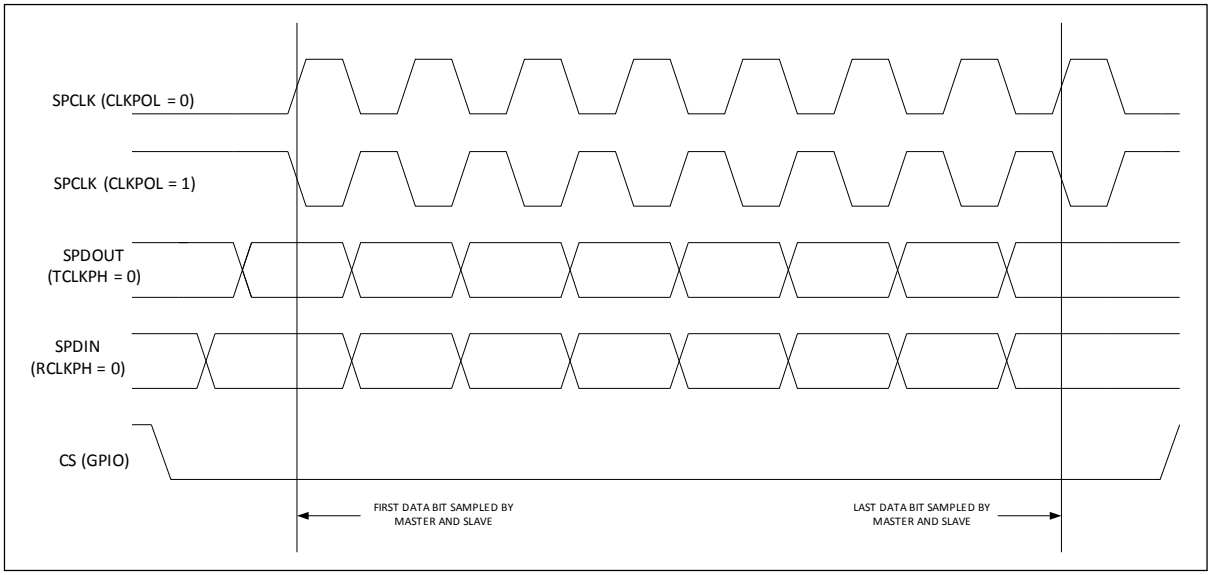


TABLE 51-20: PWM TIMING PARAMETERS

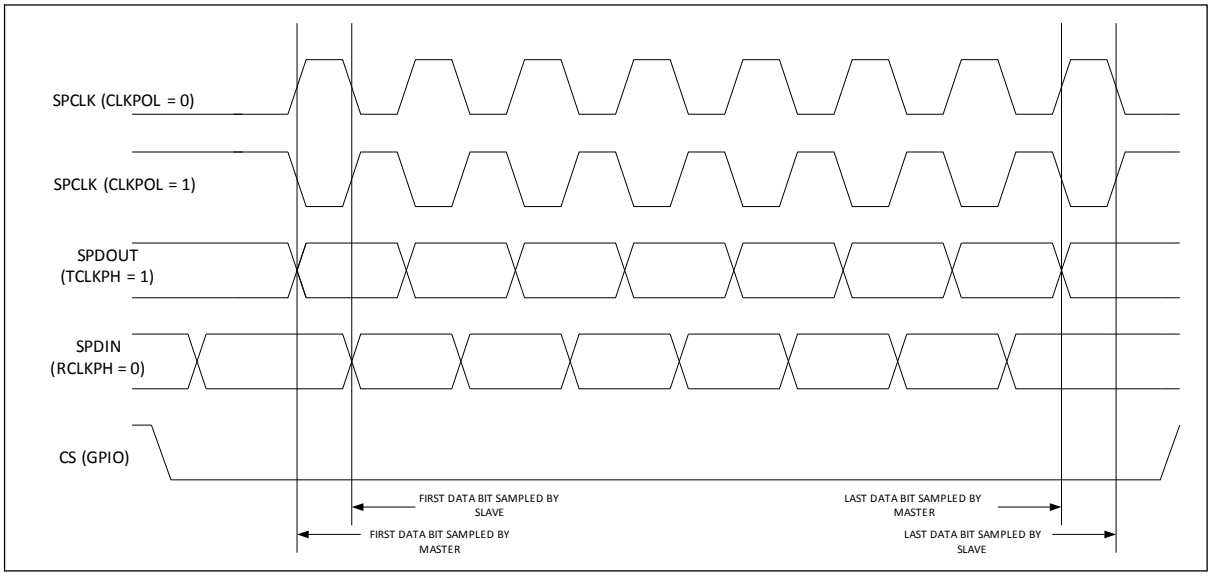
Name	Description	MIN	TYP	MAX	Units
t1	Period	42ns		23.3sec	
t_f	Frequency	0.04Hz		24MHz	
t2	High Time	0		11.65	sec
t3	Low Time	0		11.65	sec
t_d	Duty cycle	0		100	%

FIGURE 51-33: INTERFACE TIMING, FULL DUPLEX MODE (TCLKPH = 0, RCLKPH = 0)



In this mode, data is available immediately when a device is selected and is sampled on the first and following odd SPCLK edges by the master and slave.

FIGURE 51-34: SPI INTERFACE TIMING, FULL DUPLEX MODE (TCLKPH = 1, RCLKPH = 0)



In this mode, the master requires an initial SPCLK edge before data is available. The data from slave is available immediately when the slave device is selected. The.data is sampled on the first and following odd edges by the master. The data is sampled on the second and following even SPCLK edges by the slave.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820