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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89c51rc2bbd-01-55

Table 1. Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00000000B
RCAP2H#	Timer 2 Capture High	CBH									00H
RCAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T}2$	$CP/\overline{RL}2$	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0	00H
WDTRST	Watchdog Timer Reset	A6H									

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. Minimum and maximum high and low times specified in the data sheet must be observed.

This device is configured at the factory to operate using 12 clock periods per machine cycle, referred to in this datasheet as “12-clock mode”. It may be optionally configured on commercially available Flash programming equipment or via ISP or via software to operate at 6 clocks per machine cycle, referred to in this datasheet as “6-clock mode”. (This yields performance equivalent to twice that of standard 80C51 family devices). Also see next page.

LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

POWER-ON FLAG

The Power-On Flag (POF) is set by on-chip circuitry when the V_{CC} level on the P89C51RA2/RB2/RC2/RD2xx rises from 0 to 5 V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3 V for the POF to remain unaffected by the V_{CC} level.

Design Consideration

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE (“On-Circuit Emulation”) Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{\text{PSEN}}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{\text{PSEN}}$ are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency in 12-clock mode (122 Hz to 8 MHz in 6-clock mode).

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{\text{T}}$2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H, RCAP2L})}$$

n = 2 in 6-clock mode
4 in 12-clock mode

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	$\overline{\text{PSEN}}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Summary of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{OSC}}{[\, n^* \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

* n = 16 in 6-clock mode
32 in 12-clock mode

Where f_{OSC}= Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H}, \text{RCAP2L} = 65536 - \left(\frac{f_{OSC}}{n^* \times \text{Baud Rate}}\right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. see Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:
1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

SCON Address = 98H Reset Value = 00H

Bit Addressable

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	$f_{OSC}/12$ (12-clock mode) or $f_{OSC}/6$ (6-clock mode)
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$ (12-clock mode) or $f_{OSC}/32$ or $f_{OSC}/16$ (6-clock mode)
1	1	3	9-bit UART	variable

SM2 Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then Rl will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.

REN Enables serial reception. Set by software to enable reception. Clear by software to disable reception.

TB8 The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

RB8 In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.

RI Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

SU01626

Figure 12. Serial Port Control (SCON) Register

Baud Rate			f_{OSC}	SMOD	Timer 1		
Mode	12-clock mode	6-clock mode			C/$\overline{T}$	Mode	Reload Value
Mode 0 Max	1.67 MHz	3.34 MHz	20 MHz	X	X	X	X
Mode 2 Max	625 k	1250 k	20 MHz	1	X	X	X
Mode 1, 3 Max	104.2 k	208.4 k	20 MHz	1	0	2	FFH
Mode 1, 3	19.2 k	38.4 k	11.059 MHz	1	0	2	FDH
	9.6 k	19.2 k	11.059 MHz	0	0	2	FDH
	4.8 k	9.6 k	11.059 MHz	0	0	2	FAH
	2.4 k	4.8 k	11.059 MHz	0	0	2	F4H
	1.2 k	2.4 k	11.059 MHz	0	0	2	E8H
	137.5	275	11.986 MHz	0	0	2	1DH
	110	220	6 MHz	0	0	2	72H
	110	220	12 MHz	0	0	1	FEEBH

Figure 13. Timer 1 Generated Commonly Used Baud Rates

More About Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed a 1/12 the oscillator frequency (12-clock mode) or 1/6 the oscillator frequency (6-clock mode).

Figure 14 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after “write to SBUF.”

Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are

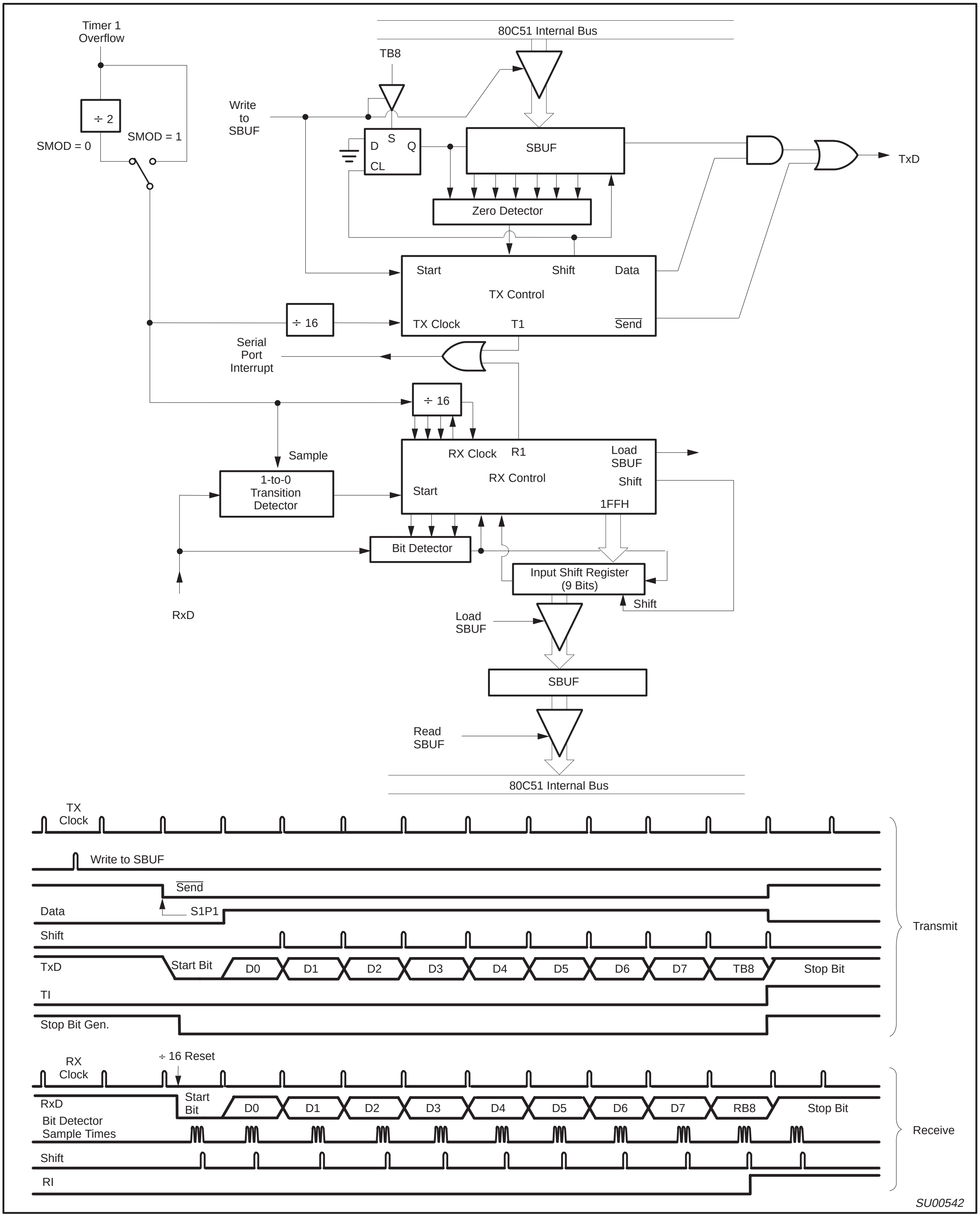


Figure 17. Serial Port Mode 3

Interrupt Priority Structure

The P89C51RA2/RB2/RC2/RD2xx has a 7 source four-level interrupt structure (see Table 7).

There are 3 SFRs associated with the four-level interrupt. They are the IE, IP, and IPH. (See Figures 21, 22, and 23.) The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 23.

The function of the IPH SFR, when combined with the IP SFR, determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L)[1] Y (T)[2]	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
PCA	5	CF, CCFn n = 0–4	N	33H
SP	6	RI, TI	N	23H
T2	7	TF2, EXF2	N	2BH

NOTES:
1. L = Level activated
2. T = Transition activated

	7	6	5	4	3	2	1	0
IE (0A8H)	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

BIT	SYMBOL	FUNCTION
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
IE.6	EC	PCA interrupt enable bit
IE.5	ET2	Timer 2 interrupt enable bit.
IE.4	ES	Serial Port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt 1 enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt 0 enable bit.

SU01290

Figure 21. IE Registers

IP (0B8H)

7	6	5	4	3	2	1	0
–	PPC	PT2	PS	PT1	PX1	PT0	PX0

Priority Bit = 1 assigns high priority
Priority Bit = 0 assigns low priority

BIT	SYMBOL	FUNCTION
IP.7	–	–
IP.6	PPC	PCA interrupt priority bit
IP.5	PT2	Timer 2 interrupt priority bit.
IP.4	PS	Serial Port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt 1 priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt 0 priority bit.

SU01291

Figure 22. IP Registers

IPH (B7H)

7	6	5	4	3	2	1	0
–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

BIT	SYMBOL	FUNCTION
IPH.7	–	–
IPH.6	PPCH	PCA interrupt priority bit
IPH.5	PT2H	Timer 2 interrupt priority bit high.
IPH.4	PSH	Serial Port interrupt priority bit high.
IPH.3	PT1H	Timer 1 interrupt priority bit high.
IPH.2	PX1H	External interrupt 1 priority bit high.
IPH.1	PT0H	Timer 0 interrupt priority bit high.
IPH.0	PX0H	External interrupt 0 priority bit high.

SU01292

Figure 23. IPH Registers

Programmable Counter Array (PCA)

The Programmable Counter Array available on the P89C51RA2/RB2/RC2/RD2xx is a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1.4 (CEX1), etc. The basic PCA configuration is shown in Figure 25.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 28):

CPS1	CPS0	PCA Timer Count Source
0	0	1/6 oscillator frequency (6-clock mode); 1/12 oscillator frequency (12-clock mode)
0	1	1/2 oscillator frequency (6-clock mode); 1/4 oscillator frequency (12-clock mode)
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 26.

The watchdog timer function is implemented in module 4 (see Figure 35).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 29). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 27.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 30). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 31 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

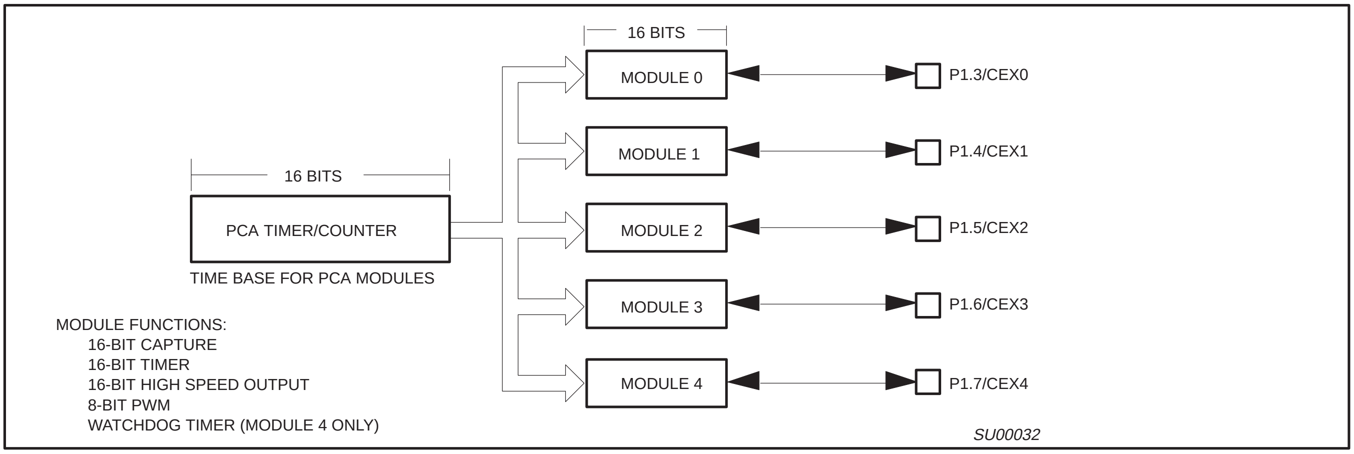


Figure 25. Programmable Counter Array (PCA)

CMOD Address = D9H — Reset Value = 00XX X000B

	CIDL	**WDTE**	**–**	**–**	**–**	**CPS1**	**CPS0**	**ECF**
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
–	Not implemented, reserved for future use.*
CPS1	PCA Count Pulse Select bit 1.
CPS0	PCA Count Pulse Select bit 0.

CPS1	**CPS0**	**Selected PCA Input****	
0	0	0	Internal clock, f_{OSC}/6 in 6-clock mode (f_{OSC}/12 in 12-clock mode)
0	1	1	Internal clock, f_{OSC}/2 in 6-clock mode (f_{OSC}/4 in 12-clock mode)
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin (max. rate = f_{OSC}/4 in 6-clock mode, f_{OCS}/8 in 12-clock mode)

Symbol	Function
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

NOTE:
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
** f_{OSC} = oscillator frequency

SU01318

Figure 28. CMOD: PCA Counter Mode Register

CCON Address = D8H — Reset Value = 00X0 0000B

Bit Addressable

	CF	**CR**	**–**	**CCF4**	**CCF3**	**CCF2**	**CCF1**	**CCF0**
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
–	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

NOTE:
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU01319

Figure 29. CCON: PCA Counter Control Register

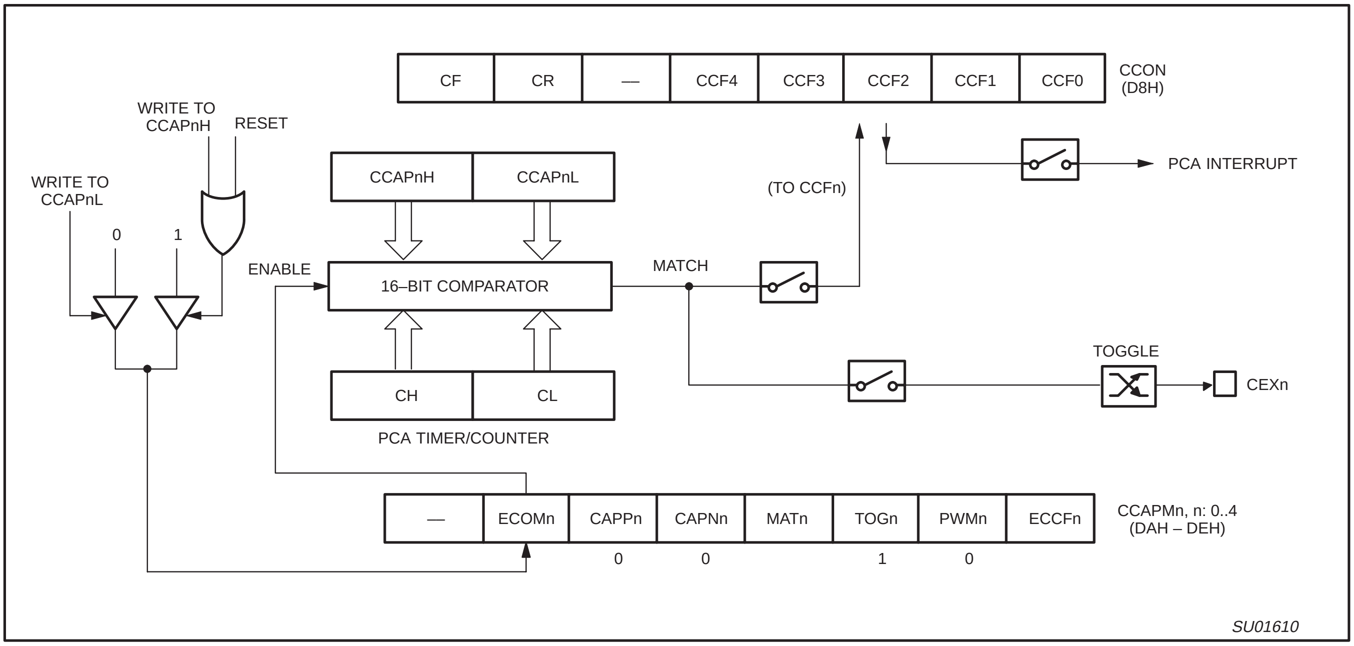


Figure 34. PCA High Speed Output Mode

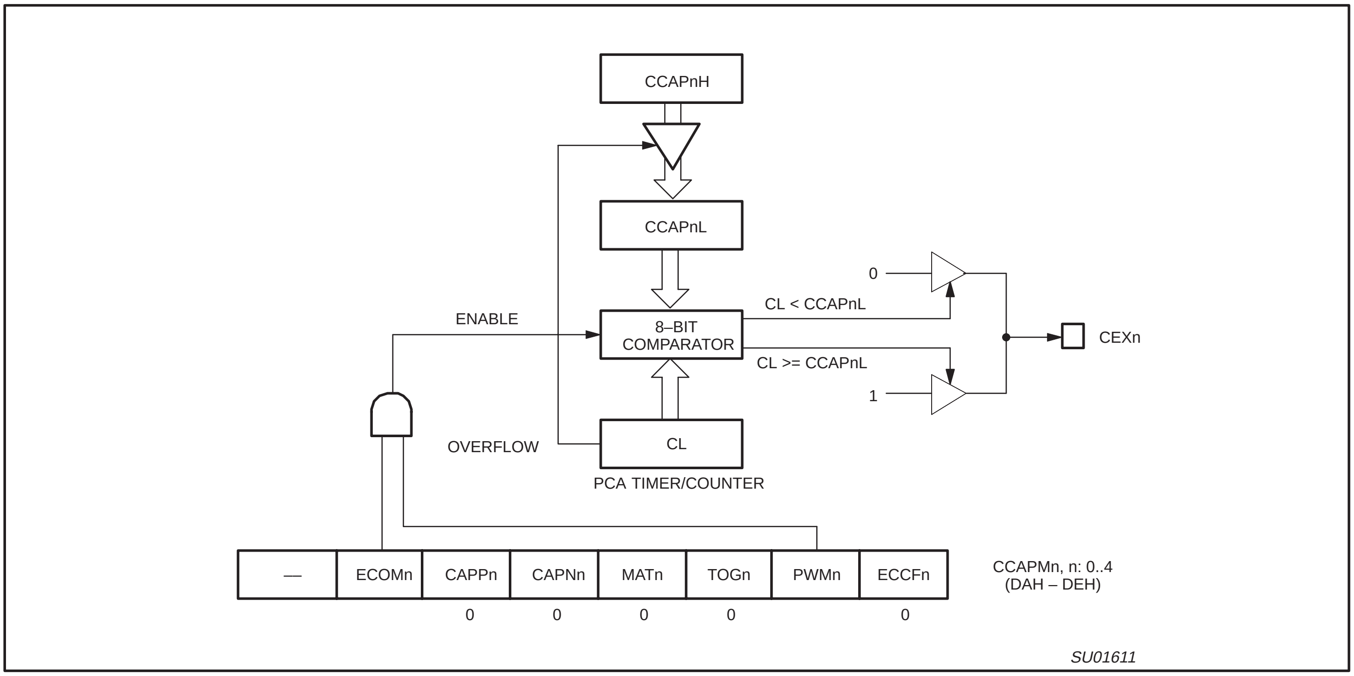


Figure 35. PCA PWM Mode

FLASH EPROM MEMORY

GENERAL DESCRIPTION

The P89C51RA2/RB2/RC2/RD2xx Flash memory augments EPROM functionality with in-circuit electrical erasure and programming. The Flash can be read and written as bytes. The Chip Erase operation will erase the entire program memory. The Block Erase function can erase any Flash block. In-system programming and standard parallel programming are both available. On-chip erase and write timing generation contribute to a user friendly programming interface.

The P89C51RA2/RB2/RC2/RD2xx Flash reliably stores memory contents even after 10,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The P89C51RA2/RB2/RC2/RD2xx uses a +5 V V_{PP} supply to perform the Program/Erase algorithms.

FEATURES – IN-SYSTEM PROGRAMMING (ISP) AND IN-APPLICATION PROGRAMMING (IAP)

- Flash EPROM internal program memory with Block Erase.
- Internal 1-kbyte fixed BootROM, containing low-level in-system programming routines and a default serial loader. User program can call these routines to perform In-Application Programming (IAP). The BootROM can be turned off to provide access to the full 64-kbyte Flash memory.
- Boot Vector allows user provided Flash loader code to reside anywhere in the Flash memory space. This configuration provides flexibility to the user.
- Default loader in BootROM allows programming via the serial port without the need for a user provided loader.
- Up to 64-kbyte external program memory if the internal program memory is disabled ($\overline{EA}$ = 0).
- Programming and erase voltage +5 V (+12 V tolerant).
- Read/Programming/Erase using ISP/IAP:
  - Byte Programming (8 μs).
  - Typical quick erase times:
    Block Erase (4 kbyte) in 3 seconds.
    Full Chip Erase:
    – RD2xx (64K) in 11 seconds
    – RC2 (32K) in 7 seconds
    – RB2 (16K) in 5 seconds
    – RA2 (4K) in 4 seconds
- Parallel programming with 87C51 compatible hardware interface to programmer.
- In-system programming (ISP).
- In-application programming (IAP).
- Programmable security for the code in the Flash.
- 10,000 minimum erase/program cycles for each byte.
- 10-year minimum data retention.

FLASH PROGRAMMING AND ERASURE

In general, there are three methods of erasing or programming of the Flash memory that may be used. First, the Flash may be programmed or erased in the end-user application by calling low-level routines through entry point in the BootROM. The end-user application, though, must be executing code from a different block than the block that is being erased or programmed. Second, the on-chip ISP boot loader may be invoked. This ISP boot loader will, in turn, call low-level routines through the common entry point in the BootROM that can be used by end-user applications. Third, the Flash may be programmed or erased using parallel method by using a commercially available EPROM programmer. The parallel programming method used by these devices is similar to that used by EPROM 87C51, but it is not identical, and the commercially available programmer will need to have support for these devices.

FLASH MEMORY SPACES

Flash User Code Memory Organization

The P89C51RA2/RB2/RC2/RD2xx contains 8KB/16KB/32KB/64KB Flash user code program memory organized into 4-kbyte blocks. ISP and IAP BootROM routines will support the new 4-kbyte block sizes through additional block number assignments while maintaining compatibility with previous 8-kbyte and 16-kbyte block assignments. This memory space is programmable via IAP, ISP, and parallel modes.

Status Byte/Boot Vector Block

This device includes a 4-kbyte block which contains the Status Byte and Boot Vector (Status Byte Block) . The Status Byte and Boot Vector are programmable via IAP, ISP, and parallel modes. Note that erasing of either the Status Byte and Boot Vector will erase the entire contents of this block. Thus the Status Byte and Boot Vector are erased together but are programmable separately.

Security & User Configuration Block

This device includes a 4-kbyte block (Security Block) which contains the Security Bits, the 6-clock/12-clock Flash-based clock mode bit FX2, and 4095 user programmable bytes. This block is programmable via IAP, ISP, and parallel modes. Security bits will prevent, as required, parallel programmers from reading or writing, however, IAP or ISP inhibitions will be software controlled. This block may only be erased using full-chip erase functions in ISP, IAP, or parallel mode. This security feature protects against software piracy and prevents the contents of the Flash from being read. The Security bits are located in the Flash. There are three programmable security bits that will provide different levels of protection for the on-chip code and data (See Table 11). The 4095 user programmable bytes are not part of user code memory are intended to be programmed or read through IAP, ISP, or parallel programmer functions.

The 6-clock/12-clock Flash-based clock mode bit FX2 will be latched at power-on. This allows the bit to be changed via IAP or ISP and delay taking effect until the next reset. This avoids changing baud rates during ISP operations.

Boot ROM

When the microcontroller programs its Flash memory, all of the low level details are handled by code that is contained in a 1-kbyte

BootROM that is shadowed over a portion of the user code memory space. A user program simply calls the common entry point with appropriate parameters in the BootROM to accomplish the desired operation. BootROM operations include: erase block, program byte, verify byte, program security bit, etc. The BootROM overlays the program memory space at the top of the address space from FC00 to FFFF hex, when it is enabled. The BootROM may be turned off so that the upper 1 kbyte of user program memory is accessible for execution.

Clock Mode

The clock mode feature sets operating frequency to be 1/12 or 1/6 of the oscillator frequency. The clock mode configuration bit, FX2, is located in the Security Block (See Table 8). FX2, when programmed, will override the SFR clock mode bit (X2) in the CKCON register. If FX2 is erased, then the SFR bit (X2) may be used to select between 6-clock and 12-clock mode.

Table 8.

CLOCK MODE CONFIG BIT (FX2)	X2 bit in CKCON	DESCRIPTION
erased	0	12-clock mode (default)
erased	1	6-clock mode
programmed	x	6-clock mode

NOTE:
1. Default clock mode after ChipErase is set to SFR selection.

FLASH MEMORY SPACES

Flash User Code Memory Organization

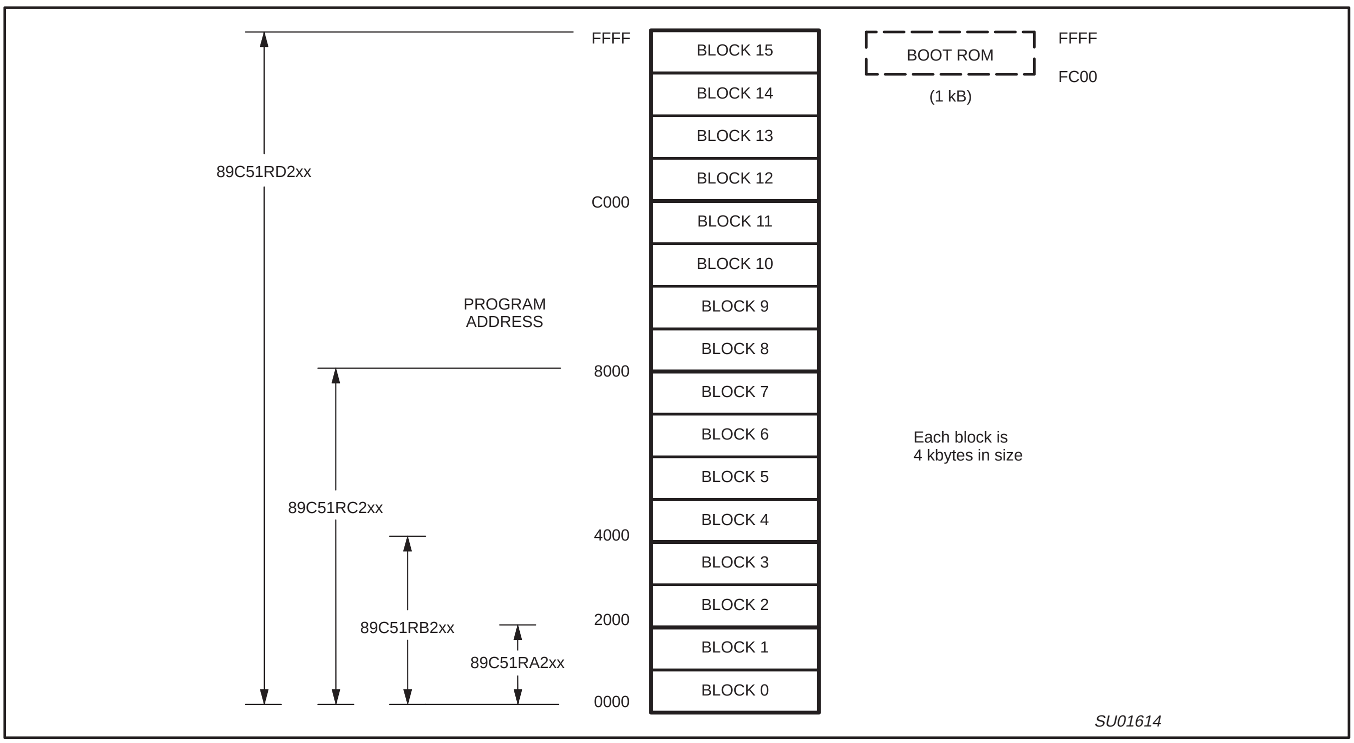


Figure 40. Flash Memory Configurations

Power-On Reset Code Execution

The P89C51RA2/RB2/RC2/RD2xx contains two special Flash registers: the BOOT VECTOR and the STATUS BYTE. At the falling edge of reset, the P89C51RA2/RB2/RC2/RD2xx examines the contents of the Status Byte. If the Status Byte is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Status Byte is set to a value other than zero, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 0FCH, corresponds to the address 0FC00H for the factory masked-ROM ISP boot loader. A custom boot loader can be written with the Boot Vector set to the custom boot loader.

NOTE: When erasing the Status Byte or Boot Vector, both bytes are erased at the same time. It is necessary to reprogram the Boot Vector after erasing and updating the Status Byte.

Table 9. Intel-Hex Records Used by In-System Programming

RECORD TYPE	COMMAND/DATA FUNCTION

00	Program Data
	`:nnaaaa00dd....ddcc`
	Where:
	`nn       = number of bytes (hex) in record`
	`aaaa     = memory address of first byte in record`
	`dd....dd = data bytes`
	`cc       = checksum`
	Example:
	`:10008000AF5F67F0602703E0322CFA92007780C3FD`

01	End of File (EOF), no operation
	`:xxxxxx01cc`
	Where:
	`xxxxxx   = required field, but value is a "don't care"`
	`cc       = checksum`
	Example:
	`:00000001FF`

03	Miscellaneous Write Functions
	`:nnxxxx03ffssddcc`
	Where:
	`nn       = number of bytes (hex) in record`
	`xxxx     = required field, but value is a "don't care"`
	`03       = Write Function`
	`ff       = subfunction code`
	`ss       = selection code`
	`dd       = data input (as needed)`
	`cc       = checksum`
	
	Subfunction Code = 01 (Erase 8K/16K Code Blocks)
	`ff = 01`
	`ss = block code as shown below:`
	`block 0,  0k to  8k, 00H`
	`block 1,  8k to 16k, 20H     (RB2, RC2, RD2)`
	`block 2, 16k to 32k, 40H     (RC2, RD2)`
	`block 3, 32k to 48k, 80H     (RD2 only)`
	`block 4, 48k to 64k, C0H     (RD2 only)`
	Example:
	`:0200000301C03A  erase block 4`
	
	Subfunction Code = 04 (Erase Boot Vector and Status Byte)
	`ff = 04`
	`ss = don't care`
	Example:
	`:020000030400F7  erase boot vector and status byte`
	
	Subfunction Code = 05 (Program Security Bits)
	`ff = 05`
	`ss = 00 program security bit 1  (inhibit writing to Flash)`
	`01 program security bit 2  (inhibit Flash verify)`
	`02 program security bit 3  (disable external memory)`
	Example:
	`:020000030501F5  program security bit 2`
	
	Subfunction Code = 06 (Program Status Byte or Boot Vector)
	`ff = 06`
	`ss = 00 program status byte`
	`01 program boot vector`
	`02 program FX2 bit (dd = 80)`
	`dd = data`
	Example 1:
	`:030000030601FCF7  program boot vector with 0FCH`
	Example 2:
	`:0300000306028072  program FX2 bit (select 12-clock mode)`

<table>
<tr><th>RECORD TYPE</th><th>COMMAND/DATA FUNCTION</th></tr>
<tr><td>03 (Cont.)</td><td>Subfunction Code = 07 (Full Chip Erase)
Erases all blocks, security bits, and sets status byte and boot vector to default values
<pre>ff = 07
ss = don’t care
dd = don’t care</pre>Example:
<pre>:0100000307F5 full chip erase</pre>Subfunction Code = 0C (Erase 4K Blocks)
<pre>ff = 0C
ss = block code as shown below:
        Block 0 , 0k~4k , 00H
        Block 1 , 4k~8k , 10H
        Block 2 , 8k~12k , 20H   (only available on RD2 / RC2 / RB2)
        Block 3 , 12k~16k , 30H   (only available on RD2 / RC2 / RB2)
        Block 4 , 16k~20k , 40H   (only available on RD2 / RC2)
        Block 5 , 20k~24k , 50H   (only available on RD2 / RC2)
        Block 6 , 24k~28k , 60H   (only available on RD2 / RC2)
        Block 7 , 28k~32k , 70H   (only available on RD2 / RC2)
        Block 8 , 32k~36k , 80H   (only available on RD2)
        Block 9 , 36k~40k , 90H   (only available on RD2)
        Block 10, 40k~44k , A0H   (only available on RD2)
        Block 11, 44k~48k , B0H   (only available on RD2)
        Block 12, 48k~52k , C0H   (only available on RD2)
        Block 13, 52k~56k , D0H   (only available on RD2)
        Block 14, 56k~60k , E0H   (only available on RD2)
        Block 15, 60k~64k , F0H   (only available on RD2)</pre>Example:
<pre>:020000030C20CF (Erase 4k block #2)</pre></td></tr>
<tr><td>04</td><td>Display Device Data or Blank Check – Record type 04 causes the contents of the entire Flash array to be sent out the serial port in a formatted display. This display consists of an address and the contents of 16 bytes starting with that address. No display of the device contents will occur if security bit 2 has been programmed. Data to the serial port is initiated by the reception of any character and terminated by the reception of any character.

General Format of Function 04
<pre>:05xxxx04sssseeeeffcc</pre>Where:
<pre>05   = number of bytes (hex) in record
xxxx   = required field, but value is a “don’t care”
04   = “Display Device Data or Blank Check” function code
ssss   = starting address
eeee   = ending address
ff   = subfunction
           00 = display data
           01 = blank check
           02 = display data in data block (valid addresses: 0001~0FFFH)
cc   = checksum</pre>Example 1:
<pre>:0500000440004FFF0069 display 4000–4FFF</pre>Example 2:
<pre>:0500000400000FFF02E7 display data in data block
  (the data at address 0000 is invalid)</pre></td></tr>
</table>

IAP CALL	PARAMETER

PROGRAM SECURITY BITS	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 05h or R1 = 85h (WDT feed)`
	`DPH = 00h`
	`DPL = 00h , security bit #1`
	`DPL = 01h , security bit #2`
	`DPL = 02h , security bit #3`
	Return Parameter:
	`ACC = 00 if pass , !=0 if fail`

PROGRAM STATUS BYTE	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 06h or R1 = 86h (WDT feed)`
	`DPH = 00h`
	`DPL = 00H - program status byte`
	`ACC = status byte`
	Return Parameter:
	`ACC = 00 if pass , !=0 if fail`

PROGRAM BOOT VECTOR	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 06h or R1 = 86h (WDT feed)`
	`DPH = 00h`
	`DPL = 01H - program boot vector`
	`ACC = boot vector`
	Return Parameter:
	`ACC = 00 if pass , !=0 if fail`

PROGRAM 6–CLK/12–CLK CONFIGURATION BIT (New function)	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 06h or R1 = 86h (WDT feed)`
	`DPH = 00h`
	`DPL = 02H - program config bit`
	`ACC = 80H (MSB = 6clk/12clk bit)`
	Return Parameter:
	`ACC = 00 if pass , !=0 if fail`

PROGRAM DATA BLOCK (New function)	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 0Dh or R1 = 8Dh (WDT feed)`
	`DPTR = address of byte to program`
	`(valid addresses = 0001h~0FFFh)`
	`ACC = data`
	Return Parameter:
	`ACC = 00 if pass , !=0 if fail`

READ DEVICE DATA	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 03h or R1 = 83h (WDT feed)`
	`DPTR = address of byte to read`
	Return Parameter:
	`ACC = value of byte read`

READ DATA BLOCK (New function)	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 0Eh or R1 = 8Eh (WDT feed)`
	`DPTR = address of byte to read`
	`(valid addresses = 0001h~0FFFh)`
	Return Parameter:
	`ACC = value of byte read`

READ MANUFACTURER ID	Input Parameter:
	`R0 = osc freq (integer)`
	`R1 = 00h or R1 = 80h (WDT feed)`
	`DPH = 00h`
	`DPL = 00h - read manufacturer ID`
	Return Parameter:
	`ACC = value of byte read`

Security

The security feature protects against software piracy and prevents the contents of the Flash from being read. The Security Lock bits are located in Flash. The P89C51RA2/RB2/RC2/RD2xx has three programmable security lock bits that will provide different levels of protection for the on-chip code and data (see Table 11).

Table 11.

	SECURITY LOCK BITS[1]			PROTECTION DESCRIPTION
LEVEL	LB1	LB2	LB3	
1	0	0	0	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory.
2	1	0	0	Block erase is disabled. Erase or programming of the status byte or boot vector is disabled.
3	1	1	0	Verify of code memory is disabled.
4	1	1	1	External execution is disabled.

NOTE:
1. Security bits are independent of each other. Full-chip erase may be performed regardless of the state of the security bits.
2. Any other combination of lock bits is undefined.
3. Setting LBx doesn’t prevent programming of unprogrammed bits.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

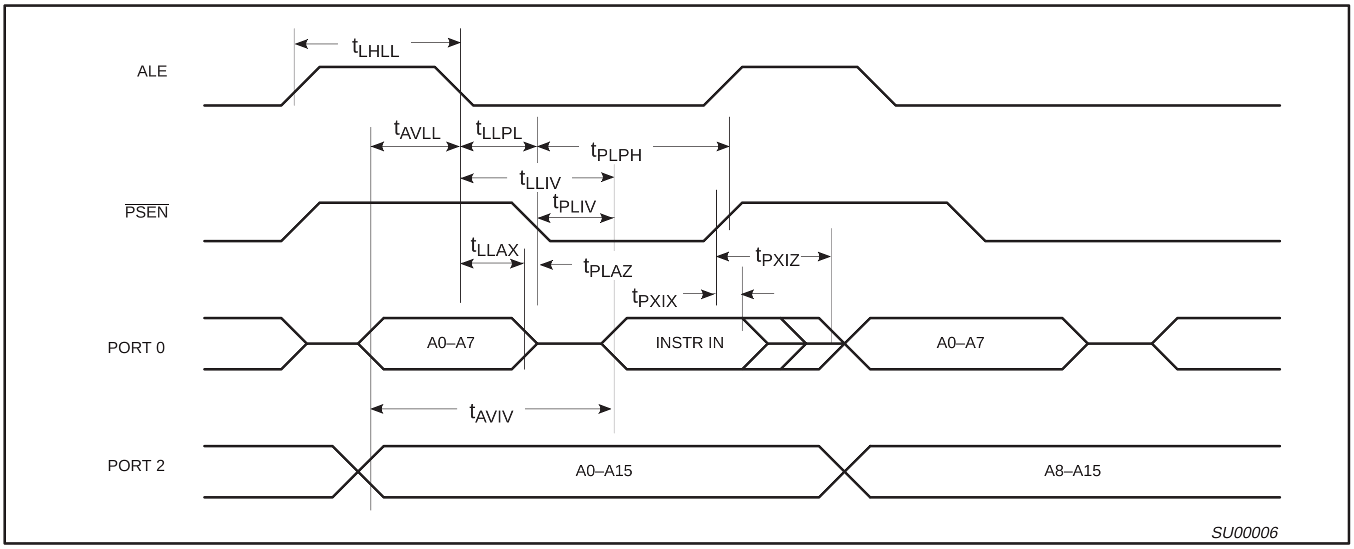


Figure 42. External Program Memory Read Cycle

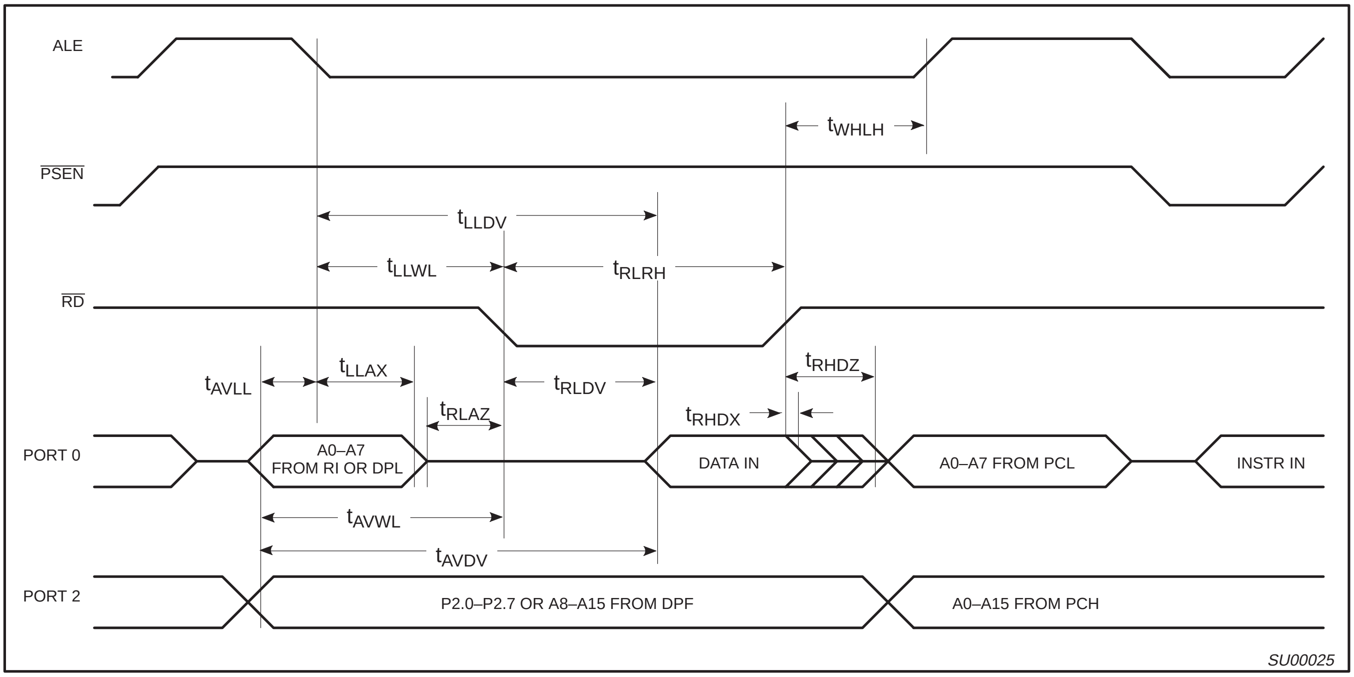
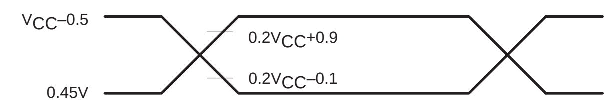


Figure 43. External Data Memory Read Cycle



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic ‘1’ and 0.45V for a logic ‘0’. Timing measurements are made at V_{IH} min for a logic ‘1’ and V_{IL} max for a logic ‘0’.

SU00717

Figure 47. AC Testing Input/Output

NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20mA$.

SU00718

Figure 48. Float Waveform

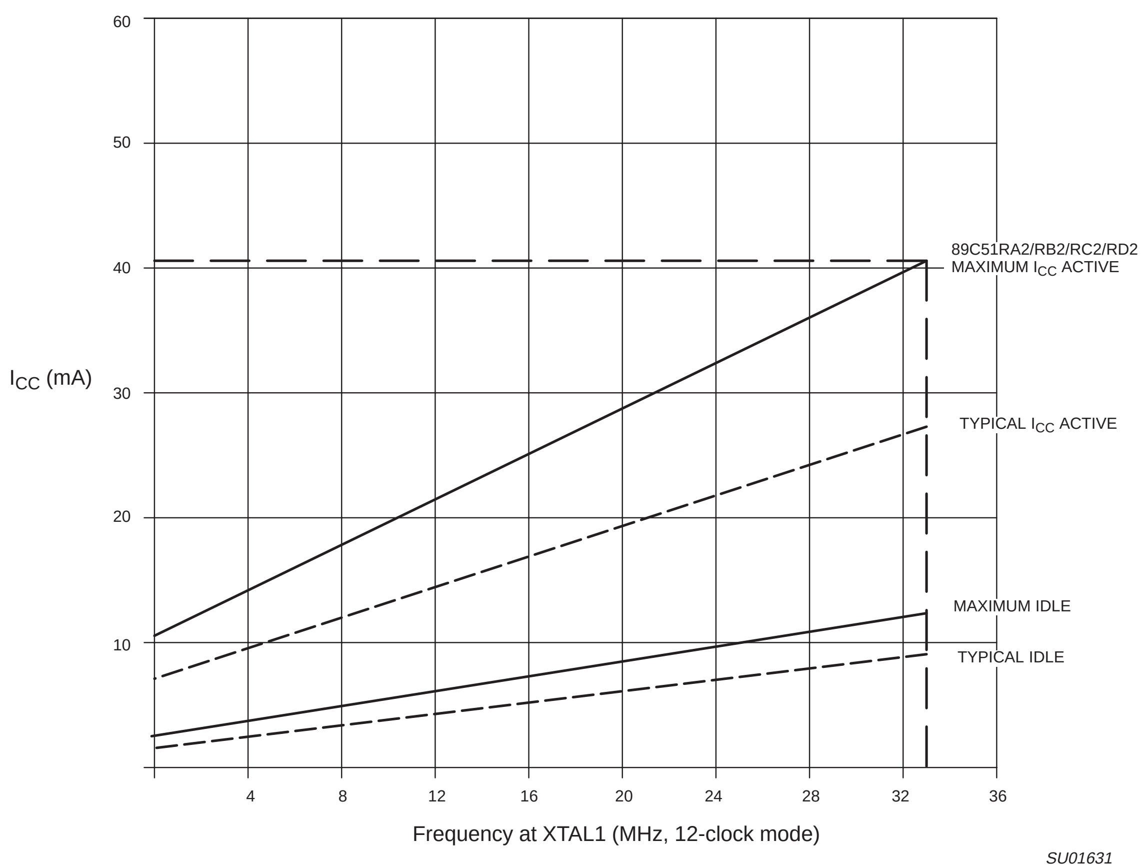


Figure 49. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

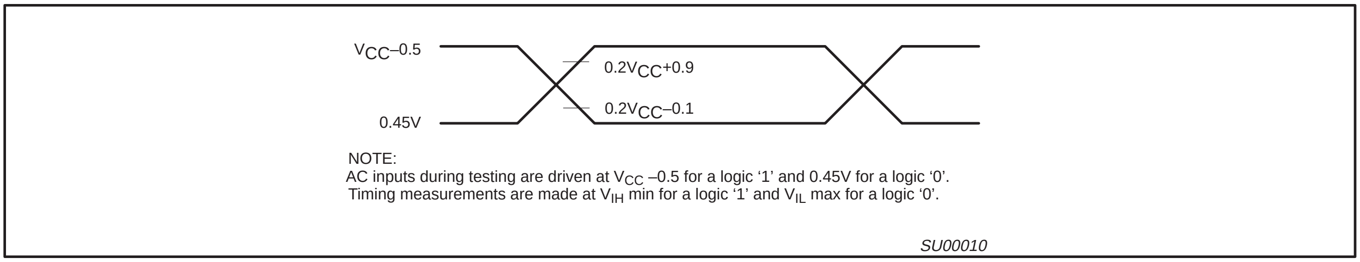


Figure 50. AC Testing Input/Output

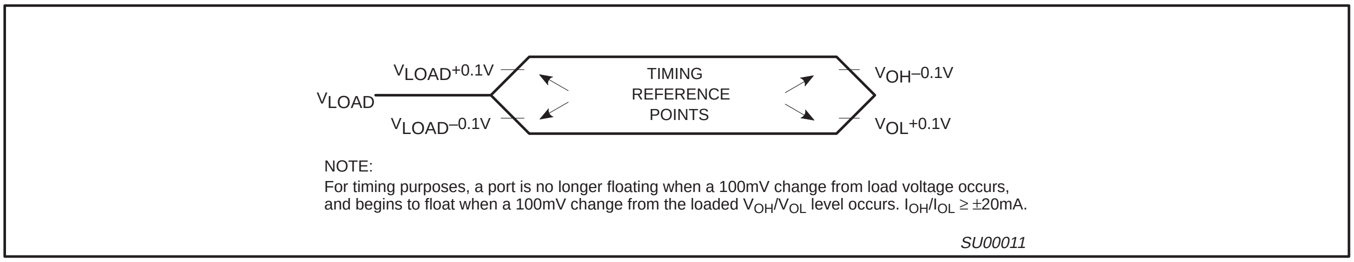


Figure 51. Float Waveform