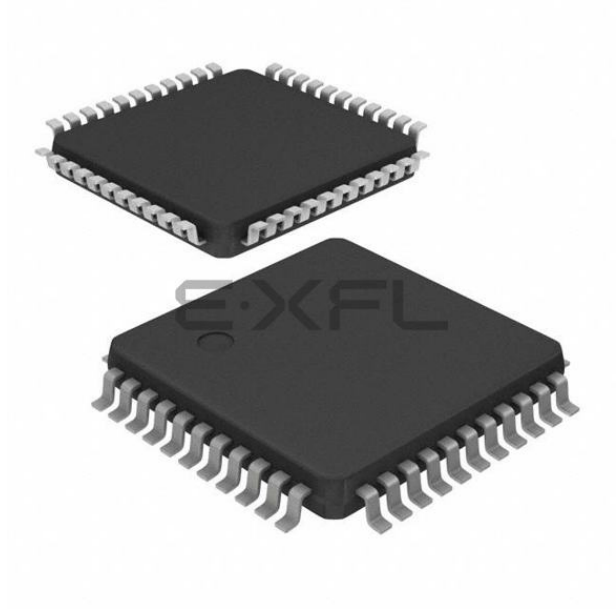


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89c51rc2fbd-01-55

DESCRIPTION

The P89C51RA2/RB2/RC2/RD2xx contains a non-volatile 8KB/16KB/32KB/64KB Flash program memory that is both parallel programmable and serial In-System and In-Application Programmable. In-System Programming (ISP) allows the user to download new code while the microcontroller sits in the application. In-Application Programming (IAP) means that the microcontroller fetches new program code and reprograms itself while in the system. This allows for remote programming over a modem link. A default serial loader (boot loader) program in ROM allows serial In-System programming of the Flash memory via the UART without the need for a loader in the Flash code. For In-Application Programming, the user program erases and reprograms the Flash memory by use of standard routines contained in ROM.

The device supports 6-clock/12-clock mode selection by programming a Flash bit using parallel programming or In-System Programming. In addition, an SFR bit (X2) in the clock control register (CKCON) also selects between 6-clock/12-clock mode.

Additionally, when in 6-clock mode, peripherals may use either 6 clocks per machine cycle or 12 clocks per machine cycle. This choice is available individually for each peripheral and is selected by bits in the CKCON register.

This device is a Single-Chip 8-Bit Microcontroller manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The instruction set is 100% compatible with the 80C51 instruction set.

The device also has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits.

The added features of the P89C51RA2/RB2/RC2/RD2xx make it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

FEATURES

- 80C51 Central Processing Unit
- On-chip Flash Program Memory with In-System Programming (ISP) and In-Application Programming (IAP) capability
- Boot ROM contains low level Flash programming routines for downloading via the UART
- Can be programmed by the end-user application (IAP)
- Parallel programming with 87C51 compatible hardware interface to programmer
- Supports 6-clock/12-clock mode via parallel programmer (default clock mode after ChipErase is 12-clock)
- 6-clock/12-clock mode Flash bit erasable and programmable via ISP
- 6-clock/12-clock mode programmable “on-the-fly” by SFR bit
- Peripherals (PCA, timers, UART) may use either 6-clock or 12-clock mode while the CPU is in 6-clock mode
- Speed up to 20 MHz with 6-clock cycles per machine cycle (40 MHz equivalent performance); up to 33 MHz with 12 clocks per machine cycle
- Fully static operation
- RAM expandable externally to 64 kbytes
- Four interrupt priority levels
- Seven interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Clock can be stopped and resumed
  - Idle mode
  - Power down mode
- Programmable clock-out pin
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Programmable Counter Array (PCA)
  - PWM
  - Capture/compare

SELECTION TABLE

Type	Memory				Timers				Serial Interfaces				ADC bits/ch.	I/O Pins	Interrupts (Ext.)/Levels	Program Security	Default Clock Rate [1]	Optional Clock Rate [1]	Reset active low/high?	Max. Freq. at 6-clk / 12-clk (MHz)	Freq. Range at 3V (MHz)	Freq. Range at 5V (MHz)
	RAM	ROM	OTP	Flash	# of Timers	PWM	PCA	WD	UART	I2C	CAN	SPI										
P89C51RD2xx	1K	–	–	64K	4	√	√	√	√	–	–	–	–	32	7(2)/4	√	12-clk	6-clk	H	20/33	–	0-20/33
P89C51RC2xx	512B	–	–	32K	4	√	√	√	√	–	–	–	–	32	7(2)/4	√	12-clk	6-clk	H	20/33	–	0-20/33
P89C51RB2xx	512B	–	–	16K	4	√	√	√	√	–	–	–	–	32	7(2)/4	√	12-clk	6-clk	H	20/33	–	0-20/33
P89C51RA2xx	512B	–	–	8K	4	√	√	√	√	–	–	–	–	32	7(2)/4	√	12-clk	6-clk	H	20/33	–	0-20/33

NOTE:
1. P89C51Rx2Hxx devices have a 6-clk default clock rate (12-clk optional). Please also see Device Comparison Table.

DEVICE COMPARISON TABLE

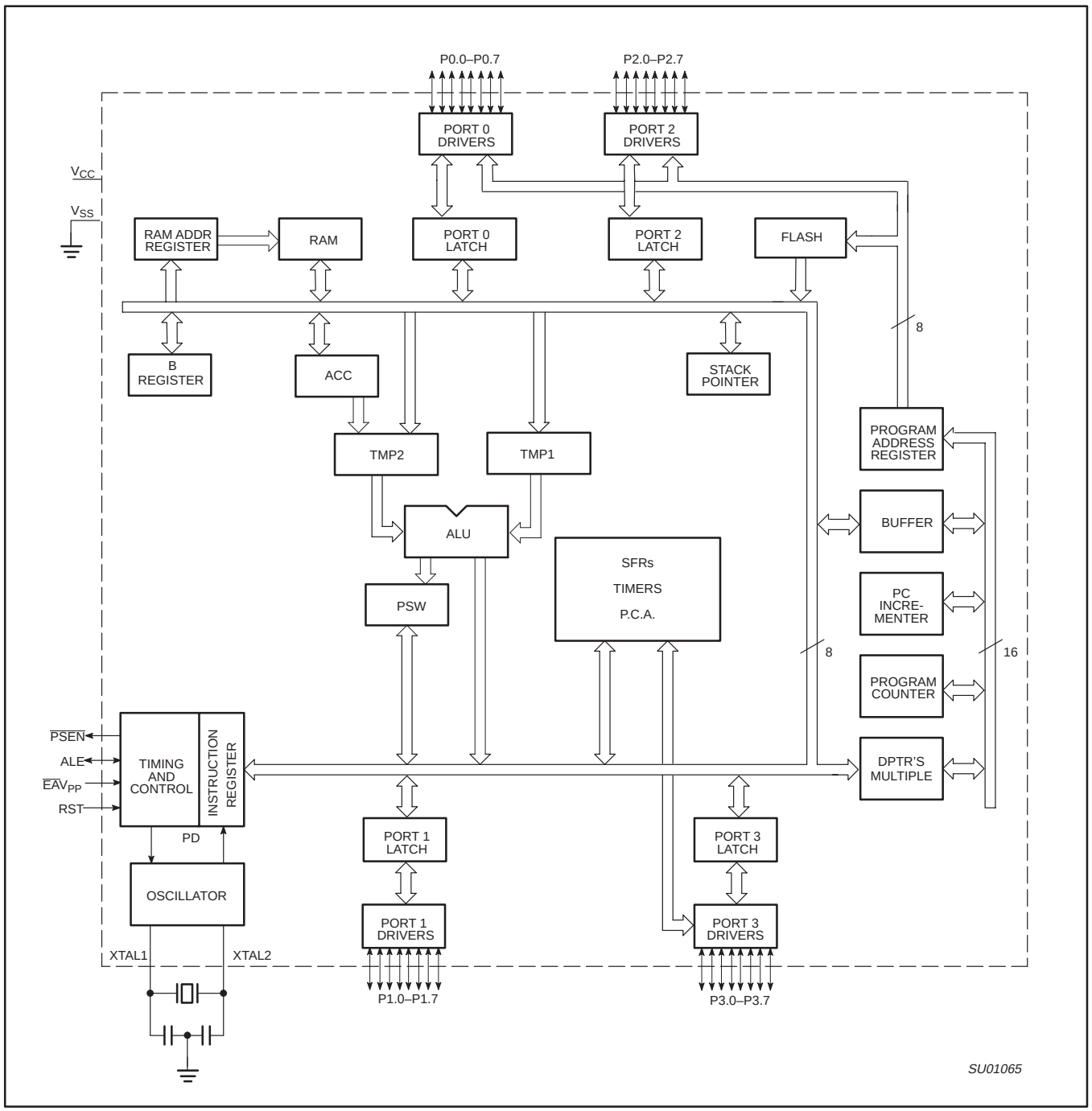
Item	1st generation of Rx2 devices	2nd generation of Rx2 devices (this data sheet)	Difference
Type description	P89C51Rx2**H**xx(x)	P89C51Rx2xx(x)	No more letter 'H'
Programming algorithm	When using a parallel programmer, be sure to select P89C51Rx2**H**xx(x) devices	When using a parallel programmer, be sure to select P89C51Rx2xx(x) devices (no more letter 'H')	Different programming algorithm due to process change
Clock mode (I)	**6-clk default, OTP** configuration bit to program to **12-clk** mode using parallel programmer (**cannot** be programmed back to 6-clk)	**12-clk default, Flash** configuration bit to program to **6-clk** mode using parallel programmer or ISP (**can** be reprogrammed)	More flexibility for the end user, more compatibility to older P89C51Rx+ parts
Clock mode (II)	N/A	6-clock/12-clock mode programmable "on the fly" by SFR bit X2 (CKCON.0)	Clock mode can be changed by software
Peripheral clock modes	N/A	Peripherals can be run in 12-clk mode while CPU runs in 6-clk mode	More flexibility, lower power consumption
Flash block structure	Two 8-Kbyte blocks 1–3 16-Kbyte blocks	2–16 4-Kbyte blocks	More flexibility

ORDERING INFORMATION

	PART ORDER NUMBER[1]	MEMORY		TEMPERATURE RANGE (°C) AND PACKAGE	VOLTAGE RANGE	FREQUENCY (MHz)		DWG #
		FLASH	RAM			6-CLOCK MODE	12-CLOCK MODE	
1.	P89C51RA2BA/01	8 KB	512 B	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
2.	P89C51RA2BBD/01	8 KB	512 B	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
3.	P89C51RB2BA/01	16 KB	512 B	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
4.	P89C51RB2BBD/01	16 KB	512 B	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
5.	P89C51RC2BN/01	32 KB	512 B	0 to +70, PDIP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT129-1
6.	P89C51RC2BA/01	32 KB	512 B	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
7.	P89C51RC2FA/01	32 KB	512 B	–40 to +85, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
8.	P89C51RC2BBD/01	32 KB	512 B	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
9.	P89C51RC2FBD/01	32 KB	512 B	–40 to +85, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
10.	P89C51RD2BN/01	64 KB	1024 B	0 to +70, PDIP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT129-1
11.	P89C51RD2BA/01	64 KB	1024 B	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
12.	P89C51RD2BBD/01	64 KB	1024 B	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
13.	P89C51RD2FA/01	64 KB	1024 B	–40 to +85, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2

NOTE:
1. The Part Marking will not include the "/01".

BLOCK DIAGRAM – CPU ORIENTED



TIMER 0 AND TIMER 1 OPERATION

Timer 0 and Timer 1

The "Timer" or "Counter" function is selected by control bits C/$\overline{T}$ in the Special Function Register TMOD. These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 2 shows the Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The counted input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Figure 3).

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

Mode 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 4. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which is preset by software. The reload leaves THn unchanged.

Mode 2 operation is the same for Timer 0 as for Timer 1.

Mode 3

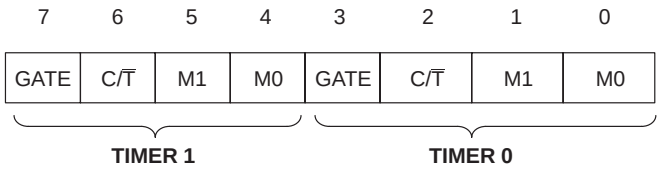
Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 5. TL0 uses the Timer 0 control bits: C/$\overline{T}$, GATE, TR0, and TF0 as well as pin $\overline{INT0}$. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the "Timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer on the counter. With Timer 0 in Mode 3, an 80C51 can look like it has three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

TMOD Address = 89H Reset Value = 00H

Not Bit Addressable



BIT	SYMBOL	FUNCTION
TMOD.3/ TMOD.7	GATE	Gating control when set. Timer/Counter "n" is enabled only while "$\overline{INTn}$" pin is high and "TRn" control pin is set. when cleared Timer "n" is enabled whenever "TRn" control bit is set.
TMOD.2/ TMOD.6	C/$\overline{T}$	Timer or Counter Selector cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from "Tn" input pin).

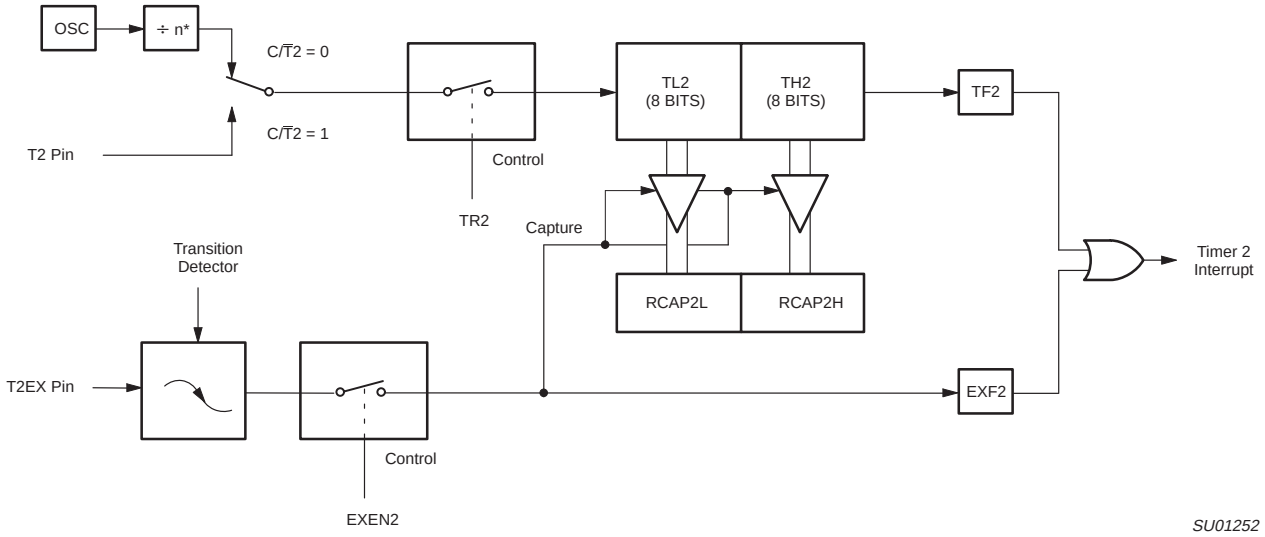
M1	M0	OPERATING
0	0	8048 Timer: "TLn" serves as 5-bit prescaler.
0	1	16-bit Timer/Counter: "THn" and "TLn" are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter: "THn" holds a value which is to be reloaded into "TLn" each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped.

SU01580

Figure 1. Timer/Counter 0/1 Mode Control (TMOD) Register

Table 3. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)



* n = 6 in 6-clock mode, or 12 in 12-clock mode.

Figure 7. Timer 2 in Capture Mode

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T2OE	DCEN
Bit 7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.*
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU00729

Figure 8. Timer 2 Mode (T2MOD) Control Register

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Summary of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{OSC}}{[\ n^* \times [65536 - (\text{RCAP2H, RCAP2L})]]}$$

* n = 16 in 6-clock mode
32 in 12-clock mode

Where f_{OSC}= Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 - \left(\frac{f_{OSC}}{n^* \times \text{Baud Rate}}\right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. see Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:
1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

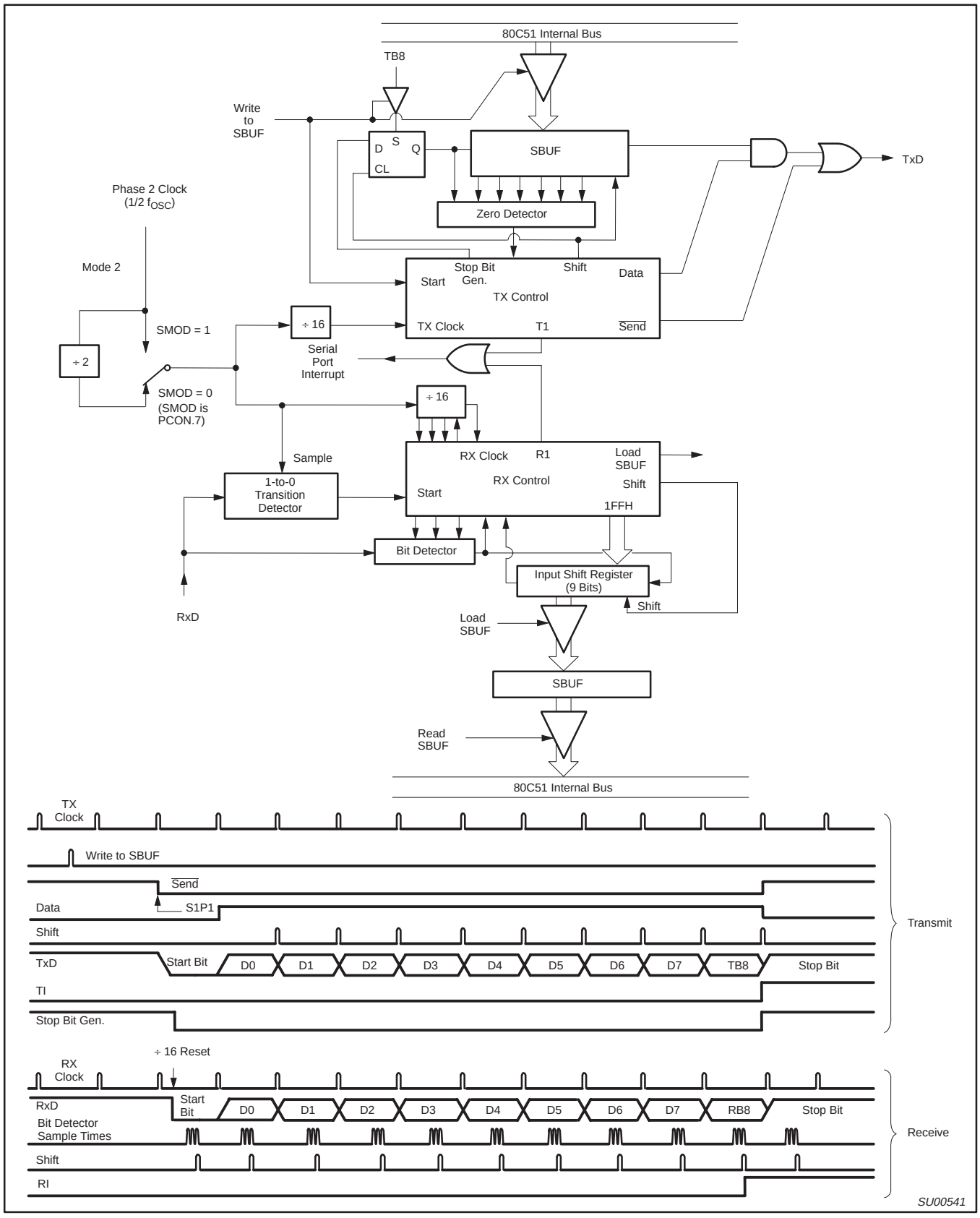


Figure 16. Serial Port Mode 2

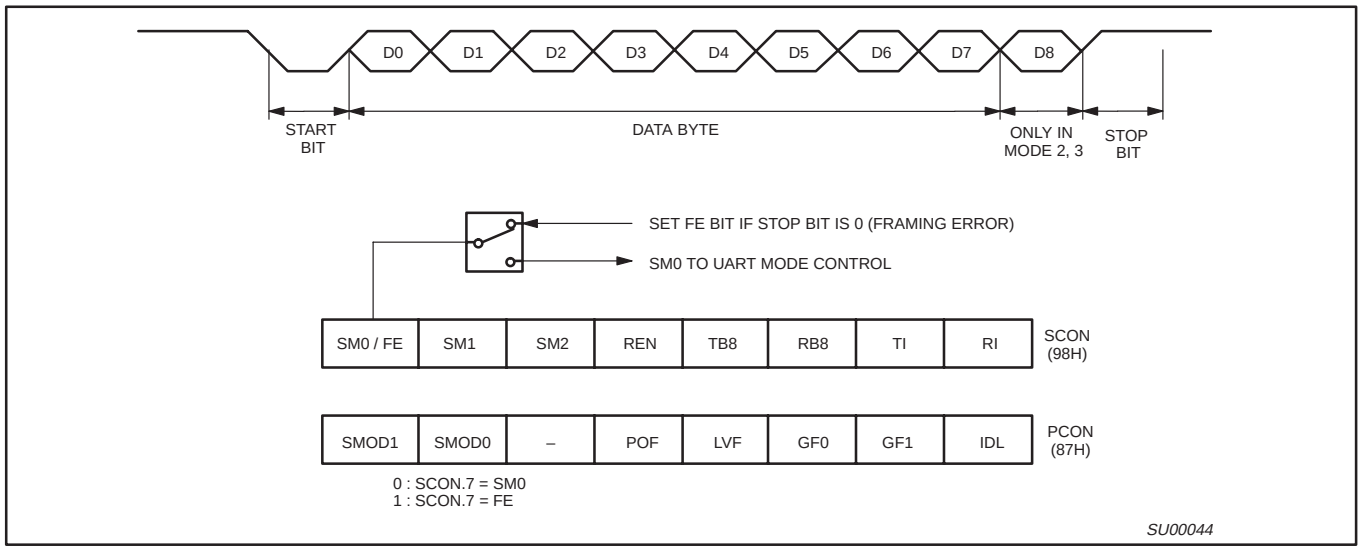


Figure 19. UART Framing Error Detection

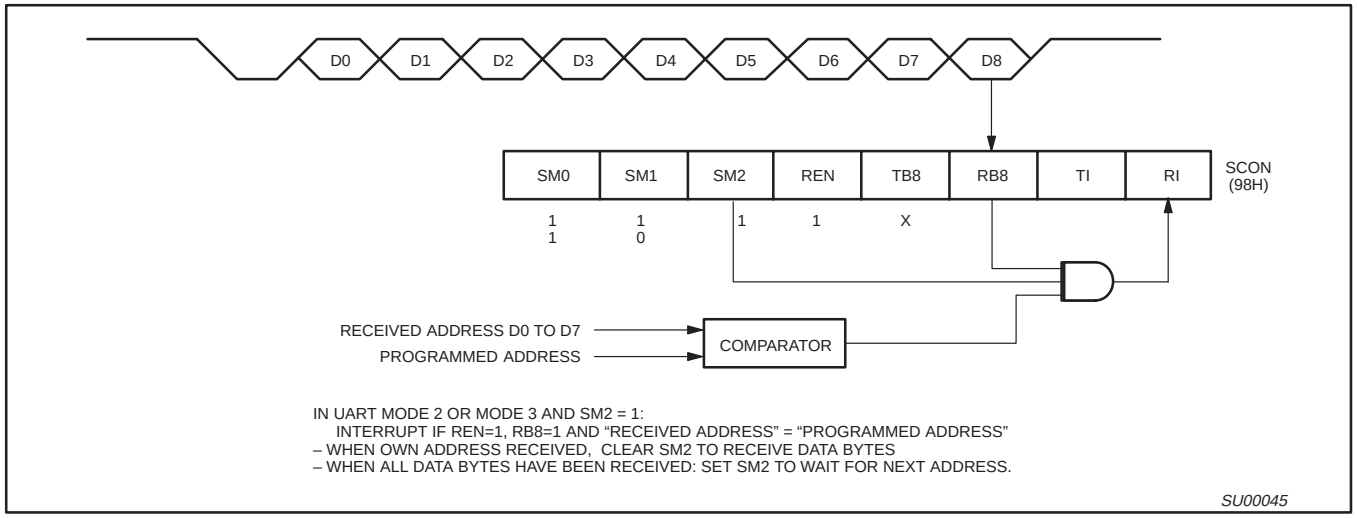


Figure 20. UART Multiprocessor Communication, Automatic Address Recognition

Interrupt Priority Structure

The P89C51RA2/RB2/RC2/RD2xx has a 7 source four-level interrupt structure (see Table 7).

There are 3 SFRs associated with the four-level interrupt. They are the IE, IP, and IPH. (See Figures 21, 22, and 23.) The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 23.

The function of the IPH SFR, when combined with the IP SFR, determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L)[1] Y (T)[2]	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
PCA	5	CF, CCFn n = 0–4	N	33H
SP	6	RI, TI	N	23H
T2	7	TF2, EXF2	N	2BH

NOTES:
1. L = Level activated
2. T = Transition activated

	7	6	5	4	3	2	1	0
IE (0A8H)	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

BIT	SYMBOL	FUNCTION
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
IE.6	EC	PCA interrupt enable bit
IE.5	ET2	Timer 2 interrupt enable bit.
IE.4	ES	Serial Port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt 1 enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt 0 enable bit.

SU01290

Figure 21. IE Registers

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output unless the CPU needs to perform an off-chip memory access.

Reduced EMI Mode

AUXR (8EH)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	EXTRAM	AO

AUXR.1 EXTRAM
AUXR.0 AO

See more detailed description in Figure 38.

Dual DPTR

The dual DPTR structure (see Figure 24) is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxxxxxx0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
–	–	ENBOOT	–	GF2	0	–	DPS

Where:
DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

The GF2 bit is a general purpose user-defined flag. Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the GF2 bit.

The ENBOOT bit determines whether the BOOTROM is enabled or disabled. This bit will automatically be set if the status byte is non zero during reset or $\overline{PSEN}$ is pulled low, ALE floats high, and EA > V_{IH} on the falling edge of reset. Otherwise, this bit will be cleared during reset.

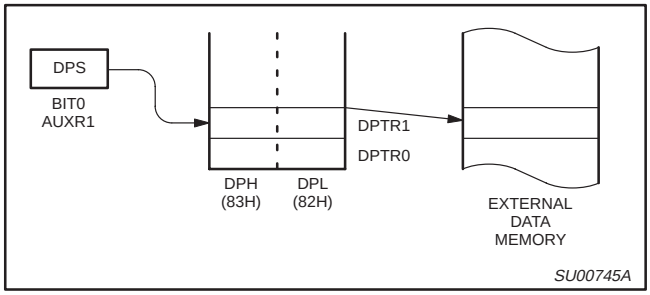


Figure 24.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR , A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See *Application Note AN458* for more details.

Programmable Counter Array (PCA)

The Programmable Counter Array available on the P89C51RA2/RB2/RC2/RD2xx is a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1.4 (CEX1), etc. The basic PCA configuration is shown in Figure 25.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 28):

CPS1	CPS0	PCA Timer Count Source
0	0	1/6 oscillator frequency (6-clock mode); 1/12 oscillator frequency (12-clock mode)
0	1	1/2 oscillator frequency (6-clock mode); 1/4 oscillator frequency (12-clock mode)
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 26.

The watchdog timer function is implemented in module 4 (see Figure 35).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 29). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 27.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 30). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 31 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

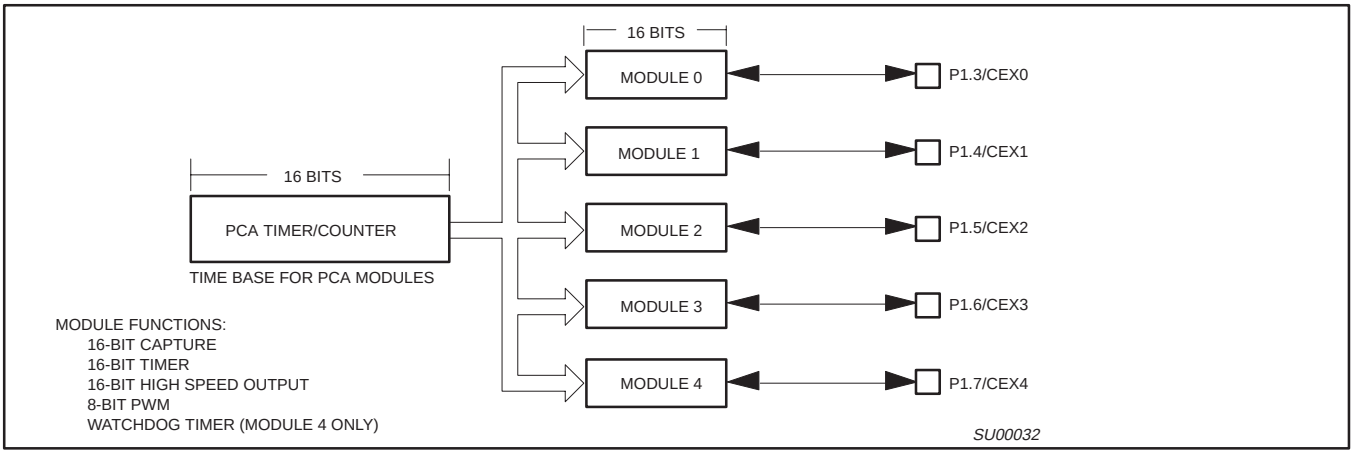


Figure 25. Programmable Counter Array (PCA)

CCAPMn Address CCAPM0 0DAH
CCAPM1 0DBH
CCAPM2 0DCH
CCAPM3 0DDH
CCAPM4 0DEH

Reset Value = X000 0000B

Not Bit Addressable

	–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use*.
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

SU01320

Figure 30. CCAPMn: PCA Modules Compare/Capture Registers

–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 31. PCA Module Modes (CCAPMn Register)

PCA Capture Mode
To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated. Refer to Figure 32.

16-bit Software Timer Mode
The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 33).

High Speed Output Mode
In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 34).

Pulse Width Modulator Mode
All of the PCA modules can be used as PWM outputs. Figure 35 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. the allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

IAP CALL	PARAMETER
READ DEVICE ID #1	Input Parameter: R0 = osc freq (integer) R1 = 00h or R1 = 80h (WDT feed) DPH = 00h DPL = 01h - read device ID #1 Return Parameter: ACC = value of byte read
READ DEVICE ID #2	Input Parameter: R0 = osc freq (integer) R1 = 00h or R1 = 80h (WDT feed) DPH = 00h DPL = 02h - read device ID #2 Return Parameter: ACC = value of byte read
READ SECURITY BITS	Input Parameter: R0 = osc freq (integer) R1 = 07h or R1 = 87h (WDT feed) DPH = 00h DPL = 00h - read lock byte Return Parameter: ACC = value of byte read
READ STATUS BYTE	Input Parameter: R0 = osc freq (integer) R1 = 07h or R1 = 87h (WDT feed) DPH = 00h DPL = 01h - read status byte Return Parameter: ACC = value of byte read
READ BOOT VECTOR	Input Parameter: R0 = osc freq (integer) R1 = 07h or R1 = 87h (WDT feed) DPH = 00h DPL = 02h - read boot vector Return Parameter: ACC = value of byte read
READ CONFIG (New function)	Input Parameter: R0 = osc freq (integer) R1 = 00h or R1 = 80h (WDT feed) DPH = 00h DPL = 03h - read config byte Return Parameter: ACC = value of byte read
READ REVISION (New function)	Input Parameter: R0 = osc freq (integer) R1 = 00h or R1 = 80h (WDT feed) DPH = 00h DPL = 80h - read revision of ROM Code Return Parameter: ACC = value of byte read

AC ELECTRICAL CHARACTERISTICS (12-CLOCK MODE)

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C; V_{CC} = 5 V ± 10%, V_{SS} = 0 V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[4]		33 MHz CLOCK[4]		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	42	Oscillator frequency	0	33			MHz
t_{LHLL}	42	ALE pulse width	$2t_{CLCL}$–40		21		ns
t_{AVLL}	42	Address valid to ALE low	t_{CLCL}–25		5		ns
t_{LLAX}	42	Address hold after ALE low	t_{CLCL}–25		5		ns
t_{LLIV}	42	ALE low to valid instruction in		$4t_{CLCL}$–65		55	ns
t_{LLPL}	42	ALE low to $\overline{PSEN}$ low	t_{CLCL}–25		5		ns
t_{PLPH}	42	$\overline{PSEN}$ pulse width	$3t_{CLCL}$–45		45		ns
t_{PLIV}	42	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}$–60		30	ns
t_{PXIX}	42	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	42	Input instruction float after $\overline{PSEN}$		t_{CLCL}–25		5	ns
t_{AVIV}	42	Address to valid instruction in		$5t_{CLCL}$–80		70	ns
t_{PLAZ}	42	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	43, 44	$\overline{RD}$ pulse width	$6t_{CLCL}$–100		82		ns
t_{WLWH}	43, 44	$\overline{WR}$ pulse width	$6t_{CLCL}$–100		82		ns
t_{RLDV}	43, 44	$\overline{RD}$ low to valid data in		$5t_{CLCL}$–90		60	ns
t_{RHDX}	43, 44	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	43, 44	Data float after $\overline{RD}$		$2t_{CLCL}$–28		32	ns
t_{LLDV}	43, 44	ALE low to valid data in		$8t_{CLCL}$–150		90	ns
t_{AVDV}	43, 44	Address to valid data in		$9t_{CLCL}$–165		105	ns
t_{LLWL}	43, 44	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}$–50	$3t_{CLCL}$+50	40	140	ns
t_{AVWL}	43, 44	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}$–75		45		ns
t_{QVWX}	43, 44	Data valid to $\overline{WR}$ transition	t_{CLCL}–30		0		ns
t_{WHQX}	43, 44	Data hold after $\overline{WR}$	t_{CLCL}–25		5		ns
t_{QVWH}	44	Data valid to $\overline{WR}$ high	$7t_{CLCL}$–130		80		ns
t_{RLAZ}	43, 44	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	43, 44	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL}–25	t_{CLCL}+25	5	55	ns
External Clock							
t_{CHCX}	46	High time	17	t_{CLCL}–t_{CLCX}			ns
t_{CLCX}	46	Low time	17	t_{CLCL}–t_{CHCX}			ns
t_{CLCH}	46	Rise time		5			ns
t_{CHCL}	46	Fall time		5			ns
Shift Register							
t_{XLXL}	45	Serial port clock cycle time	$12t_{CLCL}$		360		ns
t_{QVXH}	45	Output data setup to clock rising edge	$10t_{CLCL}$–133		167		ns
t_{XHQX}	45	Output data hold after clock rising edge	$2t_{CLCL}$–80		50		ns
t_{XHDX}	45	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	45	Clock rising edge to input data valid		$10t_{CLCL}$–133		167	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
3. Interfacing the microcontroller to devices with float times up to 45 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Parts are tested to 3.5 MHz, but guaranteed to operate down to 0 Hz.

AC ELECTRICAL CHARACTERISTICS (6-CLOCK MODE)

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C; V_{CC} = 5 V ± 10%, V_{SS} = 0 V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[4]		20 MHz CLOCK[4]		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	42	Oscillator frequency	0	20			MHz
t_{LHLL}	42	ALE pulse width	t_{CLCL}–40		10		ns
t_{AVLL}	42	Address valid to ALE low	$0.5t_{CLCL}$–20		5		ns
t_{LLAX}	42	Address hold after ALE low	$0.5t_{CLCL}$–20		5		ns
t_{LLIV}	42	ALE low to valid instruction in		$2t_{CLCL}$–65		35	ns
t_{LLPL}	42	ALE low to $\overline{PSEN}$ low	$0.5t_{CLCL}$–20		5		ns
t_{PLPH}	42	$\overline{PSEN}$ pulse width	$1.5t_{CLCL}$–45		30		ns
t_{PLIV}	42	$\overline{PSEN}$ low to valid instruction in		$1.5t_{CLCL}$–60		15	ns
t_{PXIX}	42	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	42	Input instruction float after $\overline{PSEN}$		$0.5t_{CLCL}$–20		5	ns
t_{AVIV}	42	Address to valid instruction in		$2.5t_{CLCL}$–80		45	ns
t_{PLAZ}	42	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	43, 44	$\overline{RD}$ pulse width	$3t_{CLCL}$–100		50		ns
t_{WLWH}	43, 44	$\overline{WR}$ pulse width	$3t_{CLCL}$–100		50		ns
t_{RLDV}	43, 44	$\overline{RD}$ low to valid data in		$2.5t_{CLCL}$–90		35	ns
t_{RHDX}	43, 44	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	43, 44	Data float after $\overline{RD}$		t_{CLCL}–20		5	ns
t_{LLDV}	43, 44	ALE low to valid data in		$4t_{CLCL}$–150		50	ns
t_{AVDV}	43, 44	Address to valid data in		$4.5t_{CLCL}$–165		60	ns
t_{LLWL}	43, 44	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$1.5t_{CLCL}$–50	$1.5t_{CLCL}$+50	25	125	ns
t_{AVWL}	43, 44	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$2t_{CLCL}$–75		25		ns
t_{QVWX}	43, 44	Data valid to $\overline{WR}$ transition	$0.5t_{CLCL}$–25		0		ns
t_{WHQX}	43, 44	Data hold after $\overline{WR}$	$0.5t_{CLCL}$–20		5		ns
t_{QVWH}	44	Data valid to $\overline{WR}$ high	$3.5t_{CLCL}$–130		45		ns
t_{RLAZ}	43, 44	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	43, 44	$\overline{RD}$ or $\overline{WR}$ high to ALE high	$0.5t_{CLCL}$–20	$0.5t_{CLCL}$+20	5	45	ns
External Clock							
t_{CHCX}	46	High time	20	t_{CLCL}–t_{CLCX}			ns
t_{CLCX}	46	Low time	20	t_{CLCL}–t_{CHCX}			ns
t_{CLCH}	46	Rise time		5			ns
t_{CHCL}	46	Fall time		5			ns
Shift Register							
t_{XLXL}	45	Serial port clock cycle time	$6t_{CLCL}$		300		ns
t_{QVXH}	45	Output data setup to clock rising edge	$5t_{CLCL}$–133		117		ns
t_{XHQX}	45	Output data hold after clock rising edge	t_{CLCL}–30		20		ns
t_{XHDX}	45	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	45	Clock rising edge to input data valid		$5t_{CLCL}$–133		117	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
3. Interfacing the microcontroller to devices with float times up to 45 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

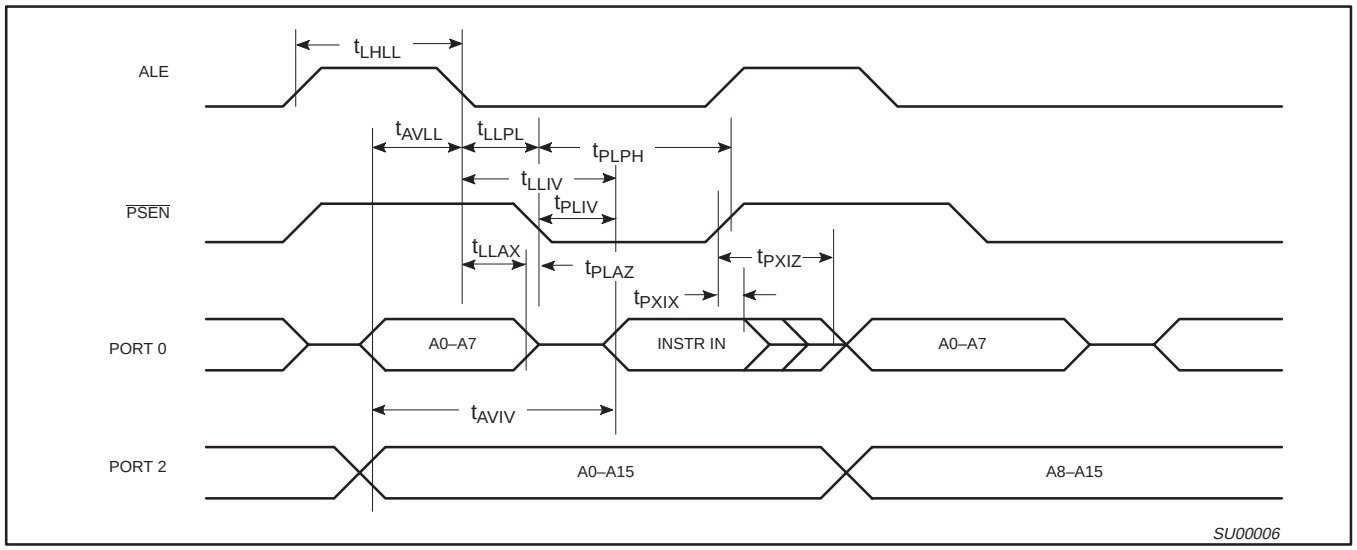


Figure 42. External Program Memory Read Cycle

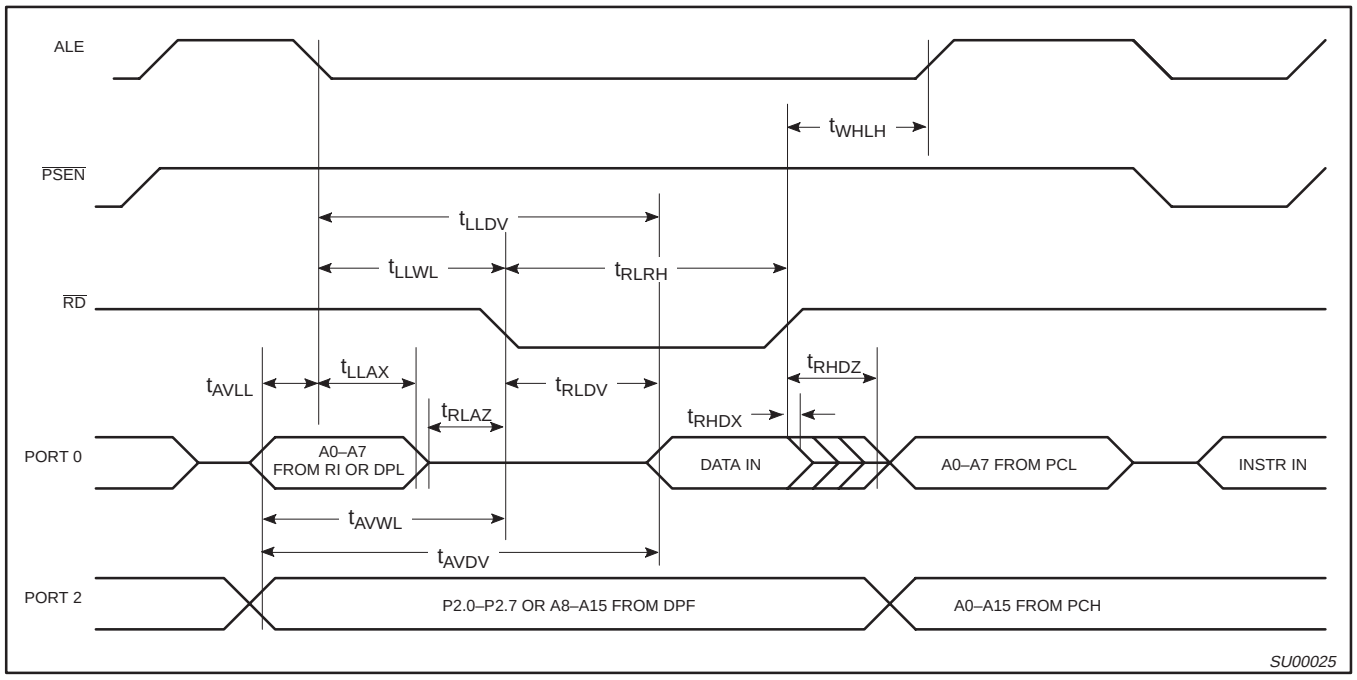


Figure 43. External Data Memory Read Cycle

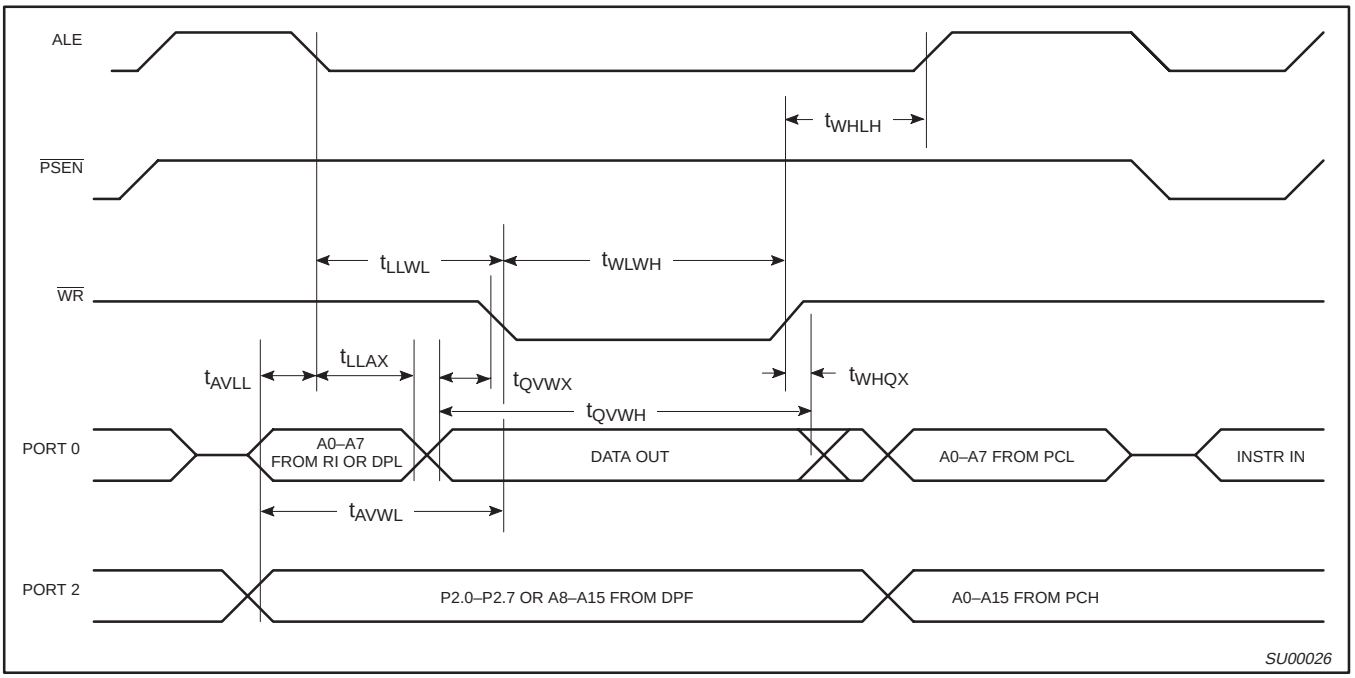


Figure 44. External Data Memory Write Cycle

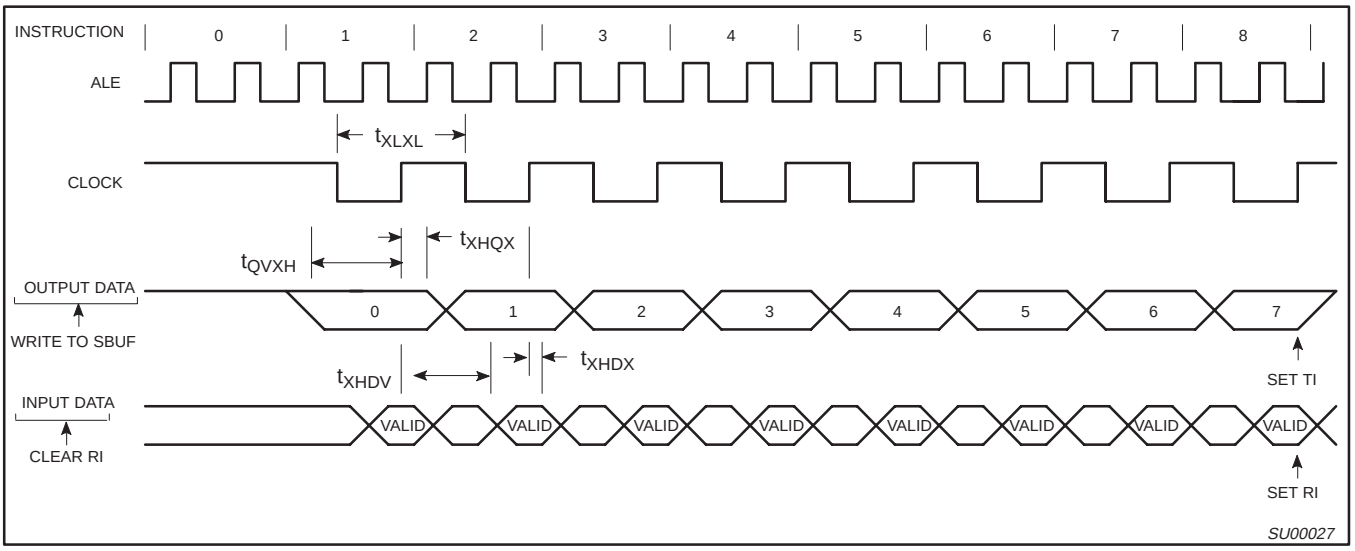


Figure 45. Shift Register Mode Timing

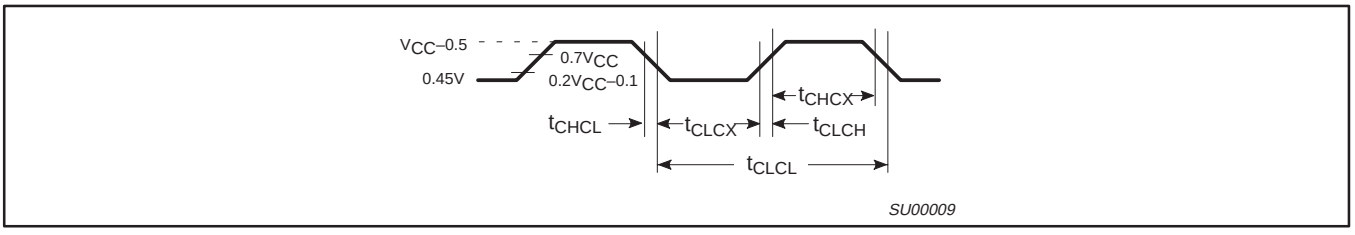


Figure 46. External Clock Drive

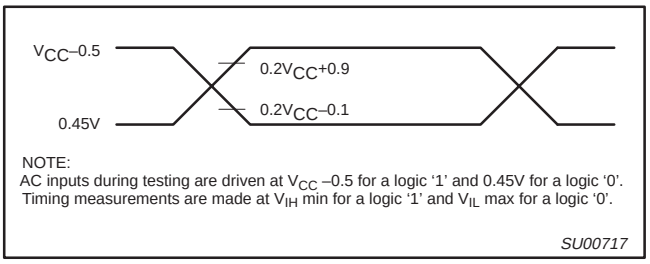


Figure 47. AC Testing Input/Output

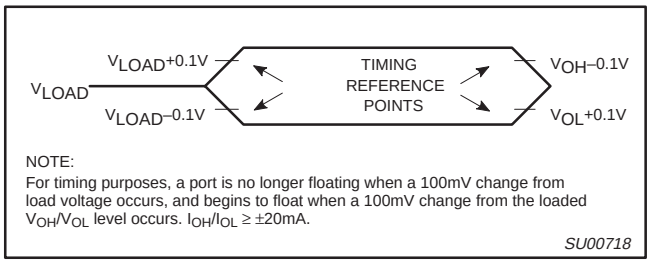


Figure 48. Float Waveform

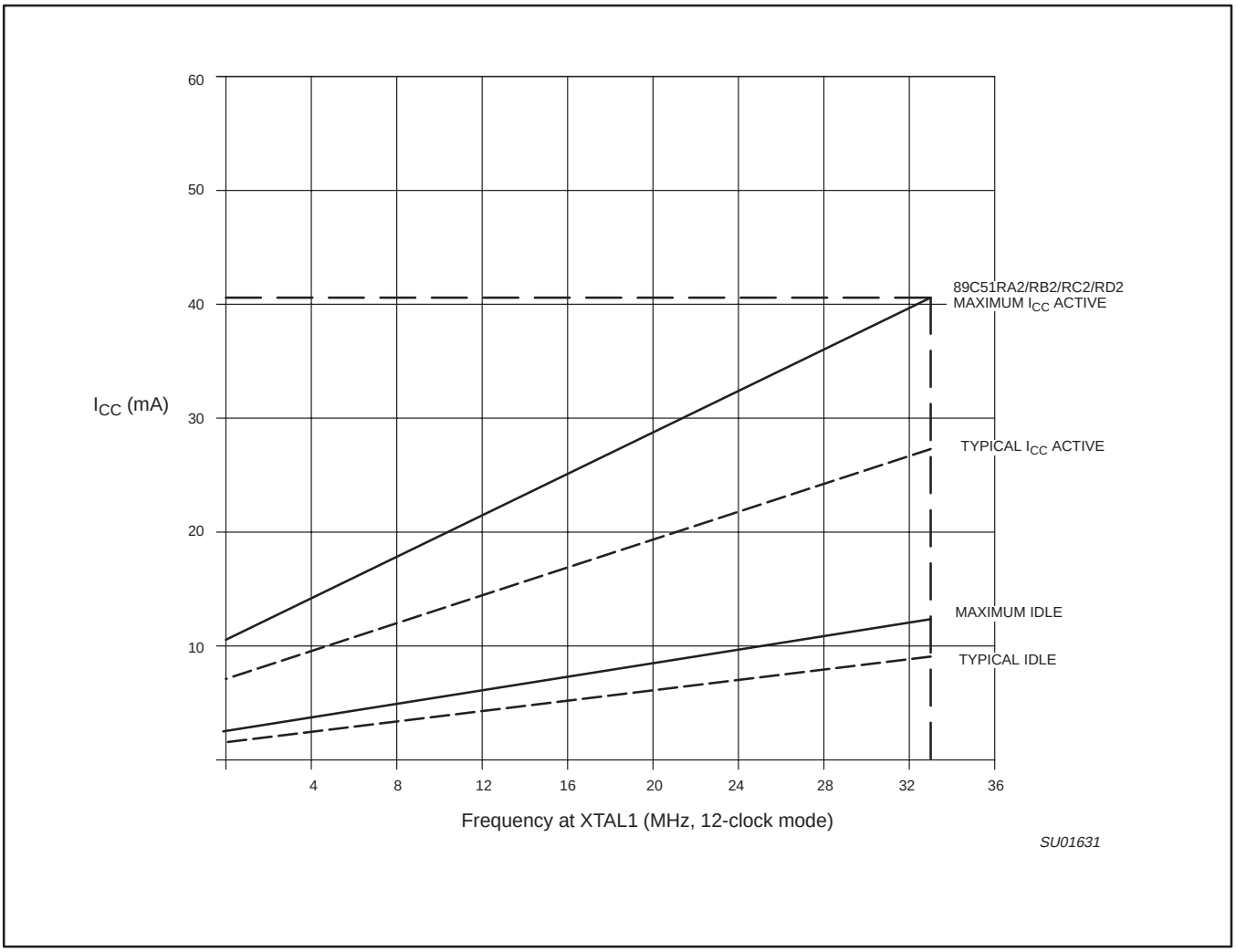


Figure 49. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

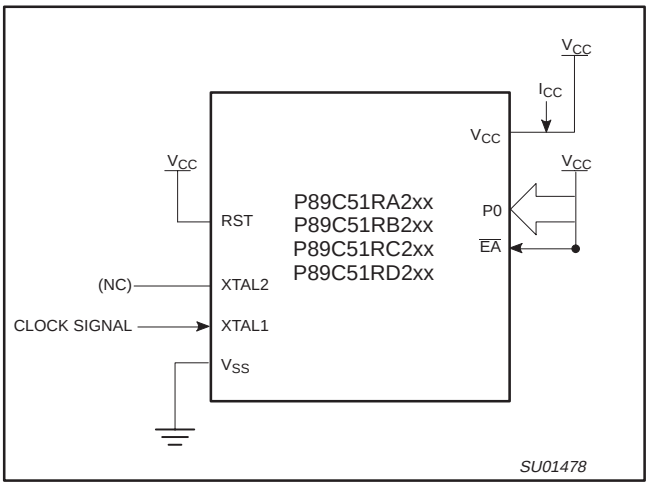


Figure 52. I_{CC} Test Condition, Active Mode, T_{amb} = 25 °C. All other pins are disconnected

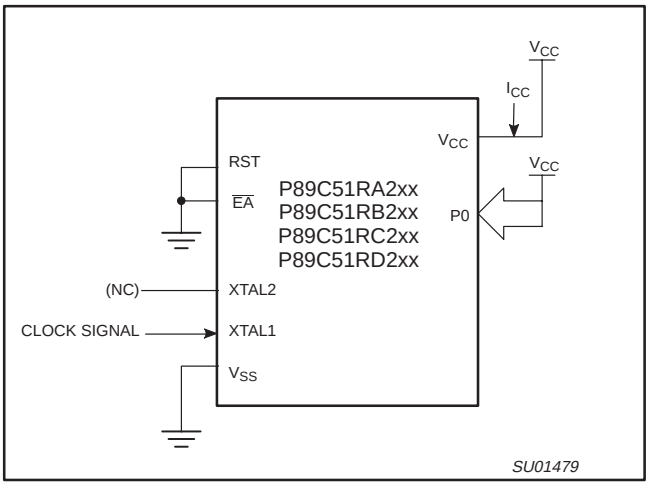


Figure 53. I_{CC} Test Condition, Idle Mode, T_{amb} = 25 °C. All other pins are disconnected

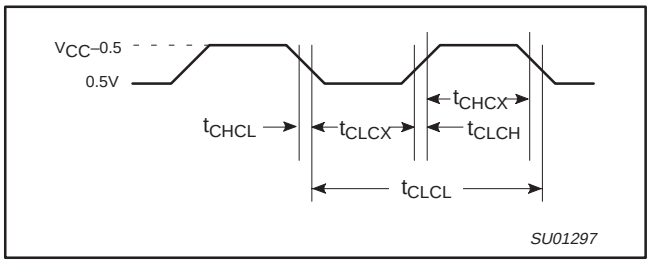


Figure 54. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. $t_{CLCL} = t_{CHCL}$ = 10 ns

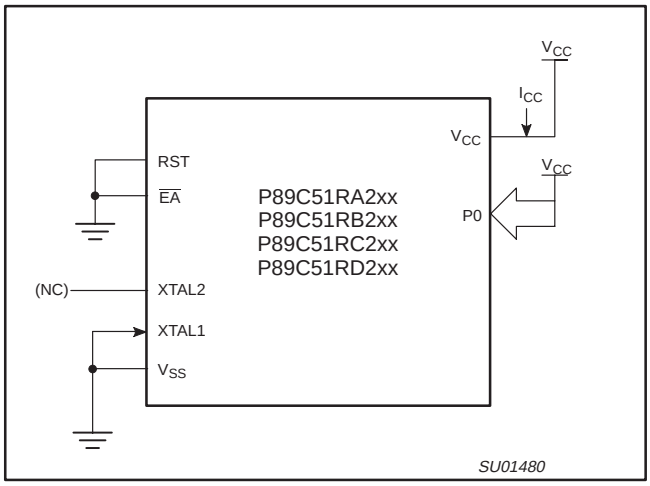


Figure 55. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected; V_{CC} = 2 V to 5.5 V

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

Date of release: 07-02

Document order number: 9397 750 10129

Let's make things better.

Philips Semiconductors

PHILIPS