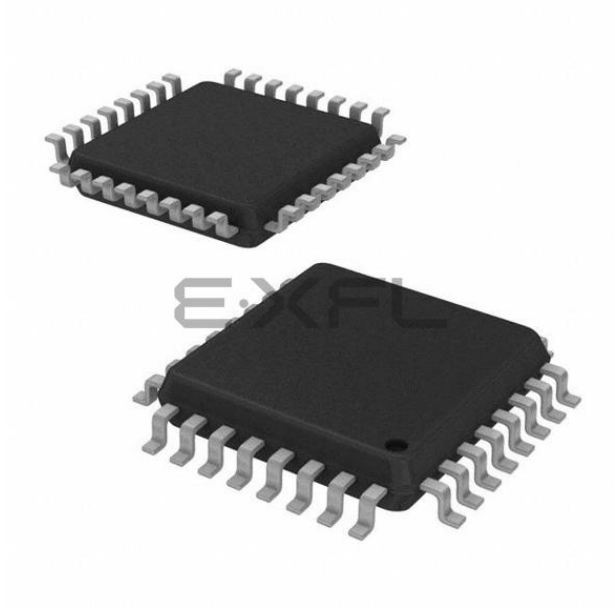

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 21x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f361-gq

List of Tables

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (bytes)	2-cycle 16 by 16 MAC	Calibrated Internal 24.5 MHz Oscillator	Internal 80 kHz Oscillator	External Memory Interface	SMBus/I^2C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200ksps ADC	10-bit Current Output DAC	Internal Voltage Reference	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051F360-C-GQ	100	32	1024	✓	✓	✓	✓	✓	✓	✓	4	✓	39	✓	✓	✓	✓	2	✓	TQFP-48
C8051F361-C-GQ[1]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	✓	✓	✓	✓	2	✓	LQFP-32
C8051F362-C-GM[2]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	✓	✓	✓	✓	2	✓	QFN-28
C8051F363-C-GQ	100	32	1024	✓	✓	✓	✓	✓	✓	✓	4	✓	39	—	—	—	—	2	✓	TQFP-48
C8051F364-C-GQ[1]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	—	—	—	—	2	✓	LQFP-32
C8051F365-C-GM[2]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	—	—	—	—	2	✓	QFN-28
C8051F366-C-GQ[1]	50	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	✓	✓	✓	✓	2	✓	LQFP-32
C8051F367-C-GM[2]	50	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	✓	✓	✓	✓	2	✓	QFN-28
C8051F368-C-GQ[1]	50	16	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	✓	✓	✓	✓	2	✓	LQFP-32
C8051F369-C-GM[2]	50	16	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	✓	✓	✓	✓	2	✓	QFN-28

Notes:
1. Pin compatible with the C8051F310-GQ.
2. Pin compatible with the C8051F311-GM.

3. Global Electrical Characteristics

Table 3.1. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage	SYSCLK = 0 to 50 MHz SYSCLK > 50 MHz	2.7 3.0	3.0 3.3	3.6 3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[1,2]	C8051F360/1/2/3/4/5 C8051F366/7/8/9	0 0	— —	100 50	MHz MHz
Specified Operating Temperature Range		–40	—	+85	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD}[2]	V_{DD} = 3.6 V, F = 100 MHz	—	68	75	mA
	V_{DD} = 3.6 V, F = 25 MHz	—	21	25	mA
	V_{DD} = 3.0 V, F = 100 MHz	—	54	60	mA
	V_{DD} = 3.0 V, F = 25 MHz	—	16	18	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.48	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	36	—	µA
I_{DD} Supply Sensitivity[3]	F = 25 MHz	—	56	—	%/V
	F = 1 MHz	—	57	—	%/V
I_{DD} Frequency Sensitivity[3,4]	V_{DD} = 3.0 V, F <= 20 MHz, T = 25 °C	—	0.45	—	mA/MHz
	V_{DD} = 3.0 V, F > 20 MHz, T = 25 °C	—	0.38	—	mA/MHz
	V_{DD} = 3.6 V, F <= 20 MHz, T = 25 °C	—	0.61	—	mA/MHz
	V_{DD} = 3.6 V, F > 20 MHz, T = 25 °C	—	0.51	—	mA/MHz

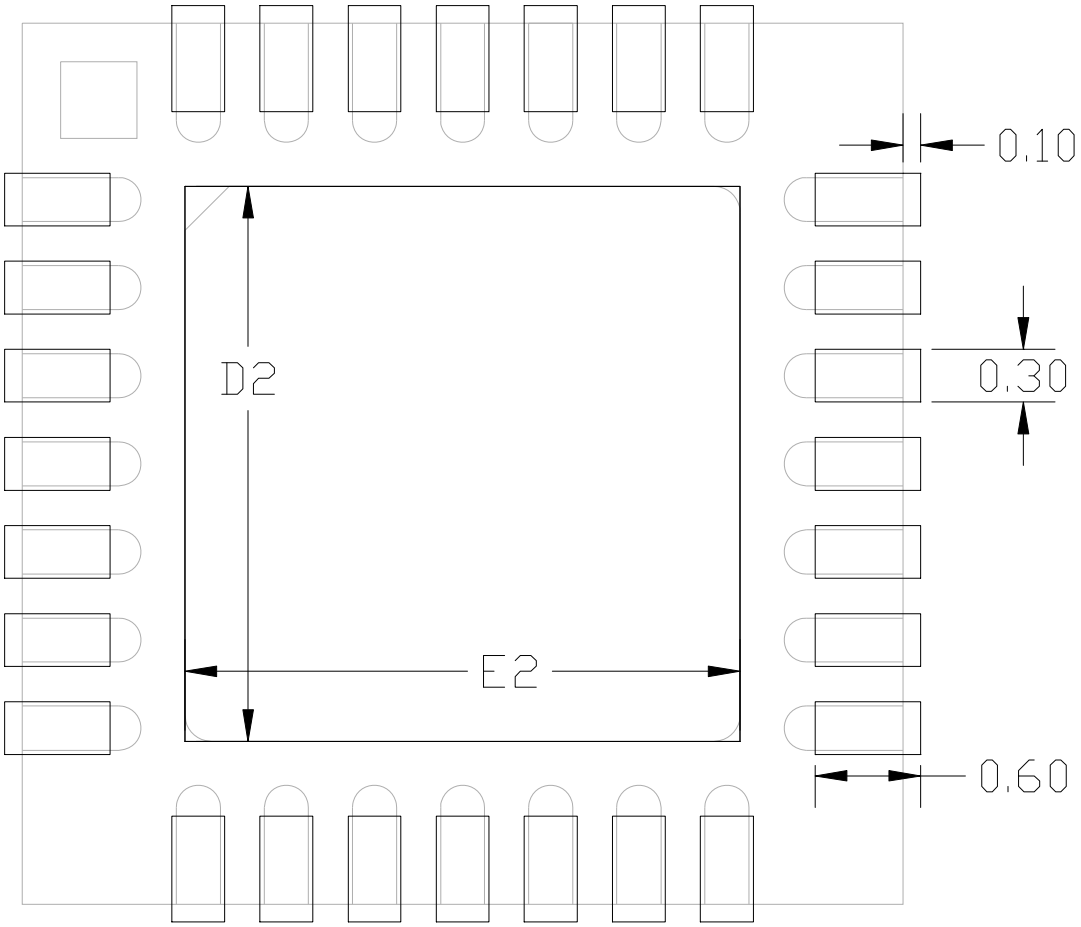


Figure 4.7. Typical QFN-28 Landing Diagram

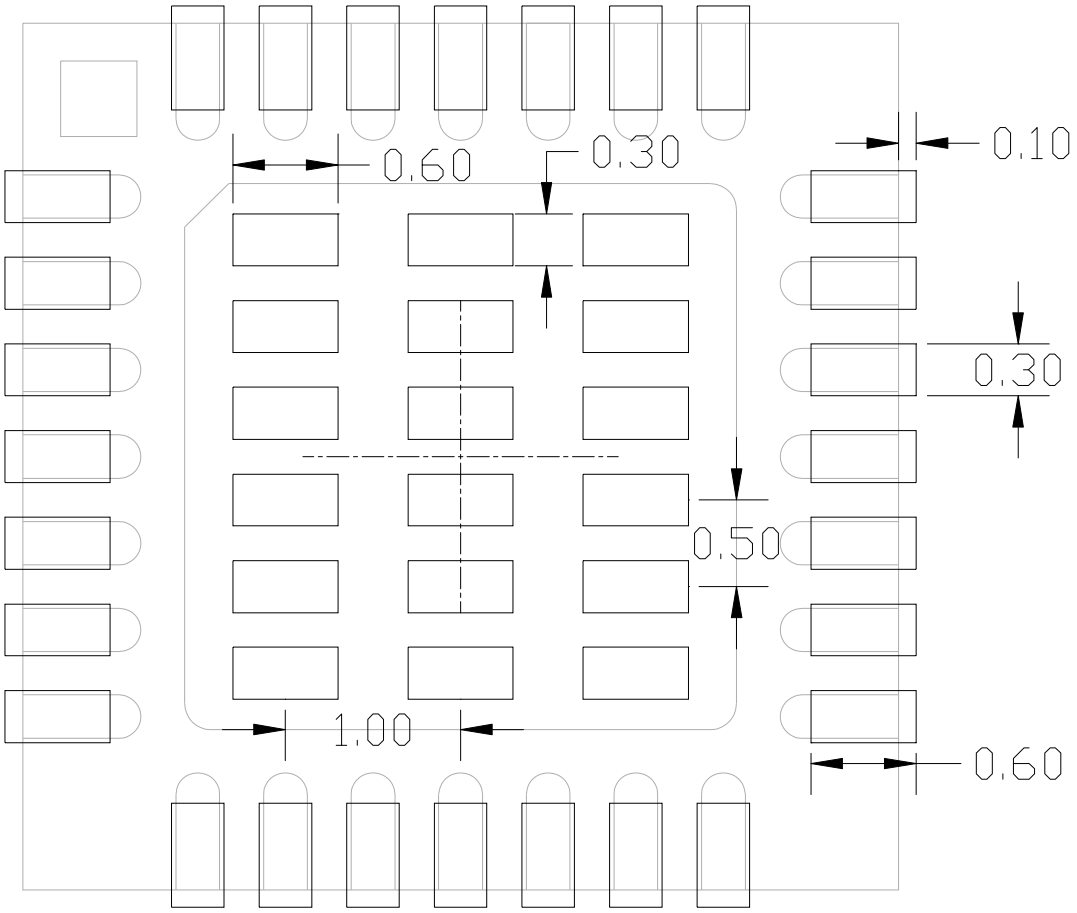


Figure 4.8. QFN-28 Solder Paste Recommendation

SFR Definition 5.1. AMX0P: AMUX0 Positive Channel Select

SFR Page: **all pages**
SFR Address: **0xBB**

R	R	R	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	–	AMX0P4	AMX0P3	AMX0P2	AMX0P1	AMX0P0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–5: UNUSED. Read = 000b; Write = don't care.
Bits 4–0: AMX0P4–0: AMUX0 Positive Input Selection

AMX0P4-0	ADC0 Positive Input
00000(1)	P1.0(1)
00001(1)	P1.1(1)
00010(1)	P1.2(1)
00011(1)	P1.3(1)
00100	P1.4
00101	P1.5
00110	P1.6
00111	P1.7
01000	P2.0
01001	P2.1
01010	P2.2
01011	P2.3
01100	P2.4
01101	P2.5
01110	P2.6
01111	P2.7
10000	P3.0
10001(2)	P3.1(2)
10010(2)	P3.2(2)
10011(2)	P3.3(2)
10100(2)	P3.4(2)
10101–11101	RESERVED
11110	Temp Sensor
11111	V_{DD}

Notes:
1. Only applies to C8051F361/2/6/7/8/9 (32-pin and 28-pin); selection RESERVED on C8051F360 (48-pin) device.
2. Only applies to C8051F360/1/6/8 (48-pin and 32-pin); selection RESERVED on C8051F362/7/9 (28-pin) devices.

5.4. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

SFR Definition 5.7. ADC0GTH: ADC0 Greater-Than Data High Byte

SFR Page: all pages
SFR Address: 0xC4

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: High byte of ADC0 Greater-Than Data Word.

SFR Definition 5.8. ADC0GTL: ADC0 Greater-Than Data Low Byte

SFR Page: all pages
SFR Address: 0xC3

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Low byte of ADC0 Greater-Than Data Word.

SFR Definition 5.9. ADC0LTH: ADC0 Less-Than Data High Byte

SFR Page: all pages
SFR Address: 0xC6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: High byte of ADC0 Less-Than Data Word.

SFR Definition 5.10. ADC0LTL: ADC0 Less-Than Data Low Byte

SFR Page: all pages
SFR Address: 0xC5

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Low byte of ADC0 Less-Than Data Word.

8. Comparators

C8051F36x devices include two on-chip programmable voltage comparators, Comparator0 and Comparator1, shown in Figure 8.1 and Figure 8.2 (**Note:** the port pin Comparator inputs differ between C8051F36x devices. The first Port I/O pin shown is for C8051F360/3 devices).

The comparators offer programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0 and CP1), or an asynchronous “raw” output (CP0A and CP1A). The asynchronous CP0A and CP1A signals are available even when the system clock is not active. This allows the Comparators to operate and generate an output with the device in STOP mode. When assigned to a Port pin, the Comparator outputs may be configured as open drain or push-pull (see Section “17.2. Port I/O Initialization” on page 186). Comparator0 may also be used as a reset source (see Section “12.5. Comparator0 Reset” on page 131).

The Comparator inputs are selected in the CPT0MX and CPT1MX registers (SFR Definition 8.2 and SFR Definition 8.5). The CMXnP1–CMXnP0 bits select the Comparator positive input; the CMXnN1–CMXnN0 bits select the Comparator negative input.

Important Note About Comparator Inputs: The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “17.3. General Purpose Port I/O” on page 189).

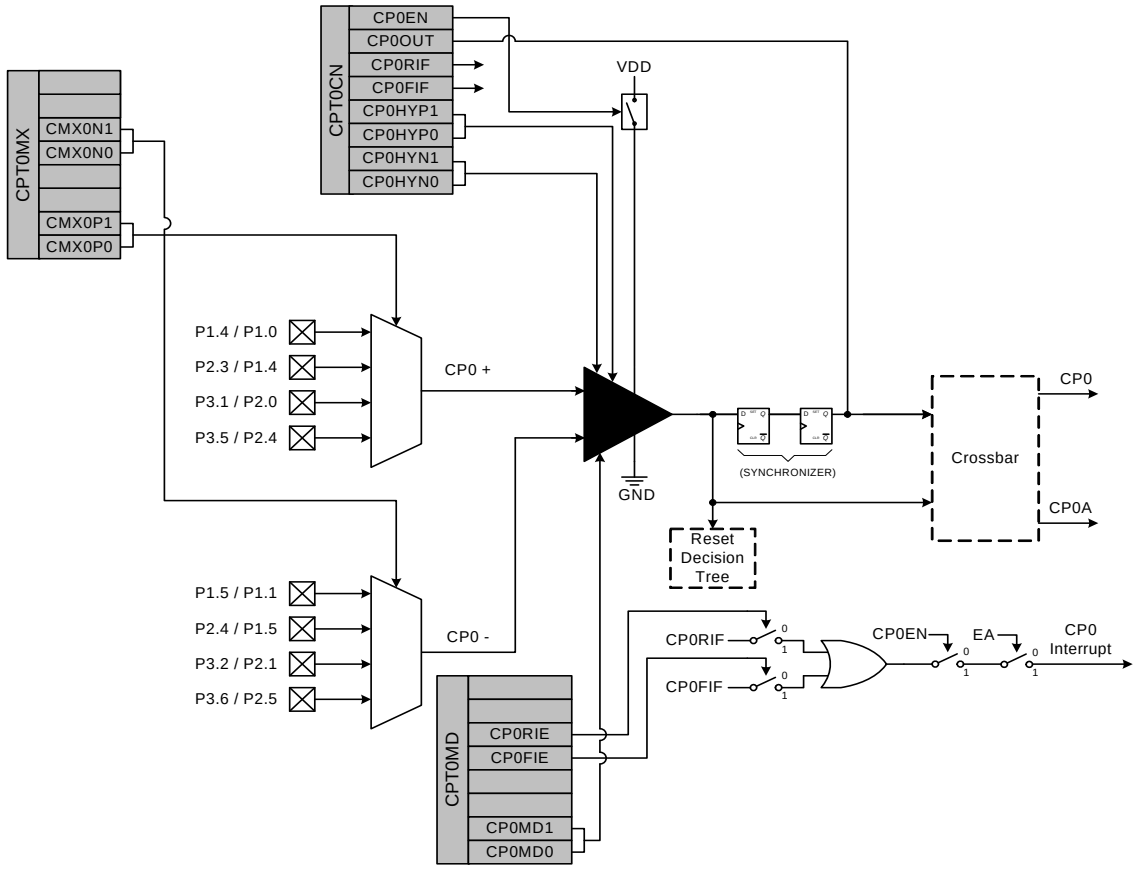


Figure 8.1. Comparator0 Functional Block Diagram

Table 9.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page No.
EMI0CF	0xC7	F	EMIF Configuration	page 155[2]
EMI0CN	0xAA	All Pages	EMIF Control	page 154[2]
EMI0TC	0xF7	F	EMIF Timing Control	page 160[2]
FLKEY	0xB7	0	Flash Lock and Key	page 142
FLSCL	0xB6	0	Flash Scale	page 143
FLSTAT	0xAC	F	Flash Status	page 152
IDA0CN	0xB9	All Pages	IDAC0 Control	page 65[1]
IDA0H	0x97	All Pages	IDAC0 High Byte	page 65[1]
IDA0L	0x96	All Pages	IDAC0 Low Byte	page 66[1]
IE	0xA8	All Pages	Interrupt Enable	page 110
IP	0xB8	All Pages	Interrupt Priority	page 111
IT01CF	0xE4	All Pages	INT0/INT1 Configuration	page 116
MAC0ACC0	0xD2	0	MAC0 Accumulator Byte 0 (LSB)	page 126
MAC0ACC1	0xD3	0	MAC0 Accumulator Byte 1	page 125
MAC0ACC2	0xD4	0	MAC0 Accumulator Byte 2	page 125
MAC0ACC3	0xD5	0	MAC0 Accumulator Byte 3 (MSB)	page 125
MAC0AH	0xA5	0	MAC0 A Register High Byte	page 123
MAC0AL	0xA4	0	MAC0 A Register Low Byte	page 124
MAC0BH	0xF2	0	MAC0 B Register High Byte	page 124
MAC0BL	0xF1	0	MAC0 B Register Low Byte	page 124
MAC0CF	0xD7	0	MAC0 Configuration	page 122
MAC0OVR	0xD6	0	MAC0 Accumulator Overflow	page 126
MAC0RNDH	0xAF	0	MAC0 Rounding Register High Byte	page 126
MAC0RNDL	0xAE	0	MAC0 Rounding Register Low Byte	page 127
MAC0STA	0xCF	0	MAC0 Status Register	page 123
OSCICL	0xBF	F	Internal Oscillator Calibration	page 169
OSCICN	0xB7	F	Internal Oscillator Control	page 170
OSCLCN	0xAD	F	Internal L-F Oscillator Control	page 171
OSCXCN	0xB6	F	External Oscillator Control	page 174
P0	0x80	All Pages	Port 0 Latch	page 189
P0MASK	0xF4	0	Port 0 Mask	page 191

Notes:
1. Refers to a register in the C8051F360/1/2/6/7/8/9 only.
2. Refers to a register in the C8051F360/3 only.

SFR Definition 9.11. PCON: Power Control

SFR Page: all pages
SFR Address: 0x87

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–3: RESERVED. Read = 000000b. Must Write 000000b.
Bit 1: STOP: STOP Mode Select.
Writing a ‘1’ to this bit will place the CIP-51 into STOP mode. This bit will always read ‘0’.
1: CIP-51 forced into power-down mode. (Turns off oscillator).
Bit 0: IDLE: IDLE Mode Select.
Writing a ‘1’ to this bit will place the CIP-51 into IDLE mode. This bit will always read ‘0’.
1: CIP-51 forced into IDLE mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, and all peripherals remain active.)

Table 10.1. Interrupt Summary (Continued)

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit addressable?	Cleared by HW?	Enable Flag	Priority Control
Programmable Counter Array	0x005B	11	CF (PCA0CN.7) CCFn (PCA0CN.n)	Y	N	EPCA0 (EIE1.4)	PPCA0 (EIP1.4)
Comparator0	0x0063	12	CP0FIF (CPT0CN.4) CP0RIF (CPT0CN.5)	N	N	ECP0 (EIE1.5)	PCP0 (EIP1.5)
Comparator1	0x006B	13	CP1FIF (CPT1CN.4) CP1RIF (CPT1CN.5)	N	N	ECP1 (EIE1.6)	PCP1 (EIP1.6)
Timer 3 Overflow	0x0073	14	TF3H (TMR3CN.7) TF3L (TMR3CN.6)	N	N	ET3 (EIE1.7)	PT3 (EIP1.7)
RESERVED	0x007B	15	N/A	N/A	N/A	N/A	N/A
Port Match	0x0083	16	N/A	N/A	N/A	EMAT (EIE2.1)	PMAT (EIP2.1)

10.4. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described below. Refer to the data sheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

11.2. Integer and Fractional Math

MAC0 is capable of interpreting the 16-bit inputs stored in MAC0A and MAC0B as signed integers or as signed fractional numbers. When the MAC0FM bit (MAC0CF.1) is cleared to '0', the inputs are treated as 16-bit, 2's complement, integer values. After the operation, the accumulator will contain a 40-bit, 2's complement, integer value. Figure 11.2 shows how integers are stored in the SFRs.

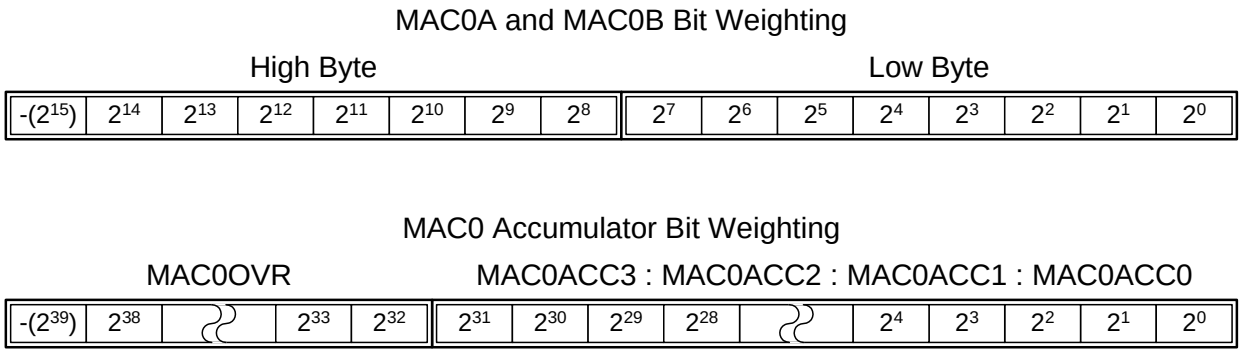
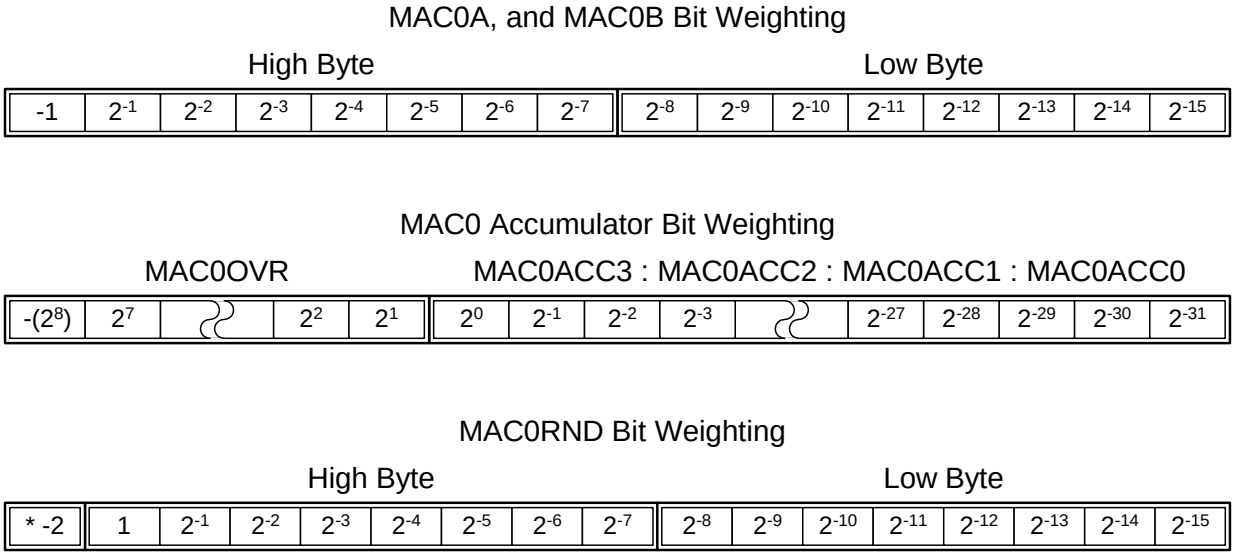


Figure 11.2. Integer Mode Data Representation

When the MAC0FM bit is set to '1', the inputs are treated at 16-bit, 2's complement, fractional values. The decimal point is located between bits 15 and 14 of the data word. After the operation, the accumulator will contain a 40-bit, 2's complement, fractional value, with the decimal point located between bits 31 and 30. Figure 11.3 shows how fractional numbers are stored in the SFRs.



* The MAC0RND register contains the 16 LSBs of a two's complement number. The MAC0N Flag can be used to determine the sign of the MAC0RND register.

Figure 11.3. Fractional Mode Data Representation

can be enabled or disabled by software as described in Section “22.3. Watchdog Timer Mode” on page 270; the WDT is enabled and clocked by SYSCLK / 12 following any reset. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit (RSTSRC.5) is set to ‘1’. The state of the RST pin is unaffected by this reset.

12.7. Flash Error Reset

If a Flash read/write/erase or program read targets an illegal address, a system reset is generated. This may occur due to any of the following:

- A Flash write or erase is attempted above user code space. This occurs when PSWE is set to ‘1’ and a MOVX write operation targets an address above address 0x7BFF.
- A Flash read is attempted above user code space. This occurs when a MOVC operation targets an address above address 0x7BFF.
- A Program read is attempted above user code space. This occurs when user code attempts to branch to an address above 0x7BFF.
- A Flash read, write or erase attempt is restricted due to a Flash security setting (see Section “13.2. Security Options” on page 137).
- A Flash write or erase is attempted while the V_{DD} Monitor is disabled.

The FERROR bit (RSTSRC.6) is set following a Flash error reset. The state of the RST pin is unaffected by this reset.

12.8. Software Reset

Software may force a reset by writing a ‘1’ to the SWRSF bit (RSTSRC.4). The SWRSF bit will read ‘1’ following a software forced reset. The state of the RST pin is unaffected by this reset.

15.6.1. Non-multiplexed Mode

15.6.1.1.16-bit MOVX: EMI0CF[4:2] = ‘101’, ‘110’, or ‘111’.

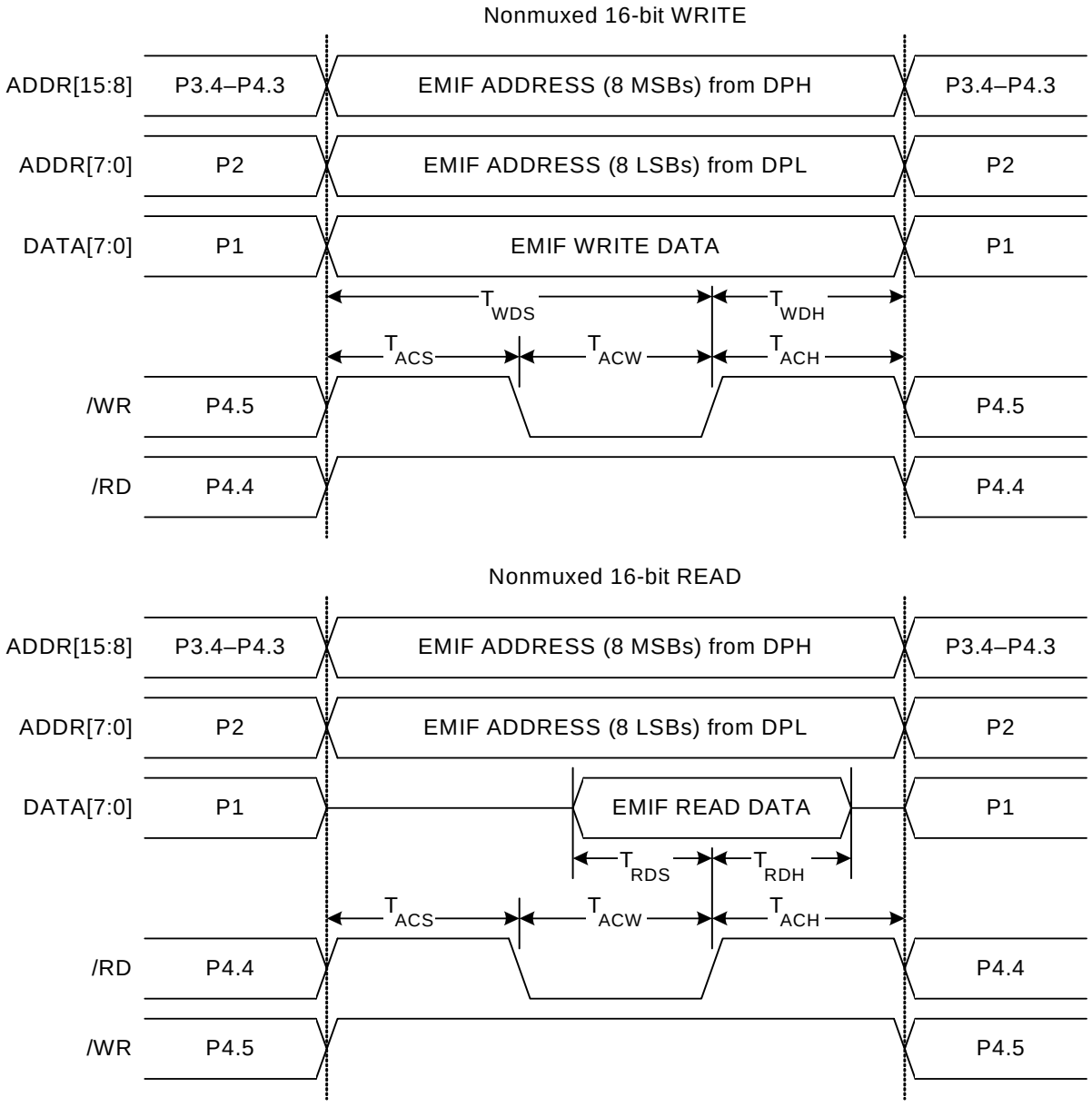


Figure 15.4. Non-multiplexed 16-bit MOVX Timing

16. Oscillators

The C8051F36x devices include a programmable internal high-frequency oscillator, a programmable internal low-frequency oscillator, and an external oscillator drive circuit. The internal high-frequency oscillator can be enabled, disabled, and calibrated using the OSCICN and OSCICL registers, as shown in Figure 16.1. The internal low-frequency oscillator can be enabled/disabled and calibrated using the OSCLCN register, as shown in SFR Definition 16.3. Both internal oscillators offer a selectable post-scaling feature. The system clock can be sourced by the external oscillator circuit, either internal oscillator, or the on-chip phase-locked loop (PLL). The internal oscillator's electrical specifications are given in Table 16.1 on page 170 and Table 16.2 on page 171.

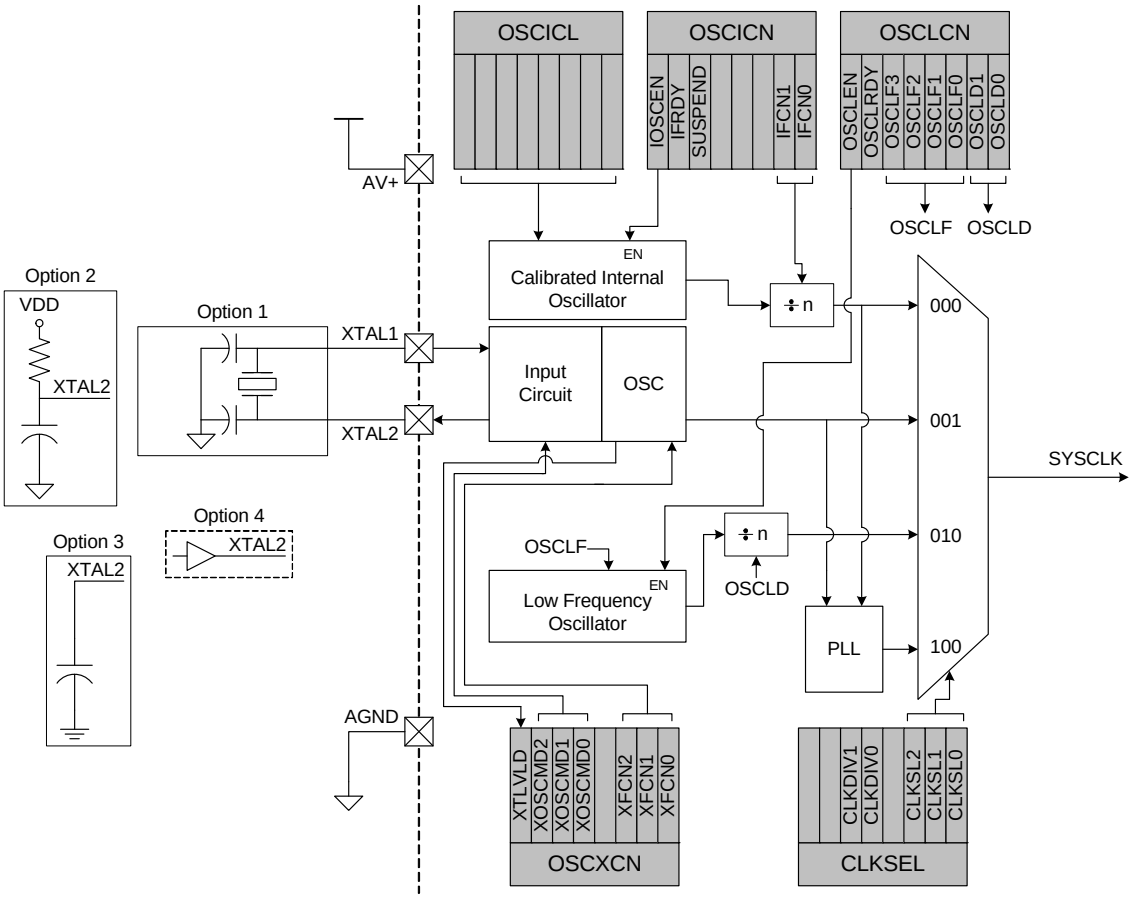


Figure 16.1. Oscillator Diagram

16.1. Programmable Internal High-Frequency (H-F) Oscillator

All devices include a calibrated internal high-frequency oscillator that defaults as the system clock after a system reset. The internal oscillator period can be adjusted via the OSCICL register as defined by SFR Definition 16.1. OSCICL is factory calibrated to obtain a 24.5 MHz frequency.

Electrical specifications for the precision internal oscillator are given in Table 16.1 on page 170 and Table 16.2 on page 171. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, or 8, as defined by the IFCN bits in register OSCICN. The divide value defaults to 8 following a reset.

20.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.

SFR Definition 20.1. SPI0CFG: SPI0 Configuration

SFR Page: all pages
SFR Address: 0xA1

R	R/W	R/W	R/W	R	R	R	R	Reset Value
SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT	00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: SPIBSY: SPI Busy (read only).
This bit is set to logic ‘1’ when a SPI transfer is in progress (Master or slave Mode).

Bit 6: MSTEN: Master Mode Enable.
0: Disable master mode. Operate in slave mode.
1: Enable master mode. Operate as a master.

Bit 5: CKPHA: SPI0 Clock Phase.
This bit controls the SPI0 clock phase.
0: Data centered on first edge of SCK period.*
1: Data centered on second edge of SCK period.*

Bit 4: CKPOL: SPI0 Clock Polarity.
This bit controls the SPI0 clock polarity.
0: SCK line low in idle state.
1: SCK line high in idle state.

Bit 3: SLVSEL: Slave Selected Flag (read only).
This bit is set to logic ‘1’ whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic ‘0’ when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.

Bit 2: NSSIN: NSS Instantaneous Pin Input (read only).
This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.

Bit 1: SRMT: Shift Register Empty (Valid in Slave Mode, read only).
This bit will be set to logic ‘1’ when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic ‘0’ when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK.
NOTE: SRMT = 1 when in Master Mode.

Bit 0: RXBMT: Receive Buffer Empty (Valid in Slave Mode, read only).
This bit will be set to logic ‘1’ when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic ‘0’.
NOTE: RXBMT = 1 when in Master Mode.

***Note:** In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 20.1 for timing parameters.

22.2.3. High Speed Output Mode

In High Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn) Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/ Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

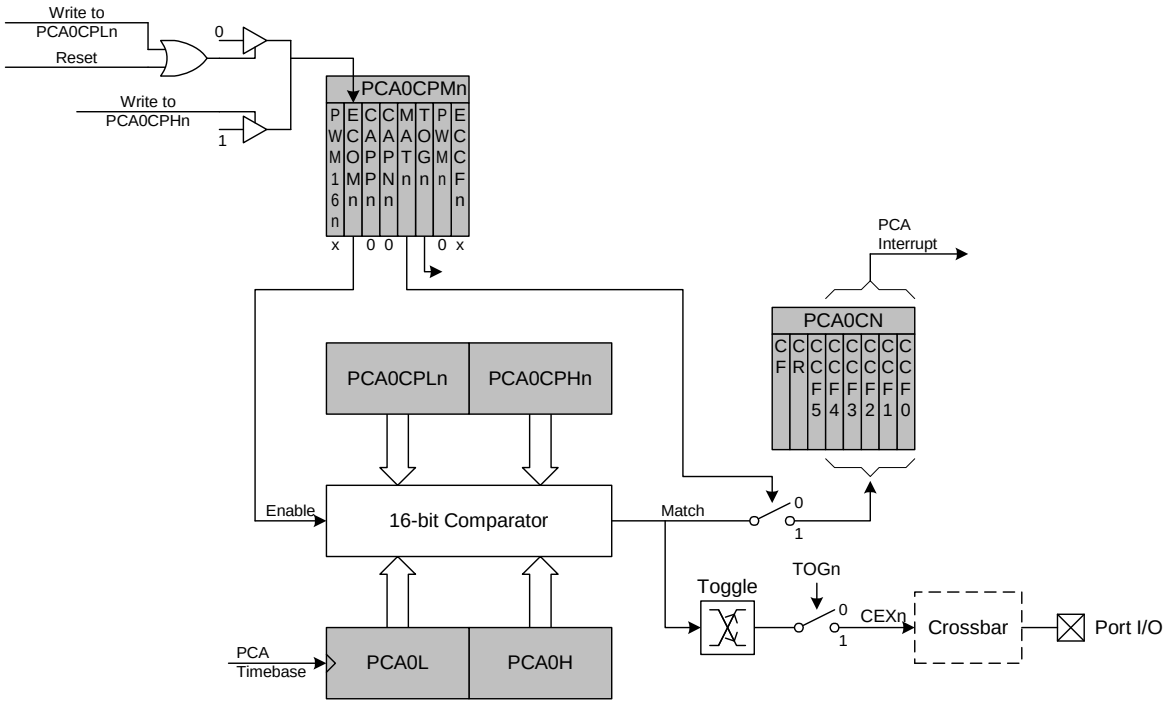


Figure 22.6. PCA High Speed Output Mode Diagram

Note: The initial state of the Toggle output is logic '1' and is initialized to this state when the module enters High Speed Output Mode.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated specification tables with most recently available characterization data.
- Fixed an error with the SYSCLK specification in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Corrected the name of the PMAT bit in SFR Definition 10.2. IP: Interrupt Priority.
- Corrected the reset value for SFR Definition 22.2. PCA0MD: PCA0 Mode.

Revision 0.2 to Revision 1.0

- Updated specification tables with characterization data.
- Fixed Table 1.1, “Product Selection Guide,” on page 19 to reflect the correct number of Port I/O pins for the C8051F361/2/4/5.
- Updated Section “10. Interrupt Handler” on page 107.
  - Added note describing EA change behavior when followed by single cycle instruction.
- Updated SFR Definition 11.1
  - Changed the MAC0SC (MAC0CF.5) bit description to correctly refer to the MAC0SD bit.
- Updated SFR Definition 15.2.
  - Changed the EMI0CF description to properly describe the 1k XRAM boundaries.
- Added Table 16.2, “Internal Low Frequency Oscillator Electrical Characteristics,” on page 171.
- Updated SFR Definition 16.9:
  - Specified that the undefined states for PLLLP3–0 are RESERVED.
- Added Table 19.7 and Table 19.8 on page 231 for UART Baud Rates when using the PLL.
- Updated Table 22.1, “PCA Timebase Input Options,” on page 263:
  - Specified that the undefined states of CPS2–0 are RESERVED.
- Added Revision B to “Revision Specific Behavior” on page 279.

Revision 1.0 to Revision 1.1

- Updated ordering table with Revision C part numbers.
- Updated Figure 17.2. ’Port I/O Cell Block Diagram’ on page 183 to refer to VDD instead of VIO.
- Added Revision C to “Revision Specific Behavior” on page 279.
- Added Revision C to the REVID C2 register in C2 Register Definition 24.3.
- Updated “Digital Supply Current (Stop Mode, shutdown)” typical value in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Updated “Missing Clock Detector Timeout” typical value in Table 12.1, “Reset Electrical Characteristics,” on page 134.