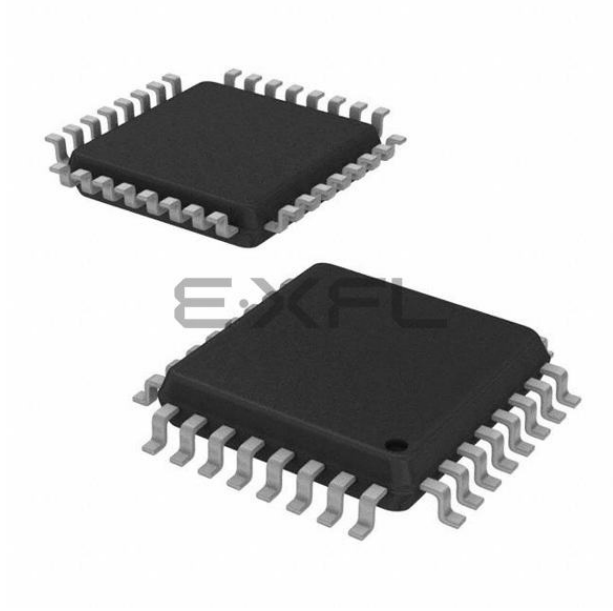

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Details	
Product Status	Discontinued at Digi-Key
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f364-gqr

Table 4.1. Pin Definitions for the C8051F36x (Continued)

Name	Pin 'F360/3 (48-pin)	Pin 'F361/4/6/8 (32-pin)	Pin 'F362/5/7/9 (28-pin)	Type	Description
P1.0	45	26	22	D I/O or A In	Port 1.0. See Section 17 for a complete description.
P1.1	44	25	21	D I/O or A In	Port 1.1. See Section 17 for a complete description.
P1.2	41	24	20	D I/O or A In	Port 1.2. See Section 17 for a complete description.
P1.3	40	23	19	D I/O or A In	Port 1.3. See Section 17 for a complete description.
P1.4	39	22	18	D I/O or A In	Port 1.4. See Section 17 for a complete description.
P1.5	38	21	17	D I/O or A In	Port 1.5. See Section 17 for a complete description.
P1.6	37	20	16	D I/O or A In	Port 1.6. See Section 17 for a complete description.
P1.7	36	19	15	D I/O or A In	Port 1.7. See Section 17 for a complete description.
P2.0	35	18	14	D I/O or A In	Port 2.0. See Section 17 for a complete description.
P2.1	34	17	13	D I/O or A In	Port 2.1. See Section 17 for a complete description.
P2.2	33	16	12	D I/O or A In	Port 2.2. See Section 17 for a complete description.
P2.3	32	15	11	D I/O or A In	Port 2.3. See Section 17 for a complete description.
P2.4	29	14	10	D I/O or A In	Port 2.4. See Section 17 for a complete description.
P2.5	28	13	9	D I/O or A In	Port 2.5. See Section 17 for a complete description.
P2.6	27	12	8	D I/O or A In	Port 2.6. See Section 17 for a complete description.
P2.7	26	11	7	D I/O or A In	Port 2.7. See Section 17 for a complete description.
P3.0	25	—	—	D I/O or A In	Port 3.0. See Section 17 for a complete description.

SFR Definition 6.3. IDA0L: IDA0 Data Word LSB

SFR Page: all pages
SFR Address: 0x96

R/W	R/W	R	R	R	R	R	R	Reset Value
		—	—	—	—	—	—	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–6: IDA0 Data Word Low-Order Bits.
Lower 2 bits of the 10-bit Data Word.
Bits 5–0: UNUSED. Read = 000000b, Write = don't care.

Table 6.1. IDAC Electrical Characteristics

–40 to +85 °C, V_{DD} = 3.0 V Full-scale output current set to 2 mA unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Static Performance					
Resolution			10		bits
Integral Nonlinearity		—	±0.5	±2	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	±0.5	±1	LSB
Output Compliance Range		—	—	V_{DD} – 1.2	V
Offset Error		—	0	—	LSB
Full Scale Error	2 mA Full Scale Output Current	–15	0	15	LSB
Full Scale Error Tempco		—	30	—	ppm/°C
V_{DD} Power Supply Rejection Ratio		—	6.5	—	µA/V
Dynamic Performance					
Output Settling Time to 1/2 LSB	IDA0H:L = 0x3FF to 0x000	—	5	—	µs
Startup Time		—	5	—	µs
Gain Variation	1 mA Full Scale Output Current 0.5 mA Full Scale Output Current	— —	±1 ±1	— —	% %
Power Consumption					
Power Supply Current (V_{DD} supplied to IDAC)	2 mA Full Scale Output Current 1 mA Full Scale Output Current 0.5 mA Full Scale Output Current	— — —	2140 1140 640	— — —	µA µA µA

8. Comparators

C8051F36x devices include two on-chip programmable voltage comparators, Comparator0 and Comparator1, shown in Figure 8.1 and Figure 8.2 (**Note:** the port pin Comparator inputs differ between C8051F36x devices. The first Port I/O pin shown is for C8051F360/3 devices).

The comparators offer programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0 and CP1), or an asynchronous “raw” output (CP0A and CP1A). The asynchronous CP0A and CP1A signals are available even when the system clock is not active. This allows the Comparators to operate and generate an output with the device in STOP mode. When assigned to a Port pin, the Comparator outputs may be configured as open drain or push-pull (see Section “17.2. Port I/O Initialization” on page 186). Comparator0 may also be used as a reset source (see Section “12.5. Comparator0 Reset” on page 131).

The Comparator inputs are selected in the CPT0MX and CPT1MX registers (SFR Definition 8.2 and SFR Definition 8.5). The CMXnP1–CMXnP0 bits select the Comparator positive input; the CMXnN1–CMXnN0 bits select the Comparator negative input.

Important Note About Comparator Inputs: The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “17.3. General Purpose Port I/O” on page 189).

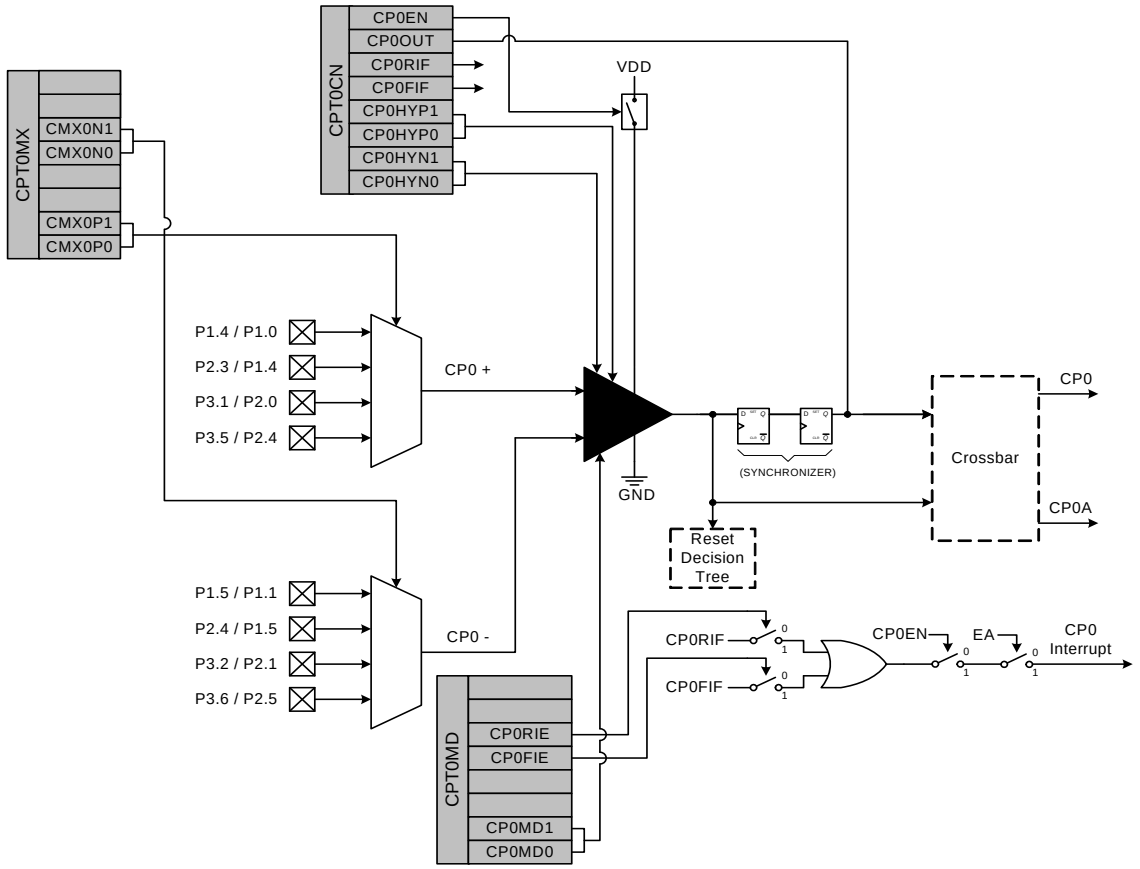

Figure 8.1. Comparator0 Functional Block Diagram

Table 9.2. Special Function Register (SFR) Memory Map

ADDRESS	SFR Page	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
F8	0 F	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
F0	0 F	B	MAC0BL P0MDIN	MAC0BH P1MDIN	P0MAT P2MDIN	P0MASK P3MDIN	PCA0CPL5	PCA0CPH5	- EMI0TC
E8	0 F	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
E0	0 F	ACC	P1MAT XBR0	P1MASK XBR1	- -	IT01CF	- SFR0CN	EIE1	EIE2
D8	0 F	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	PCA0CPM5
D0	0 F	PSW	REF0CN	MAC0ACC0 CCH0LC	MAC0ACC1 CCH0MA	MAC0ACC2 P0SKIP	MAC0ACC3 P1SKIP	MAC0OVR P2SKIP	MAC0CF P3SKIP
C8	0 F	TMR2CN	- CCH0TN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	- EIP1	MAC0STA EIP2
C0	0 F	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	- EMI0CF
B8	0 F	IP	IDA0CN	AMX0N	AMX0P	ADC0CF	ADC0L	ADC0H	- OSCICL
B0	0 F	P3	P2MAT PLL0MUL	P2MASK PLL0FLT	- PLL0CN	- -	P4	FLSCL OSCXCN	FLKEY OSCICN
A8	0 F	IE	- PLL0DIV	EMI0CN	- -	- FLSTAT	- OSCLCN	MAC0RNDL P4MDOUT	MAC0RNDH P3MDOUT
A0	0 F	P2	SPI0CFG	SPI0CKR	SPI0DAT	MAC0AL P0MDOUT	MAC0AH P1MDOUT	- P2MDOUT	SFRPAGE
98	0 F	SCON0	SBUF0	CPT1CN	CPT0CN	CPT1MD	CPT0MD	CPT1MX	CPT0MX
90	0 F	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	IDA0L	IDA0H
88	0 F	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL CLKSEL
80	0 F	P0	SP	DPL	DPH	- CCH0CN	SFRNEXT	SFRLAST	PCON
		0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

bit-addressable shaded SFRs are accessible on all SFR Pages regardless of the contents of SFRPAGE

SFR Definition 9.8. PSW: Program Status Word

SFR Page: **all pages**
SFR Address: **0xD0** (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	Reset Value
CY	AC	F0	RS1	RS0	OV	F1	PARITY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: CY: Carry Flag.
This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit 6: AC: Auxiliary Carry Flag
This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit 5: F0: User Flag 0.
This is a bit-addressable, general purpose flag for use under software control.

Bits 4–3: RS1–RS0: Register Bank Select.
These bits select which register bank is used during register accesses.

RS1	RS0	Register Bank	Address
0	0	0	0x00–0x07
0	1	1	0x08–0x0F
1	0	2	0x10–0x17
1	1	3	0x18–0x1F

Bit 2: OV: Overflow Flag.
This bit is set to 1 under the following circumstances:
- An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
- A MUL instruction results in an overflow (result is greater than 255).
- A DIV instruction causes a divide-by-zero condition.

The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit 1: F1: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit 0: PARITY: Parity Flag.
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

10.5. External Interrupts

The /INT0 and /INT1 external interrupt sources are configurable as active high or low, edge or level sensitive. The IN0PL (/INT0 Polarity) and IN1PL (/INT1 Polarity) bits in the IT01CF register select active high or active low; the IT0 and IT1 bits in TCON (Section “21.1. Timer 0 and Timer 1” on page 246) select level or edge sensitive. The table below lists the possible configurations.

IT0	IN0PL	/INT0 Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

IT1	IN1PL	/INT1 Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

/INT0 and /INT1 are assigned to Port pins as defined in the IT01CF register (see SFR Definition 10.7). Note that /INT0 and /INT0 Port pin assignments are independent of any Crossbar assignments. /INT0 and /INT1 will monitor their assigned Port pins without disturbing the peripheral that was assigned the Port pin via the Crossbar. To assign a Port pin only to /INT0 and/or /INT1, configure the Crossbar to skip the selected pin(s). This is accomplished by setting the associated bit in register XBR0 (see Section “17.1. Priority Crossbar Decoder” on page 184 for complete details on configuring the Crossbar).

IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flags for the /INT0 and /INT1 external interrupts, respectively. If an /INT0 or /INT1 external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag remains logic ‘1’ while the input is active as defined by the corresponding polarity bit (IN0PL or IN1PL); the flag remains logic ‘0’ while the input is inactive. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.

SFR Definition 15.2. EMI0CF: External Memory Configuration

SFR Page: F
SFR Address: 0xC7

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	–	EMD2	EMD1	EMD0	EALE1	EALE0	00000011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–5: UNUSED. Read = 000b. Write = don't care.
Bit 4: EMD2: EMIF Multiplex Mode Select.
0: EMIF operates in multiplexed address/data mode.
1: EMIF operates in non-multiplexed mode (separate address and data pins).
Bits 3–2: EMD1–0: EMIF Operating Mode Select.
These bits control the operating mode of the External Memory Interface.
00: Internal Only: MOVX accesses on-chip XRAM only. All effective addresses alias to on-chip memory space.
01: Split Mode without Bank Select: Accesses below the 1 k boundary are directed on-chip. Accesses above the 1 k boundary are directed off-chip. 8-bit off-chip MOVX operations use the current contents of the Address High port latches to resolve upper address byte. Note that in order to access off-chip space, EMI0CN must be set to a page that is not contained in the on-chip address space.
10: Split Mode with Bank Select: Accesses below the 1 k boundary are directed on-chip. Accesses above the 1 k boundary are directed off-chip. 8-bit off-chip MOVX operations use the contents of EMI0CN to determine the high-byte of the address.
11: External Only: MOVX accesses off-chip XRAM only. On-chip XRAM is not visible to the CPU.
Bits 1–0: EALE1–0: ALE Pulse-Width Select Bits (only has effect when EMD2 = 0).
00: ALE high and ALE low pulse width = 1 SYSCLK cycle.
01: ALE high and ALE low pulse width = 2 SYSCLK cycles.
10: ALE high and ALE low pulse width = 3 SYSCLK cycles.
11: ALE high and ALE low pulse width = 4 SYSCLK cycles.

15.4.2. Non-multiplexed Configuration

In Non-multiplexed mode, the Data Bus and the Address Bus pins are not shared. An example of a Non-multiplexed Configuration is shown in Figure 15.2. See Section “15.6.1. Non-multiplexed Mode” on page 161 for more information about Non-multiplexed operation.

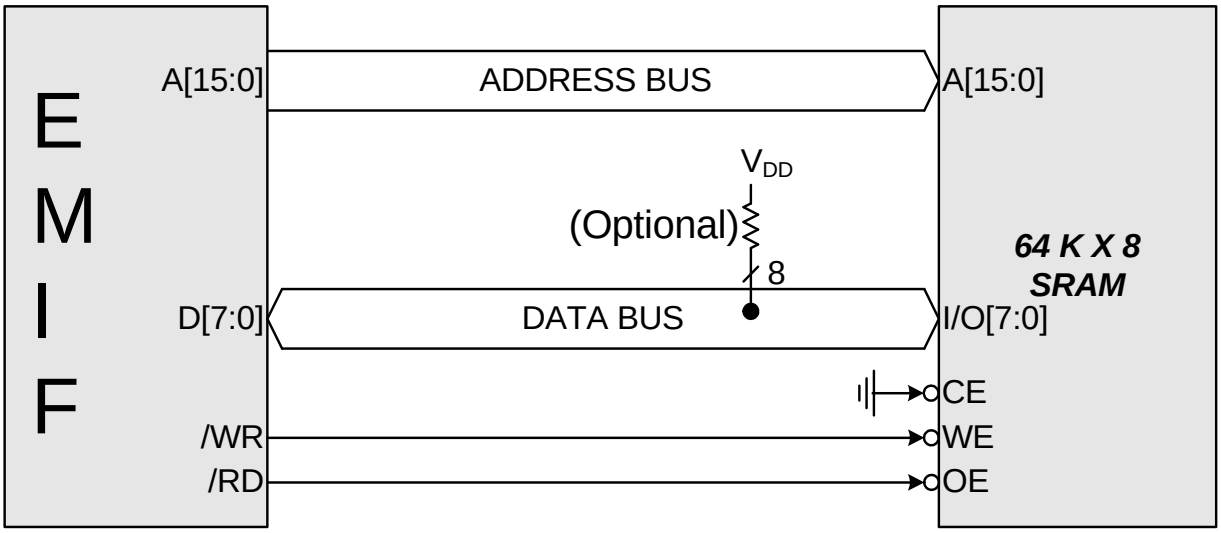

Figure 15.2. Non-multiplexed Configuration Example

15.5.3. Split Mode with Bank Select

When EMI0CF.[3:2] are set to ‘10’, the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the internal XRAM size boundary will access on-chip XRAM space.
- Effective addresses above the internal XRAM size boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. The upper 8-bits of the Address Bus A[15:8] are determined by EMI0CN, and the lower 8-bits of the Address Bus A[7:0] are determined by R0 or R1. All 16-bits of the Address Bus A[15:0] are driven in “Bank Select” mode.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

15.5.4. External Only

When EMI0CF[3:2] are set to ‘11’, all MOVX operations are directed to off-chip space. On-chip XRAM is not visible to the CPU. This mode is useful for accessing off-chip memory located between 0x0000 and the internal XRAM size boundary.

- 8-bit MOVX operations ignore the contents of EMI0CN. The upper Address bits A[15:8] are not driven (identical behavior to an off-chip access in “Split Mode without Bank Select” described above). This allows the user to manipulate the upper address bits at will by setting the Port state directly. The lower 8-bits of the effective address A[7:0] are determined by the contents of R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine the effective address A[15:0]. The full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

15.6. Timing

The timing parameters of the External Memory Interface can be configured to enable connection to devices having different setup and hold time requirements. The Address Setup time, Address Hold time, /RD and /WR strobe widths, and in multiplexed mode, the width of the ALE pulse are all programmable in units of SYSCLK periods through EMI0TC, shown in SFR Definition 15.3, and EMI0CF[1:0].

The timing for an off-chip MOVX instruction can be calculated by adding 4 SYSCLK cycles to the timing parameters defined by the EMI0TC register. Assuming non-multiplexed operation, the minimum execution time for an off-chip XRAM operation is 5 SYSCLK cycles (1 SYSCLK for /RD or /WR pulse + 4 SYSCLKs). For multiplexed operations, the Address Latch Enable signal will require a minimum of 2 additional SYSCLK cycles. Therefore, the minimum execution time for an off-chip XRAM operation in multiplexed mode is 7 SYSCLK cycles (2 for /ALE + 1 for /RD or /WR + 4). The programmable setup and hold times default to the maximum delay settings after a reset. Table 15.2 lists the AC parameters for the External Memory Interface, and Figure 15.4 through Figure 15.9 show the timing diagrams for the different External Memory Interface modes and MOVX operations.

15.6.2. Multiplexed Mode

15.6.2.1.16-bit MOVX: EMI0CF[4:2] = ‘001’, ‘010’, or ‘011’.

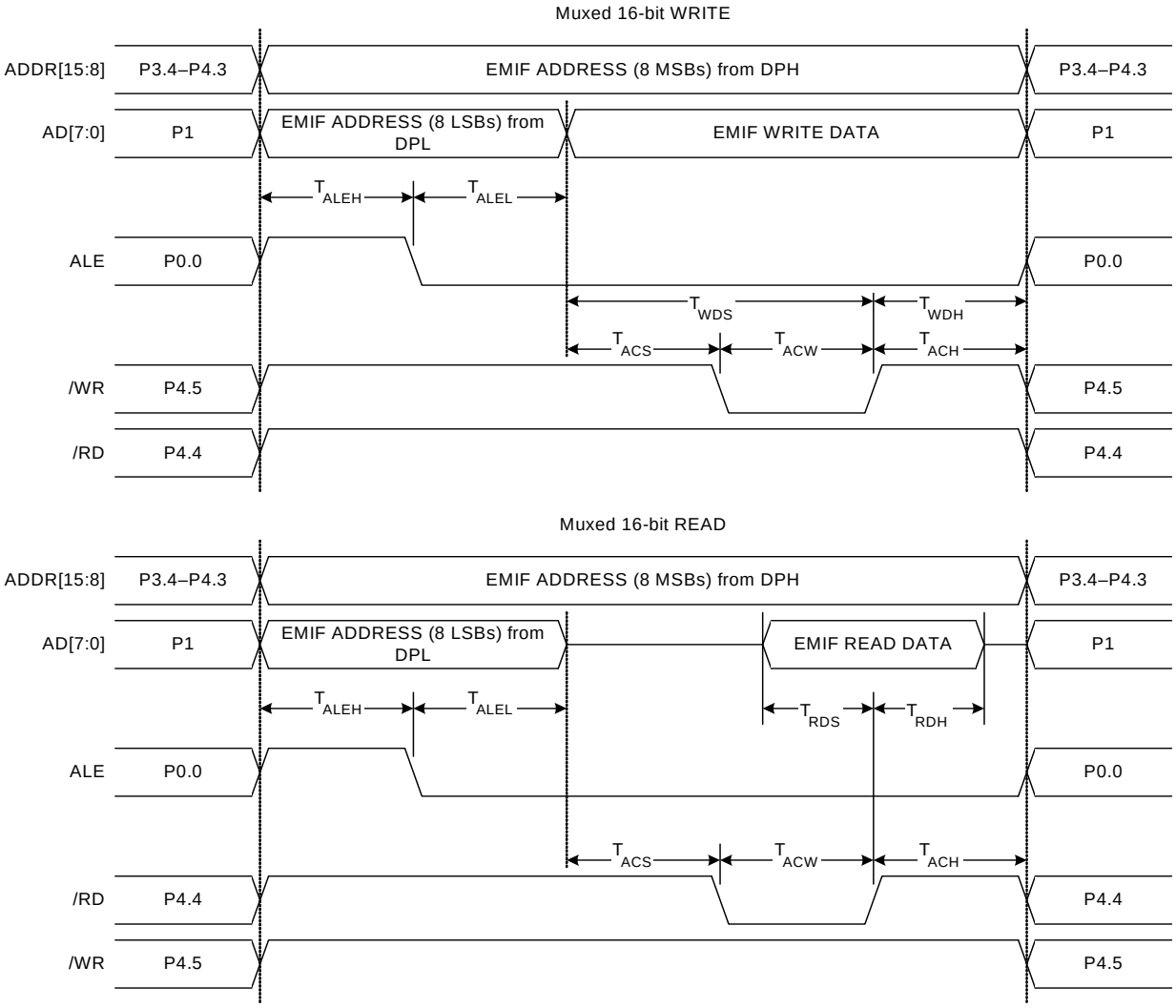

Figure 15.7. Multiplexed 16-bit MOVX Timing

SFR Definition 16.4. CLKSEL: System Clock Selection

SFR Page: F
SFR Address: 0x8F

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	CLKDIV1	CLKDIV0	Reserved	CLKSL2	CLKSL1	CLKSL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–6: RESERVED. Read = 00b. Must Write 00b.
Bits 5–4: CLKDIV1-0: Output SYSCLK Divide Factor.
These bits can be used to pre-divide SYSCLK before it is output to a port pin through the crossbar.
00: Output will be SYSCLK.
01: Output will be SYSCLK/2.
10: Output will be SYSCLK/4.
11: Output will be SYSCLK/8.
See Section “17. Port Input/Output” on page 182 for more details about routing this output to a port pin.
Bit 3: RESERVED. Read = 0b. Must Write 0b.
Bits 2–0: CLKSL2–0: System Clock Source Select Bits.
000: SYSCLK derived from the high-frequency Internal Oscillator, and scaled as per the IFCN bits in OSCICN.
001: SYSCLK derived from the External Oscillator circuit.
010: SYSCLK derived from the low-frequency Internal Oscillator, and scaled as per the OSCLD bits in OSCLCN.
011: RESERVED.
100: SYSCLK derived from the PLL.
101-11x: RESERVED.

SFR Definition 17.2. XBR1: Port I/O Crossbar Register 1

SFR Page: F
SFR Address: 0xE2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WEAKPUD	XBARE	T1E	T0E	ECIE	PCA0ME			00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: WEAKPUD: Port I/O Weak Pullup Disable.
0: Weak Pullups enabled (except for Ports whose I/O are configured as analog input).
1: Weak Pullups disabled.

Bit 6: XBARE: Crossbar Enable.
0: Crossbar disabled.
1: Crossbar enabled.

Bit 5: T1E: T1 Enable
0: T1 unavailable at Port pin.
1: T1 routed to Port pin.

Bit 4: T0E: T0 Enable
0: T0 unavailable at Port pin.
1: T0 routed to Port pin.

Bit 3: ECIE: PCA0 External Counter Input Enable
0: ECI unavailable at Port pin.
1: ECI routed to Port pin.

Bits 2–0: PCA0ME: PCA Module I/O Enable Bits.
000: All PCA I/O unavailable at Port pins.
001: CEX0 routed to Port pin.
010: CEX0, CEX1 routed to Port pins.
011: CEX0, CEX1, CEX2 routed to Port pins.
100: CEX0, CEX1, CEX2, CEX3 routed to Port pins.
101: CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins.
110: CEX0, CEX1, CEX2, CEX3, CEX4, CEX5 routed to Port pins.
111: Reserved.

18.6. SMBus Status Decoding

The current SMBus status can be easily decoded using the SMB0CN register. In the table below, STATUS VECTOR refers to the four upper bits of SMB0CN: MASTER, TXMODE, STA, and STO. The shown response options are only the typical responses; application-specific procedures are allowed as long as they conform to the SMBus specification. Highlighted responses are allowed but do not conform to the SMBus specification.

Table 18.4. SMBus Status Decoding

Mode	Values Read				Current SMbus State	Typical Response Options	Values Written		
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STo	ACK
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X
	1100	0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X
						Abort transfer.	0	1	X
		0	0	1	A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0DAT.	0	0	X
						End transfer with STOP.	0	1	X
						End transfer with STOP and start another transfer.	1	1	X
						Send repeated START.	1	0	X
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT).	0	0	X

20.1. Signal Descriptions

The four signals used by SPI0 (MOSI, MISO, SCK, NSS) are described below.

20.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI0 is operating as a master and an input when SPI0 is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

20.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI0 is operating as a master and an output when SPI0 is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

20.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. SPI0 generates this signal when operating as a master. The SCK signal is ignored by a SPI slave when the slave is not selected (NSS = 1) in 4-wire slave mode.

20.1.4. Slave Select (NSS)

The function of the slave-select (NSS) signal is dependent on the setting of the NSSMD1 and NSSMD0 bits in the SPI0CN register. There are three possible modes that can be selected with these bits:

1. NSSMD[1:0] = 00: 3-Wire Master or 3-Wire Slave Mode: SPI0 operates in 3-wire mode, and NSS is disabled. When operating as a slave device, SPI0 is always selected in 3-wire mode. Since no select signal is present, SPI0 must be the only slave on the bus in 3-wire mode. This is intended for point-to-point communication between a master and one slave.
2. NSSMD[1:0] = 01: 4-Wire Slave or Multi-Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an input. When operating as a slave, NSS selects the SPI0 device. When operating as a master, a 1-to-0 transition of the NSS signal disables the master function of SPI0 so that multiple master devices can be used on the same SPI bus.
3. NSSMD[1:0] = 1x: 4-Wire Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an output. The setting of NSSMD0 determines what logic level the NSS pin will output. This configuration should only be used when operating SPI0 as a master device.

See Figure 20.2, Figure 20.3, and Figure 20.4 for typical connection diagrams of the various operational modes. **Note that the setting of NSSMD bits affects the pinout of the device.** When in 3-wire master or 3-wire slave mode, the NSS pin will not be mapped by the crossbar. In all other modes, the NSS signal will be mapped to a pin on the device. See Section “17. Port Input/Output” on page 182 for general purpose port I/O and crossbar information.

SFR Definition 20.3. SPI0CKR: SPI0 Clock Rate

SFR Page: all pages
SFR Address: 0xA2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: SCR7–SCR0: SPI0 Clock Rate.
These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register.

$$f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR + 1)}$$

for 0 <= SPI0CKR <= 255

Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04,

$$f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$$

$$f_{SCK} = 200kHz$$

SFR Definition 20.4. SPI0DAT: SPI0 Data

SFR Page: all pages
SFR Address: 0xA3

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: SPI0DAT: SPI0 Transmit and Receive Data.
The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.

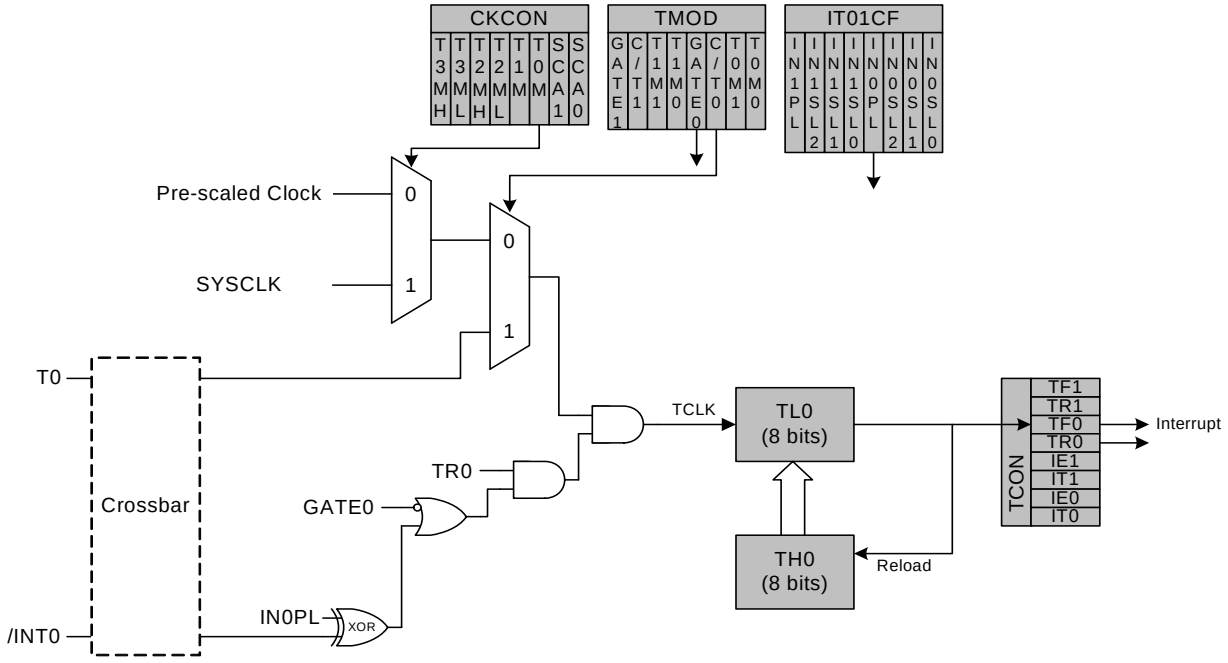

Figure 21.2. T0 Mode 2 Block Diagram

22. Programmable Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. PCA0 consists of a dedicated 16-bit counter/timer and six 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled (See Section “17.3. General Purpose Port I/O” on page 189). The counter/timer is driven by a programmable timebase that can select between six inputs as its source: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0 overflow, or an external clock signal on the ECI line. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8-Bit PWM, or 16-Bit PWM (each is described in Section 22.2). The PCA is configured and controlled through the system controller's Special Function Registers. The basic PCA block diagram is shown in Figure 22.1.

Important Note: The PCA Module 5 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled**. See Section 22.3 for details.

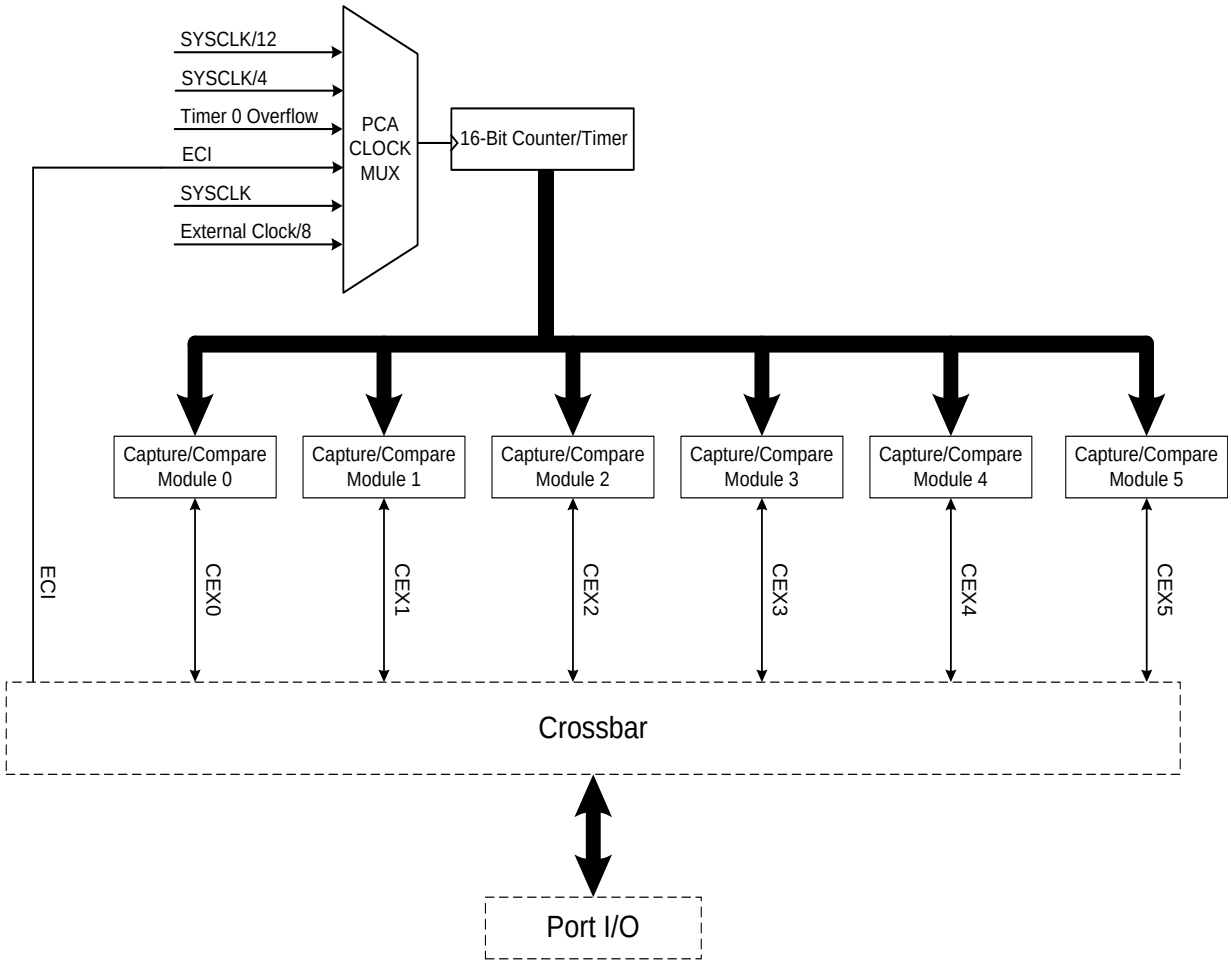

Figure 22.1. PCA Block Diagram

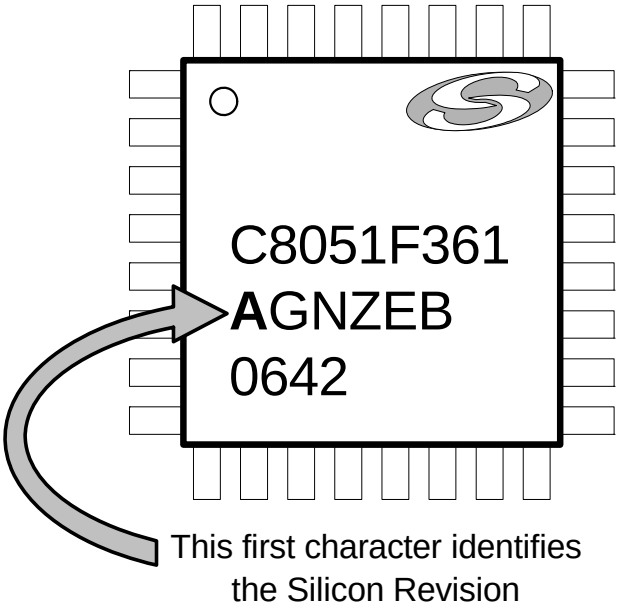

Figure 23.2. Device Package - LQFP 32

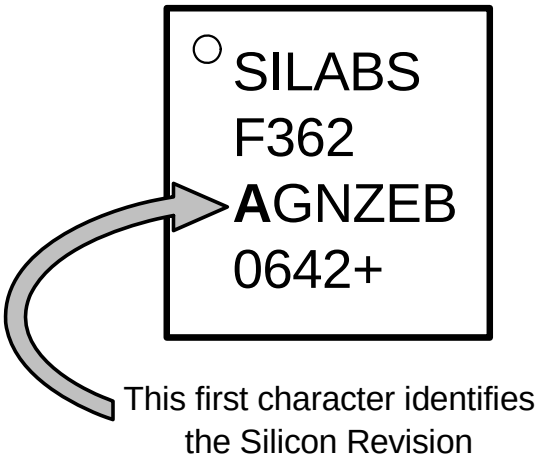

Figure 23.3. Device Package - QFN 28

23.2. CPL C Instruction Behavior

Problem

On Revision A and Revision B devices, a bug in the CPU causes an execution failure for the “CPL C” (Complement Carry bit) instruction under a narrow set of conditions involving an instruction order dependency. The probability of failure is increased at higher temperatures, lower power supply voltage, and higher system clock frequencies.

The failure mode is as follows: if the Carry bit contains a 1 prior to the execution phase of the “CPL C” opcode, the Carry bit will remain a 1 after the execution phase of the opcode has completed. If the Carry

24.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming functions may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely ‘borrow’ the C2CK (/RST) and C2D (P4.6 on C8051F360/3 devices, P3.0 on C8051F361/2/4/5/6/7/8/9 devices) pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 24.1.

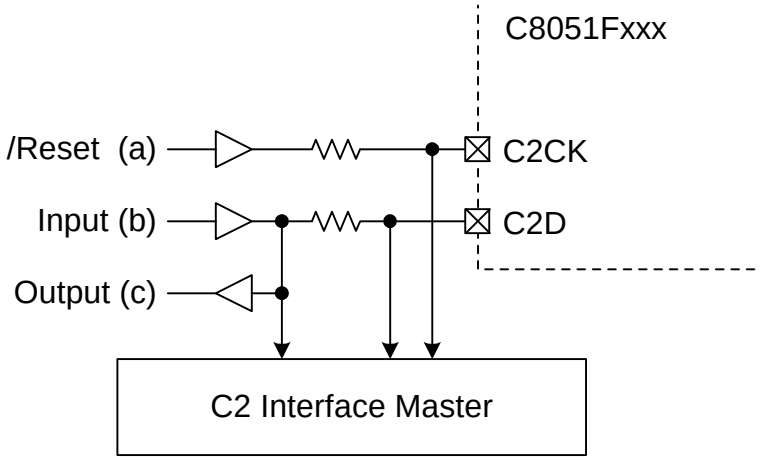

Figure 24.1. Typical C2 Pin Sharing

The configuration in Figure 24.1 assumes the following:

1. The user input (b) cannot change state while the target device is halted.
2. The /RST pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.