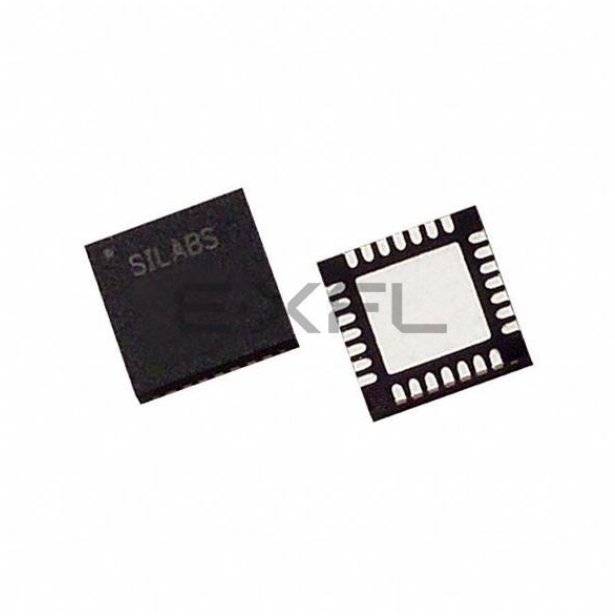

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f365-gm

The Digital Crossbar allows mapping of internal digital system resources to Port I/O pins. (See Figure 1.8.) On-chip counter/timers, serial buses, HW interrupts, comparator output, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

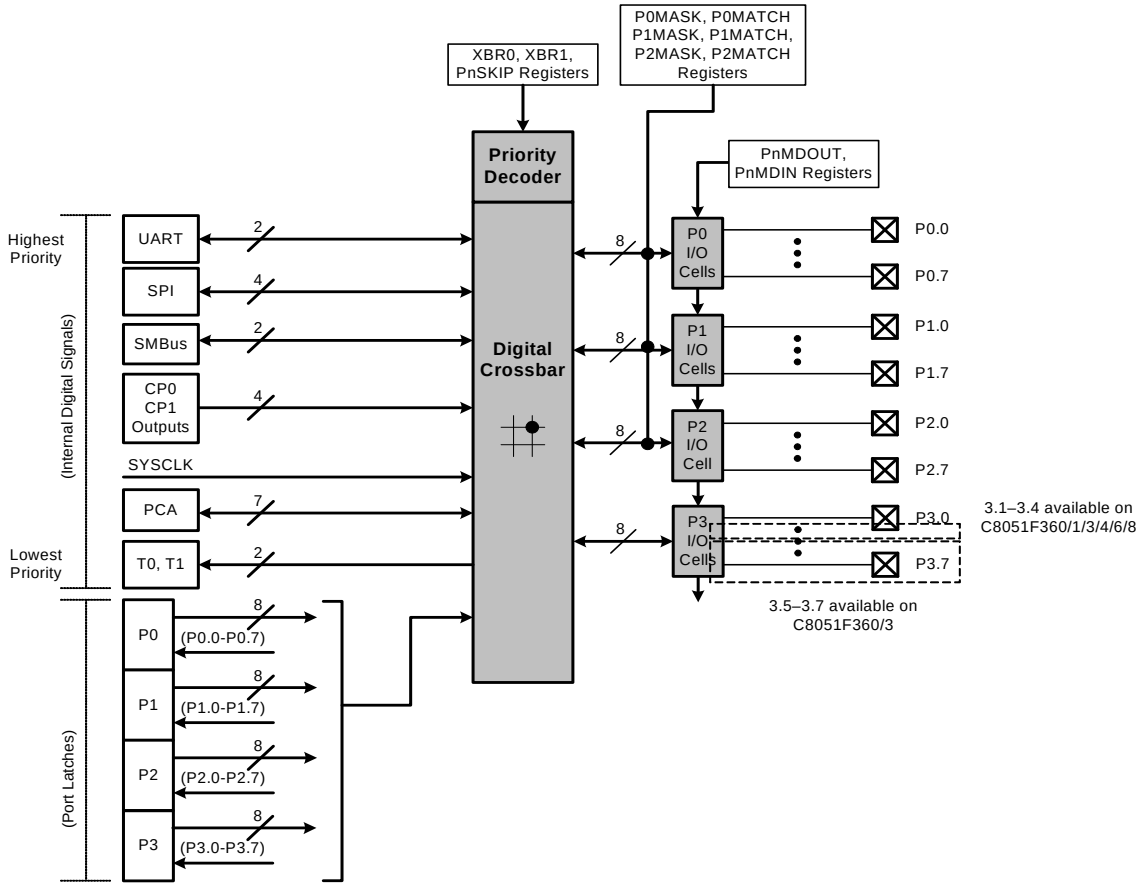

Figure 1.8. Digital Crossbar Diagram (Port 0 to Port 3)

1.5. Serial Ports

The C8051F36x Family includes an SMBus/I^2C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.6. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with three programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8. The external clock source selection is useful for

3. Global Electrical Characteristics

Table 3.1. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage	SYSCLK = 0 to 50 MHz SYSCLK > 50 MHz	2.7 3.0	3.0 3.3	3.6 3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[1,2]	C8051F360/1/2/3/4/5 C8051F366/7/8/9	0 0	— —	100 50	MHz MHz
Specified Operating Temperature Range		–40	—	+85	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD}[2]	V_{DD} = 3.6 V, F = 100 MHz	—	68	75	mA
	V_{DD} = 3.6 V, F = 25 MHz	—	21	25	mA
	V_{DD} = 3.0 V, F = 100 MHz	—	54	60	mA
	V_{DD} = 3.0 V, F = 25 MHz	—	16	18	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.48	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	36	—	µA
I_{DD} Supply Sensitivity[3]	F = 25 MHz	—	56	—	%/V
	F = 1 MHz	—	57	—	%/V
I_{DD} Frequency Sensitivity[3,4]	V_{DD} = 3.0 V, F <= 20 MHz, T = 25 °C	—	0.45	—	mA/MHz
	V_{DD} = 3.0 V, F > 20 MHz, T = 25 °C	—	0.38	—	mA/MHz
	V_{DD} = 3.6 V, F <= 20 MHz, T = 25 °C	—	0.61	—	mA/MHz
	V_{DD} = 3.6 V, F > 20 MHz, T = 25 °C	—	0.51	—	mA/MHz

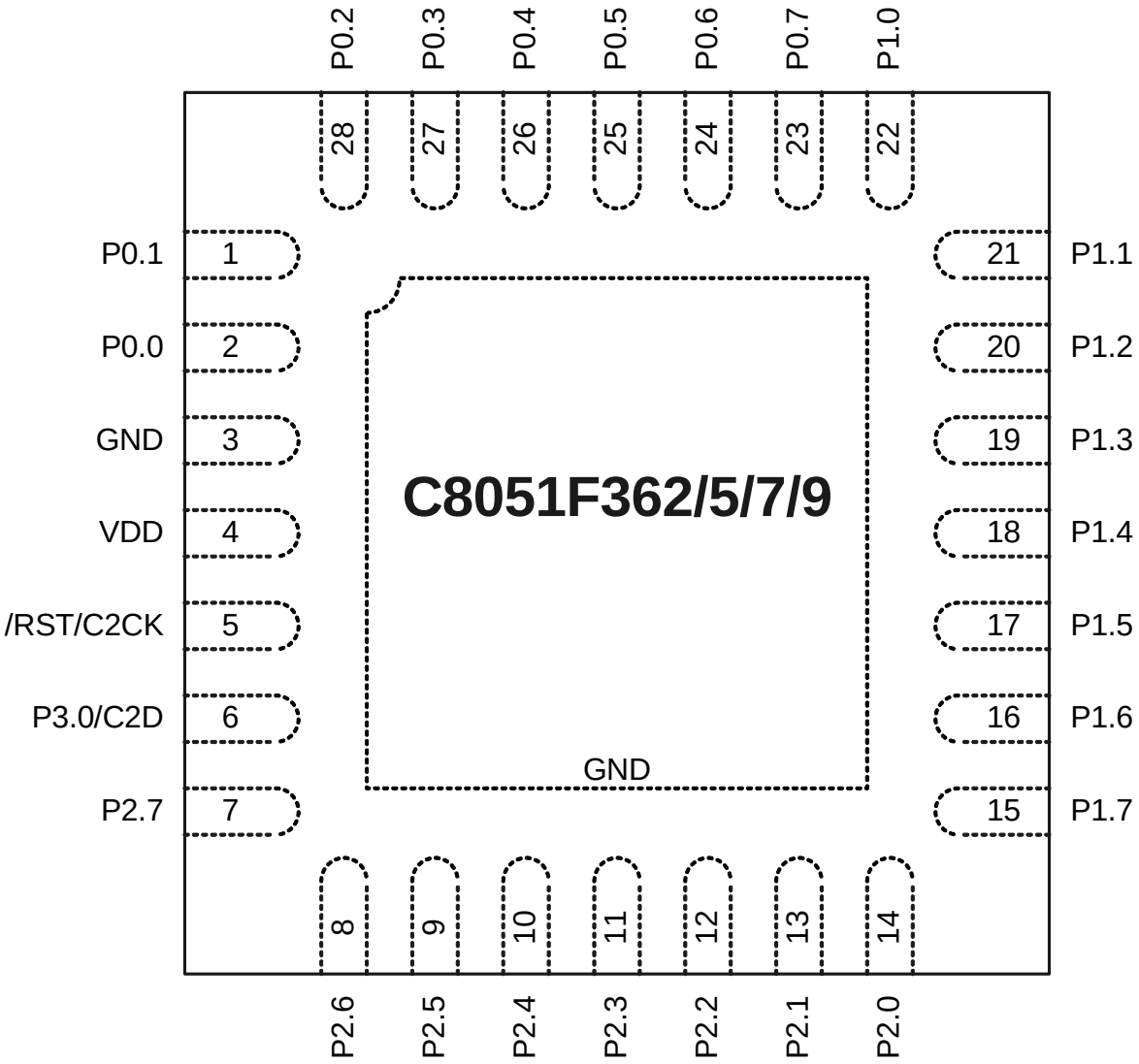

Figure 4.5. QFN-28 Pinout Diagram (Top View)

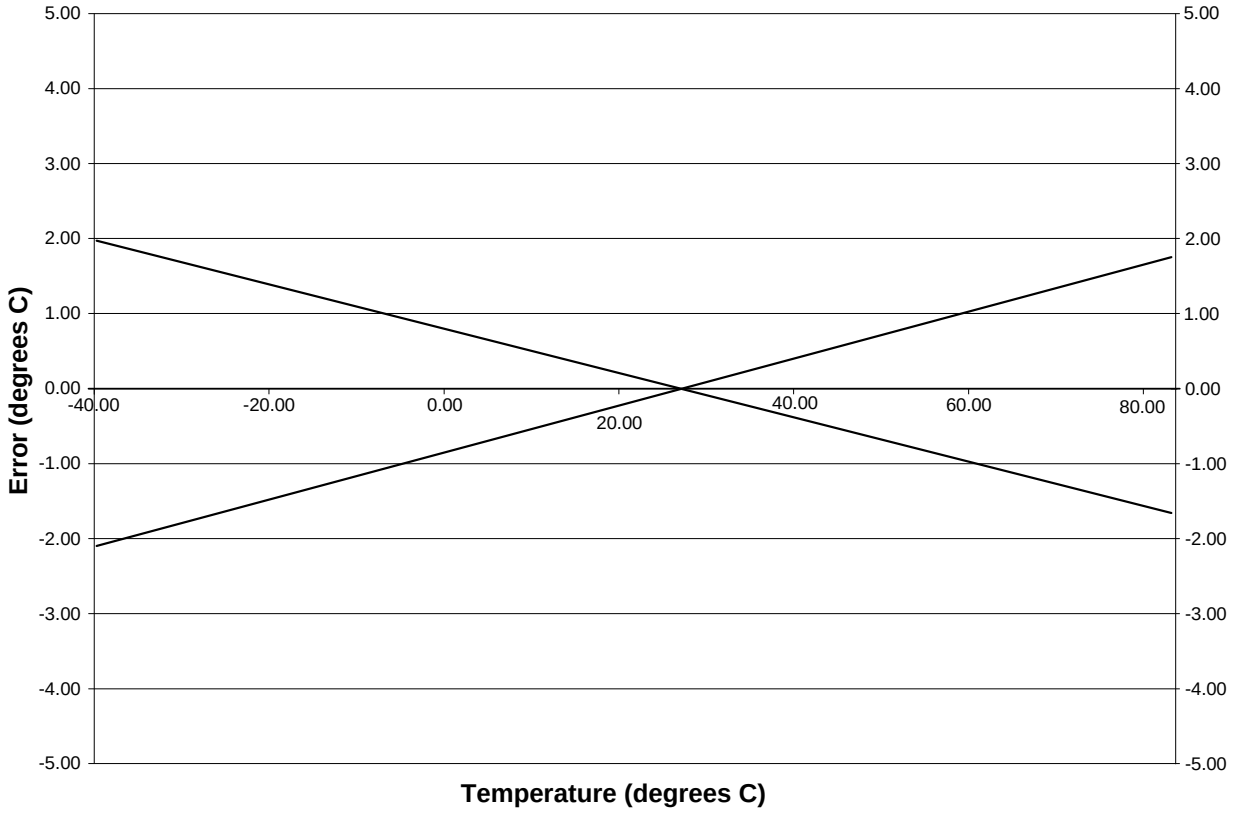

Figure 5.3. Temperature Sensor Error with 1-Point Calibration

5.4.1. Window Detector In Single-Ended Mode

Figure 5.6 shows two example window comparisons for right-justified, single-ended data, with ADC0LTH:ADC0LTL = 0x0080 (128d) and ADC0GTH:ADC0GTL = 0x0040 (64d). In single-ended mode, the input voltage can range from '0' to VREF x (1023/1024) with respect to GND, and is represented by a 10-bit unsigned integer value. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0040 < ADC0H:ADC0L < 0x0080). In the right example, and AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0040 or ADC0H:ADC0L > 0x0080). Figure 5.7 shows an example using left-justified data with the same comparison values.

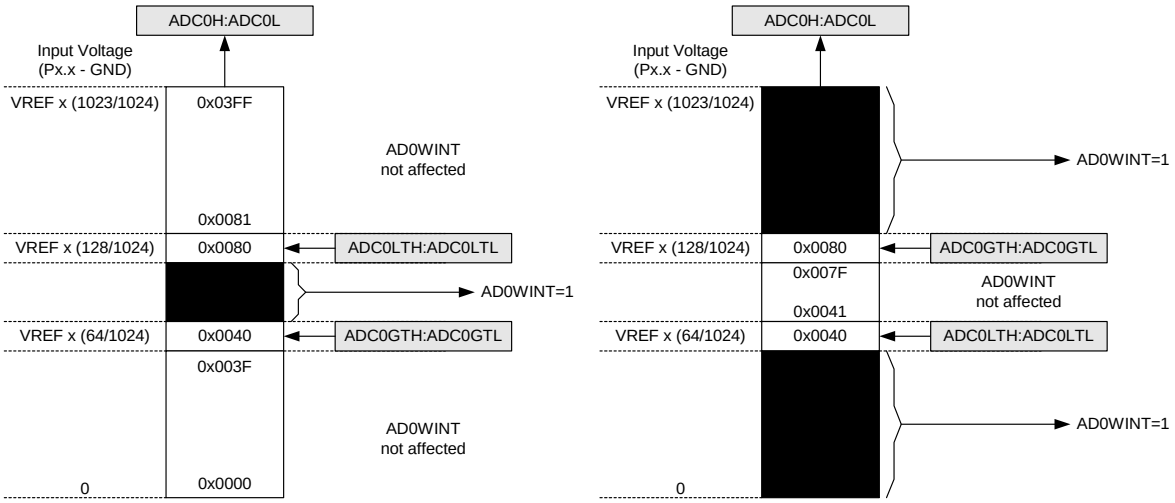

Figure 5.6. ADC Window Compare Example: Right-Justified Single-Ended Data

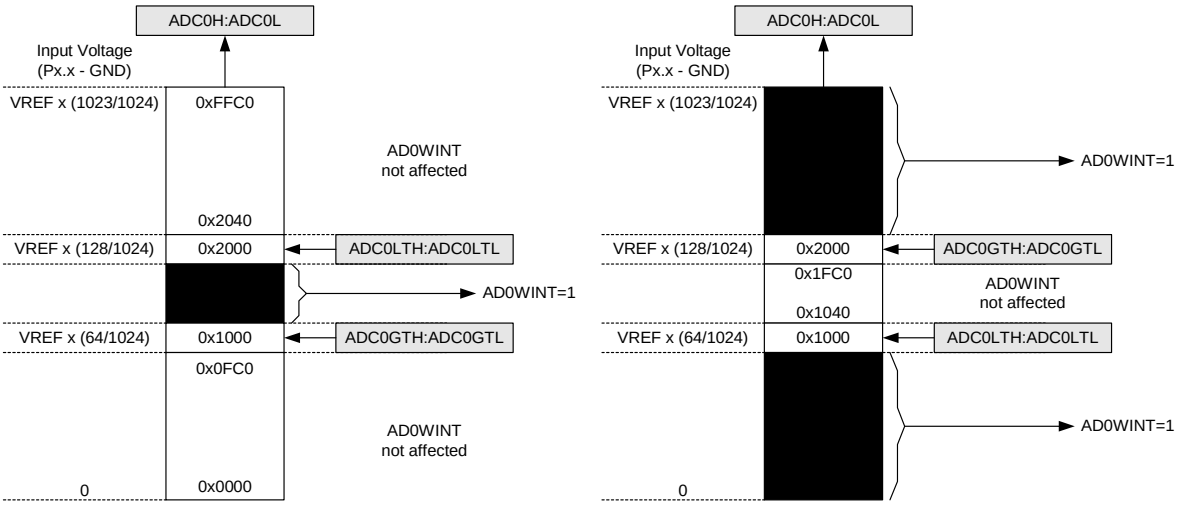

Figure 5.7. ADC Window Compare Example: Left-Justified Single-Ended Data

9.4.2. Data Memory

The CIP-51 implements 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFR's. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 9.2 illustrates the data memory organization of the CIP-51.

9.4.3. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 9.8). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

9.4.4. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit 7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination). The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte.

For example, the instruction:

```
MOV    C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

9.4.5. Stack

A programmer's stack can be located anywhere in the 256 byte data memory. The stack area is designated using the Stack Pointer (SP, address 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07; therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

The MCUs also have built-in hardware for a stack record which is accessed by the debug logic. The stack record is a 32-bit shift register, where each PUSH or increment SP pushes one record bit onto the register,

SFR Definition 9.9. ACC: Accumulator

SFR Page: all pages
SFR Address: 0xE0 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: ACC: Accumulator.
This register is the accumulator for arithmetic operations.

SFR Definition 9.10. B: B Register

SFR Page: all pages
SFR Address: 0xF0 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: B: B Register.
This register serves as a second accumulator for certain arithmetic operations.

9.5. Power Management Modes

The CIP-51 core has two software programmable power management modes: Idle and Stop. Idle mode halts the CPU while leaving the external peripherals and internal clocks active. In Stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the system clock is stopped. Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power. SFR Definition 9.11 describes the Power Control Register (PCON) used to control the CIP-51's power management modes.

Although the CIP-51 has Idle and Stop modes built in (as with any standard 8051 architecture), power management of the entire MCU is better accomplished by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and put into low power mode. Digital peripherals, such as timers or serial buses, draw little power whenever they are not in use. Turning off the Flash memory saves power, similar to entering Idle mode. Turning off the oscillator saves even more power, but requires a reset to restart the MCU.

The C8051F36x devices feature an additional low-power SUSPEND mode, which stops the internal oscillator until an awakening event occurs. See Section “16.1.1. Internal Oscillator Suspend Mode” on page 169 for more information.

SFR Definition 10.2. IP: Interrupt Priority

SFR Page: all pages
SFR Address: 0xB8 (bit addressable)

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	PSPI0	PT2	PS0	PT1	PX1	PT0	PX0	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: UNUSED. Read = 1b, Write = don't care.
Bit 6: PSPI0: Serial Peripheral Interface (SPI0) Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.
Bit 5: PT2: Timer 2 Interrupt Priority Control.
This bit sets the priority of the Timer 2 interrupt.
0: Timer 2 interrupt set to low priority level.
1: Timer 2 interrupt set to high priority level.
Bit 4: PS0: UART0 Interrupt Priority Control.
This bit sets the priority of the UART0 interrupt.
0: UART0 interrupt set to low priority level.
1: UART0 interrupt set to high priority level.
Bit 3: PT1: Timer 1 Interrupt Priority Control.
This bit sets the priority of the Timer 1 interrupt.
0: Timer 1 interrupt set to low priority level.
1: Timer 1 interrupt set to high priority level.
Bit 2: PX1: External Interrupt 1 Priority Control.
This bit sets the priority of the External Interrupt 1 interrupt.
0: External Interrupt 1 set to low priority level.
1: External Interrupt 1 set to high priority level.
Bit 1: PT0: Timer 0 Interrupt Priority Control.
This bit sets the priority of the Timer 0 interrupt.
0: Timer 0 interrupt set to low priority level.
1: Timer 0 interrupt set to high priority level.
Bit 0: PX0: External Interrupt 0 Priority Control.
This bit sets the priority of the External Interrupt 0 interrupt.
0: External Interrupt 0 set to low priority level.
1: External Interrupt 0 set to high priority level.

11.7.2. Multiply Only Example

The example below implements the equation:

$$4660 \times -292 = -1360720$$

```
MOV   MAC0CF, #01h    ; Use integer numbers, and multiply only mode (add to zero)
MOV   MAC0AH, #12h    ; Load MAC0A register with 1234 hex = 4660 decimal
MOV   MAC0AL, #34h
MOV   MAC0BH, #FEh    ; Load MAC0B register with FEDC hex = -292 decimal
MOV   MAC0BL, #DCh    ; This line initiates the Multiply operation
NOP
NOP                   ; After this instruction, the Accumulator should be equal to
                      ; FFFFEB3CB0 hex = -1360720 decimal. The MAC0STA register should
                      ; be 0x01, indicating a negative result.
NOP                   ; After this instruction, the Rounding register is updated
```

11.7.3. MAC0 Accumulator Shift Example

The example below shifts the MAC0 accumulator left one bit, and then right two bits:

```
MOV   MAC0OVR, #40h   ; The next few instructions load the accumulator with the value
MOV   MAC0ACC3, #88h  ; 4088442211 Hex.
MOV   MAC0ACC2, #44h
MOV   MAC0ACC1, #22h
MOV   MAC0ACC0, #11h
MOV   MAC0CF, #20h    ; Initiate a Left-shift
NOP                   ; After this instruction, the accumulator should be 0x8110884422
NOP                   ; The rounding register is updated after this instruction
MOV   MAC0CF, #30h    ; Initiate a Right-shift
MOV   MAC0CF, #30h    ; Initiate a second Right-shift
NOP                   ; After this instruction, the accumulator should be 0xE044221108
NOP                   ; The rounding register is updated after this instruction
```

13. Flash Memory

All devices include either 32 kB (C8051F360/1/2/3/4/5/6/7) or 16 kB (C8051F368/9) of on-chip, reprogrammable Flash memory for program code or non-volatile data storage. The Flash memory can be programmed in-system through the C2 interface, or by software using the MOVX write instructions. Once cleared to logic ‘0’, a Flash bit must be erased to set it back to logic ‘1’. Bytes should be erased (set to 0xFF) before being reprogrammed. Flash write and erase operations are automatically timed by hardware for proper execution. During a Flash erase or write, the FLBUSY bit in the FLSTAT register is set to ‘1’ (see SFR Definition 14.5). During this time, instructions that are located in the prefetch buffer or the branch target cache can be executed, but the processor will stall until the erase or write is completed if instruction data must be fetched from Flash memory. Interrupts that have been pre-loaded into the branch target cache can also be serviced at this time, if the current code is also executing from the prefetch engine or cache memory. Any interrupts that are not pre-loaded into cache, or that occur while the core is halted, will be held in a pending state during the Flash write/erase operation, and serviced in priority order once the Flash operation has completed. Refer to Table 13.2 for the electrical characteristics of the Flash memory.

13.1. Programming the Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Labs or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section “24. C2 Interface” on page 283. For detailed guidelines on writing or erasing Flash from firmware, please see Section “13.3. Flash Write and Erase Guidelines” on page 140.

The Flash memory can be programmed from software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before writing to Flash memory using MOVX, Flash write operations must be enabled by setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic ‘1’. This directs the MOVX writes to Flash memory instead of to XRAM, which is the default target. The PSWE bit remains set until cleared by software. To avoid errant Flash writes, it is recommended that interrupts be disabled while the PSWE bit is logic ‘1’.

Flash memory is read using the MOVC instruction. MOVX reads are always directed to XRAM, regardless of the state of PSWE.

Note: To ensure the integrity of the Flash contents, the on-chip V_{DD} Monitor must be enabled in any system that includes code that writes and/or erases Flash memory from software. Furthermore, there should be no delay between enabling the V_{DD} Monitor and enabling the V_{DD} Monitor as a reset source. Any attempt to write or erase Flash memory while the V_{DD} Monitor disabled will cause a Flash Error device reset.

A write to Flash memory can clear bits but cannot set them; only an erase operation can set bits in Flash. **A byte location to be programmed must be erased before a new value can be written**.

Write/Erase timing is automatically controlled by hardware. Note that on the 32 k Flash devices, 1024 bytes beginning at location 0x7C00 are reserved. Flash writes and erases targeting the reserved area should be avoided.

13.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and

15.6.1.3.8-bit MOVX with Bank Select: EMI0CF[4:2] = ‘110’.

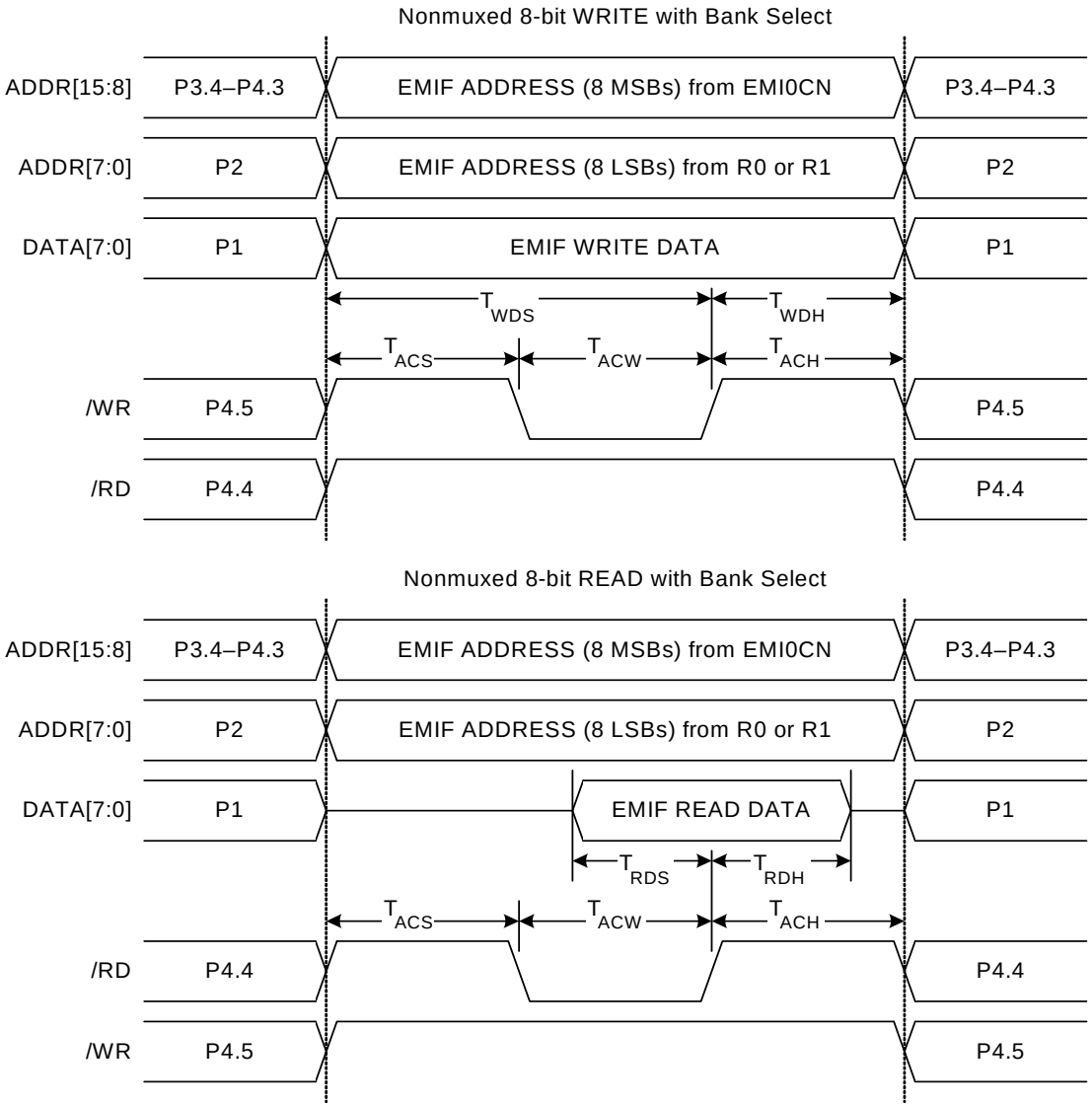

Figure 15.6. Non-multiplexed 8-bit MOVX with Bank Select Timing

16. Oscillators

The C8051F36x devices include a programmable internal high-frequency oscillator, a programmable internal low-frequency oscillator, and an external oscillator drive circuit. The internal high-frequency oscillator can be enabled, disabled, and calibrated using the OSCICN and OSCICL registers, as shown in Figure 16.1. The internal low-frequency oscillator can be enabled/disabled and calibrated using the OSCLCN register, as shown in SFR Definition 16.3. Both internal oscillators offer a selectable post-scaling feature. The system clock can be sourced by the external oscillator circuit, either internal oscillator, or the on-chip phase-locked loop (PLL). The internal oscillator's electrical specifications are given in Table 16.1 on page 170 and Table 16.2 on page 171.

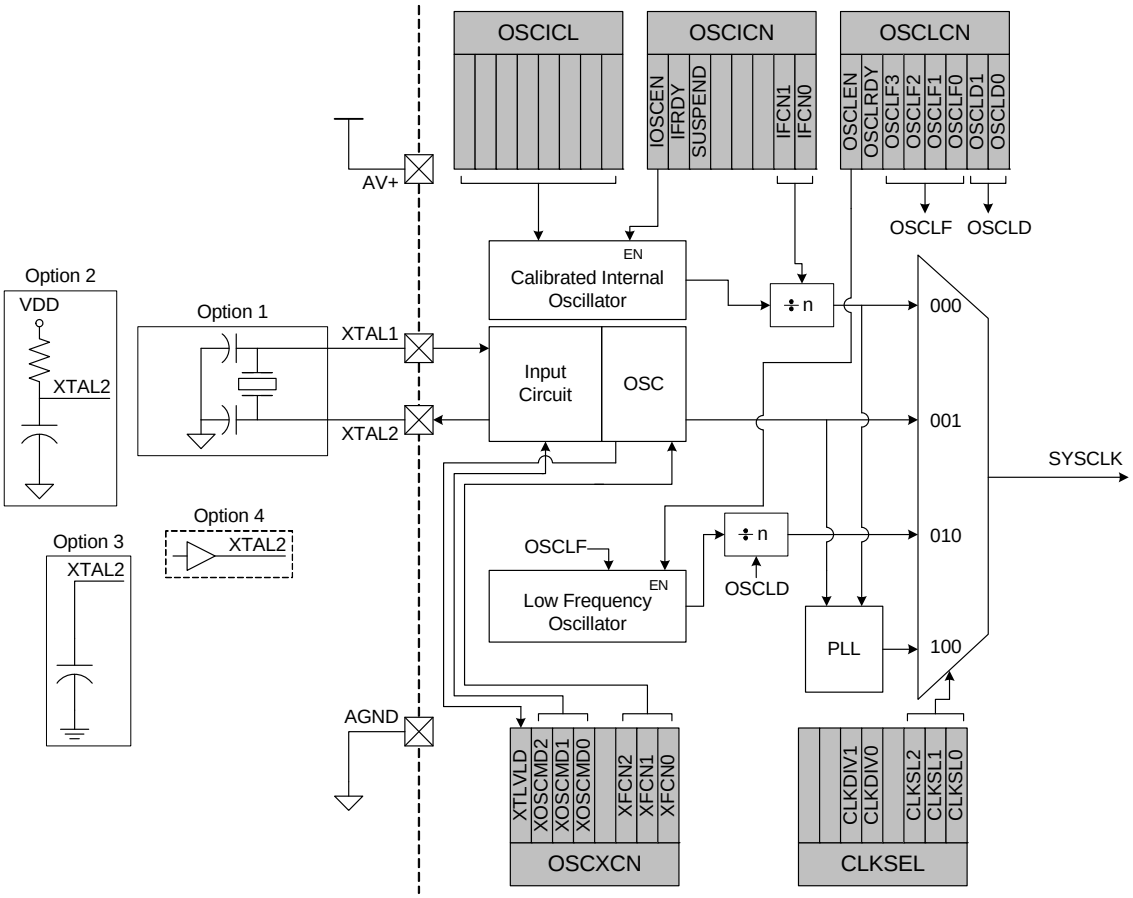

Figure 16.1. Oscillator Diagram

16.1. Programmable Internal High-Frequency (H-F) Oscillator

All devices include a calibrated internal high-frequency oscillator that defaults as the system clock after a system reset. The internal oscillator period can be adjusted via the OSCICL register as defined by SFR Definition 16.1. OSCICL is factory calibrated to obtain a 24.5 MHz frequency.

Electrical specifications for the precision internal oscillator are given in Table 16.1 on page 170 and Table 16.2 on page 171. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, or 8, as defined by the IFCN bits in register OSCICN. The divide value defaults to 8 following a reset.

16.6. External RC Example

If an RC network is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 16.1, Option 2. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. If the frequency desired is 100 kHz, let R = 246 kΩ and C = 50 pF:

$f = 1.23(10^3)/RC = 1.23\ (10^3)/[246 \times 50] = 0.1\ MHz = 100\ kHz$

Referring to the table in SFR Definition 16.5, the required XFCN setting is 010b. Programming XFCN to a higher setting in RC mode will improve frequency accuracy at a slightly increased external oscillator supply current.

16.7. External Capacitor Example

If a capacitor is used as an external oscillator for the MCU, the circuit should be configured as shown in Figure 16.1, Option 3. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume V_{DD} = 3.0 V and f = 75 kHz:

$f = KF / (C \times V_{DD})$
$0.075\ MHz = KF / (C \times 3.0)$

Since the frequency of roughly 75 kHz is desired, select the K Factor from the table in SFR Definition 16.5 as KF = 7.7:

$0.075\ MHz = 7.7 / (C \times 3.0)$

$C \times 3.0 = 7.7 / 0.075\ MHz$

$C = 102.6 / 3.0\ pF = 34.2\ pF$

Therefore, the XFCN value to use in this example is 010b.

SFR Definition 16.8. PLL0MUL: PLL Clock Scaler

SFR Page: F
SFR Address: 0xB1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PLLN7	PLLN6	PLLN5	PLLN4	PLLN3	PLLN2	PLLN1	PLLN0	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: PLLN7–0: PLL Multiplier.
These bits select the multiplication factor of the divided PLL reference clock. When set to any non-zero value, the multiplication factor will be equal to the value in PLLN7-0. When set to ‘00000000b’, the multiplication factor will be equal to 256.

SFR Definition 16.9. PLL0FLT: PLL Filter

SFR Page: F
SFR Address: 0xB2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	PLLICO1	PLLICO0	PLLLP3	PLLLP2	PLLLP1	PLLLP0	00110001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–6: UNUSED. Read = 00b. Write = don’t care.
Bits 5–4: PLLICO1-0: PLL Current-Controlled Oscillator Control Bits.
Selection is based on the desired output frequency, according to the following table:

PLL Output Clock	PLLICO1-0
65–100 MHz	00
45–80 MHz	01
30–60 MHz	10
25–50 MHz	11

Bits 3–0: PLLLP3-0: PLL Loop Filter Control Bits.
Selection is based on the divided PLL reference clock, according to the following table:

Divided PLL Reference Clock	PLLLP3-0
19–30 MHz	0001
12.2–19.5 MHz	0011
7.8–12.5 MHz	0111
5–8 MHz	1111

All other states of PLLLP3–0 are RESERVED.

SFR Definition 17.1. XBR0: Port I/O Crossbar Register 0

SFR Page: F
SFR Address: 0xE1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CP1AE	CP1E	CP0AE	CP0E	SYSCKE	SMB0E	SPI0E	URT0E	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: CP1AE: Comparator1 Asynchronous Output Enable
0: Asynchronous CP1 unavailable at Port pin.
1: Asynchronous CP1 routed to Port pin.

Bit 6: CP1E: Comparator1 Output Enable
0: CP1 unavailable at Port pin.
1: CP1 routed to Port pin.

Bit 5: CP0AE: Comparator0 Asynchronous Output Enable
0: Asynchronous CP0 unavailable at Port pin.
1: Asynchronous CP0 routed to Port pin.

Bit 4: CP0E: Comparator0 Output Enable
0: CP0 unavailable at Port pin.
1: CP0 routed to Port pin.

Bit 3: SYSCKE: /SYSCLK Output Enable
0: /SYSCLK unavailable at Port pin.
1: /SYSCLK (divided by 1, 2, 4, or 8) routed to Port pin. The divide factor is determined by the CLKDIV1–0 bits in register CLKSEL (See Section Section “16. Oscillators” on page 168).

Bit 2: SMB0E: SMBus I/O Enable
0: SMBus I/O unavailable at Port pins.
1: SMBus I/O routed to Port pins.

Bit 1: SPI0E: SPI I/O Enable
0: SPI I/O unavailable at Port pins.
1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO pins.

Bit 0: URT0E: UART I/O Output Enable
0: UART I/O unavailable at Port pin.
1: UART TX0, RX0 routed to Port pins P0.1 and P0.2 (C8051F360/3) or P0.4 and P0.5 (C8051F361/2/4/5/6/7/8/9).

Table 19.5. Timer Settings for Standard Baud Rates Using an External 11.0592 MHz Oscillator

	Frequency: 11.0592 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)[1]	T1M[1]	Timer 1 Reload Value (hex)
SYSCLK and Timer Clock from External Osc.	230400	0.00%	48	SYSCLK	XX[2]	1	0xE8
	115200	0.00%	96	SYSCLK	XX	1	0xD0
	57600	0.00%	192	SYSCLK	XX	1	0xA0
	28800	0.00%	384	SYSCLK	XX	1	0x40
	14400	0.00%	768	SYSCLK/12	00	0	0xE0
	9600	0.00%	1152	SYSCLK/12	00	0	0xD0
	2400	0.00%	4608	SYSCLK/12	00	0	0x40
	1200	0.00%	9216	SYSCLK/48	10	0	0xA0
SYSCLK from Internal Osc., Timer Clock from External Osc.	230400	0.00%	48	EXTCLK/8	11	0	0xFD
	115200	0.00%	96	EXTCLK/8	11	0	0xFA
	57600	0.00%	192	EXTCLK/8	11	0	0xF4
	28800	0.00%	384	EXTCLK/8	11	0	0xE8
	14400	0.00%	768	EXTCLK/8	11	0	0xD0
	9600	0.00%	1152	EXTCLK/8	11	0	0xB8

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 21.1.
2. X = Don't care.

20.2. SPI0 Master Mode Operation

A SPI master device initiates all data transfers on a SPI bus. SPI0 is placed in master mode by setting the Master Enable flag (MSTEN, SPI0CN.6). Writing a byte of data to the SPI0 data register (SPI0DAT) when in master mode writes to the transmit buffer. If the SPI shift register is empty, the byte in the transmit buffer is moved to the shift register, and a data transfer begins. The SPI0 master immediately shifts out the data serially on the MOSI line while providing the serial clock on SCK. The SPIF (SPI0CN.7) flag is set to logic '1' at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers the contents of its shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CN.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 20.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used, and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 20.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin, and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 20.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.

21.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. The counter/timer in TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/T0, GATE0 and TF0. TL0 can use either the system clock or an external input signal as its timebase. The TH0 register is restricted to a timer function sourced by the system clock or prescaled clock. TH0 is enabled using the Timer 1 run control bit TR1. TH0 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

Timer 1 is inactive in Mode 3. When Timer 0 is operating in Mode 3, Timer 1 can be operated in Modes 0, 1 or 2, but cannot be clocked by external signals nor set the TF1 flag and generate an interrupt. However, the Timer 1 overflow can be used to generate baud rates for the SMBus and/or UART, and/or initiate ADC conversions. While Timer 0 is operating in Mode 3, Timer 1 run control is handled through its mode settings. To run Timer 1 while Timer 0 is in Mode 3, set the Timer 1 Mode as 0, 1, or 2. To disable Timer 1, configure it for Mode 3.

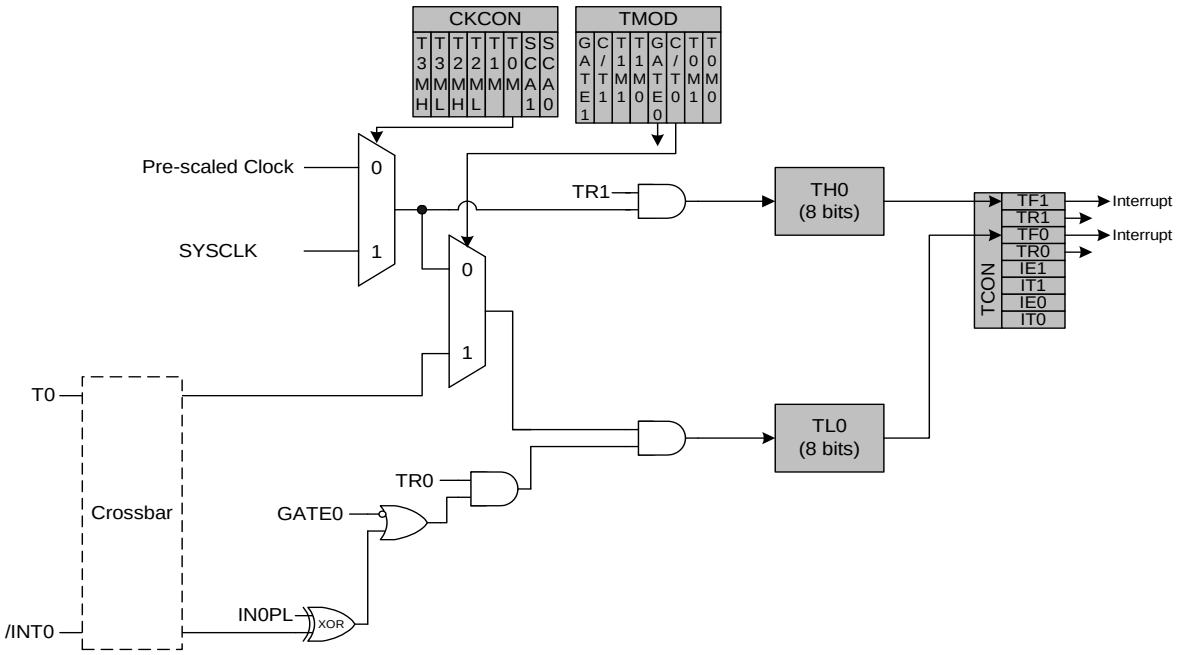

Figure 21.3. T0 Mode 3 Block Diagram

SFR Definition 22.7. PCA0CPHn: PCA0 Capture Module High Byte

SFR Page: PCA0CPH0: all pages, PCA0CPH1: all pages, PCA0CPH2: all pages, PCA0CPH3: all pages, PCA0CPH4: all pages, PCA0CPH5: all pages

SFR Address: PCA0CPH0: 0xFC, PCA0CPH1: 0xEA, PCA0CPH2: 0xEC, PCA0CPH3: 0xEE, PCA0CPH4: 0xFE, PCA0CPH5: 0xF6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: PCA0CPHn: PCA0 Capture Module High Byte.
The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated specification tables with most recently available characterization data.
- Fixed an error with the SYSCLK specification in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Corrected the name of the PMAT bit in SFR Definition 10.2. IP: Interrupt Priority.
- Corrected the reset value for SFR Definition 22.2. PCA0MD: PCA0 Mode.

Revision 0.2 to Revision 1.0

- Updated specification tables with characterization data.
- Fixed Table 1.1, “Product Selection Guide,” on page 19 to reflect the correct number of Port I/O pins for the C8051F361/2/4/5.
- Updated Section “10. Interrupt Handler” on page 107.
  - Added note describing EA change behavior when followed by single cycle instruction.
- Updated SFR Definition 11.1
  - Changed the MAC0SC (MAC0CF.5) bit description to correctly refer to the MAC0SD bit.
- Updated SFR Definition 15.2.
  - Changed the EMI0CF description to properly describe the 1k XRAM boundaries.
- Added Table 16.2, “Internal Low Frequency Oscillator Electrical Characteristics,” on page 171.
- Updated SFR Definition 16.9:
  - Specified that the undefined states for PLLLP3–0 are RESERVED.
- Added Table 19.7 and Table 19.8 on page 231 for UART Baud Rates when using the PLL.
- Updated Table 22.1, “PCA Timebase Input Options,” on page 263:
  - Specified that the undefined states of CPS2–0 are RESERVED.
- Added Revision B to “Revision Specific Behavior” on page 279.

Revision 1.0 to Revision 1.1

- Updated ordering table with Revision C part numbers.
- Updated Figure 17.2. ’Port I/O Cell Block Diagram’ on page 183 to refer to VDD instead of VIO.
- Added Revision C to “Revision Specific Behavior” on page 279.
- Added Revision C to the REVID C2 register in C2 Register Definition 24.3.
- Updated “Digital Supply Current (Stop Mode, shutdown)” typical value in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Updated “Missing Clock Detector Timeout” typical value in Table 12.1, “Reset Electrical Characteristics,” on page 134.