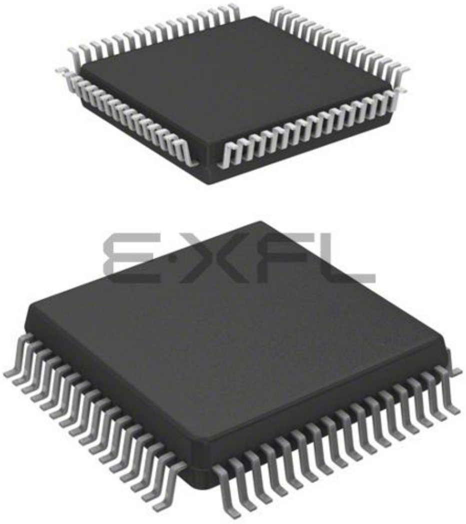
NXP USA Inc. - MC68EC000AA16R2 Datasheet



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	EC000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68ec000aa16r2

Freescale Semiconductor, Inc.

The primary features of the MC68SEC000 embedded processor include the following:

- Direct Replacement for the MC68EC000
  - Pin-for-pin compatibility with the MC68EC000 in the plastic QFP and TQFP packages
  - Vast selection of existing third-party development tools for the MC68EC000 support the MC68SEC000
  - Software written for the MC68EC000 will run unchanged on the MC68SEC000
- Power Management
  - Low-power HCMOS technology
  - Static design allows for stopping the processor clock
  - 3.3V or 5V operation
  - Typical 0.5µA current consumption at 3.3V in sleep mode
- Software Strength
  - Fully upward object-code compatible with other M68000 Family products
  - M68000 architecture allows effective assembly code with a C compiler
- Upgrade
  - Fully upward code-compatible with higher performance 680x0 and 68300 Family members
  - ColdFire® code-compatible with minor modifications

1. MC68HC000

The primary benefit of the MC68HC000 is reduced power consumption. The device dissipates less power (by an order of magnitude) than the NMOS MC68000.

The MC68HC000 is an implementation of the M68000 16/-32 bit microprocessor architecture. The MC68HC000 has a 16-bit data bus implementation of the MC68000 and is upward code-compatible with the MC68010 and the MC68020 32-bit implementation of the architecture.

1.1 MC68HC001

The MC68HC001 provides a functional extension to the MC68HC000 HCMOS 16-/32-bit microprocessor with the addition of statically selectable 8- or 16-bit data bus operation. The MC68HC001 is object-code compatible with the MC68HC000. You can migrate code written for the MC68HC001 without modification to any member of the M68000 Family.

1.2 MC68EC000

The MC68EC000 is an economical high-performance embedded controller designed to suit the needs of the cost-sensitive embedded-controller market. The HCMOS MC68EC000 has an internal 32-bit architecture that is supported by a statically selectable 8- or 16-bit data bus. This architecture provides a fast and efficient processing device that can satisfy the requirements of sophisticated applications based on high-level languages.

The MC68EC000 is fully object-code compatible with the MC68000. You can migrate code written for the MC68EC000 without modification to any member of the M68000 Family.

The MC68EC000 brings the performance level of the M68000 Family to cost levels previously associated with 8-bit microprocessors. The MC68EC000 benefits from the rich M68000 instruction set and its related high code density with low memory bandwidth requirements.

1.3 MC68SEC000

The MC68SEC000 is a cost-effective static embedded processor engineered for low-power applications. In addition to providing the substantial cost and performance benefits of the MC68EC000, the low-power mode of the MC68SEC000 provides significant advantages in power consumption and power management. The typical current consumption of the MC68SEC000 is only 0.5µA in static standby mode and 15.0mA in normal 3.3V operation. The MC68SEC000 operates in either 3.3V or 5.0V systems. The remarkably low power consumption, small footprint packages, and static implementation are combined in the MC68SEC000 for low-power applications such as portable measuring equipment, electronic games, and battery-operated hand-held consumer products.

The HCMOS MC68SEC000's static architecture is a direct replacement for the MC68EC000, which offers the lowest cost entry point to 32-bit processing. The internal 32-bit architecture provides fast and efficient processing that satisfies the requirements of sophisticated applications based on high-level languages.

All of the existing third-party developer tools widely available for the MC68EC000 will directly support the MC68SEC000. You can find detailed descriptions of these tools in the *High Performance Embedded Systems Source Catalog*.

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

2.0 SIGNAL DESCRIPTION

Change Figure 3-3 on Page 3-2.

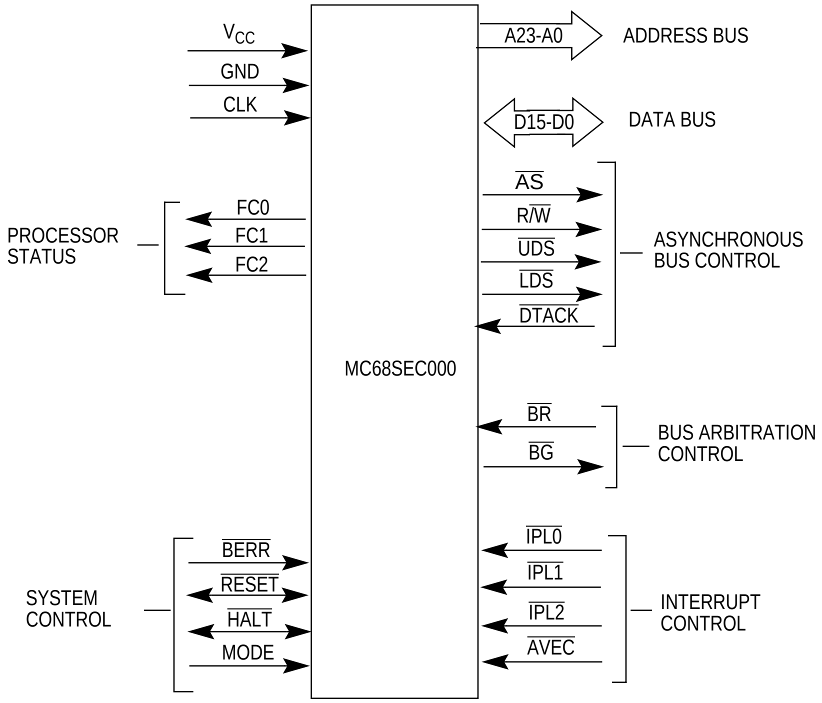


Figure 1. Input and Output Signals (MC68EC000 and MC68SEC000)

2.1 Data Bus (D15-D0)

In Section 3.2 on page 3-4, replace “The MC68EC000 and MC68HC001 use D7-D0 in 8-bit mode, and D15-D8 are undefined.” with “Using the MC68HC001, MC68EC000, and MC68SEC000 mode pin, you can statically select either 8- or 16-bit modes for data transfer. The MC68EC000, MC68SEC000, and MC68HC001 use D7-D0 in 8-bit mode. D15-D8 are undefined.”

2.2 Bus Arbitration Control

In Section 3.4 on page 3-5, the sentence “In the 48-pin version of the MC68008 and MC68EC000, no pin is available for the bus grant acknowledge signal; this microprocessor uses a two-wire bus arbitration scheme.” should read “In the 64-pin MC68EC000 and MC68SEC000, no pin is available for the bus grant acknowledge signal. These microprocessors use a two-wire bus arbitration scheme.”

2.3 System Control

The Mode subsection heading of Section 3.6 on page 3-7 should read ‘‘Mode (MODE) (MC68HC001/68EC000/68SEC000).’’

2.4 MC68SEC000 Low-Power Mode

Add the following to Sections 4 and 5, Bus Operation.

The MC68SEC000 has been redesigned to provide fully static- and low-power operation. This section describes the recommended method for placing the MC68SEC000 into a low-power mode to reduce the

Freescale Semiconductor, Inc.

8-bit mode requires two bus cycles to fetch the immediate data of the STOP instruction. After the processor clock is disabled, it is often necessary to disable the clock to other sections of your circuit. This can be done, but be careful that runt clocks and spurious glitches are not presented to the MC68SEC000. A timing diagram is shown in Figure 4.

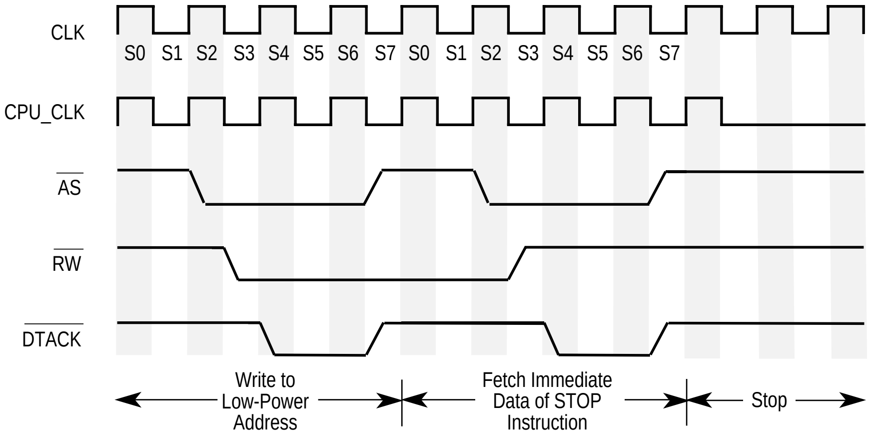


Figure 4. MC68SEC000 Clock Stop Timing for 16-Bit Data Bus

Note: While the MC68SEC000 is in the low-power mode, all inputs must be driven to V_{DD} or V_{SS}, or have a pull-up or pull-down resistor.

3. This step is optional depending on whether your applications require the MC68SEC000 signals with three-state capability to be placed into a high-impedance state. To place the MC68SEC000 into a three-state condition, the proper method for arbitrating the bus (as described in **5.2 Bus Arbitration** in the *M68000 User's Manual, Rev 8*) should be completed during the fetch of the status register data for the STOP instruction. A timing diagram with the bus arbitration sequence is shown in Figure 5.

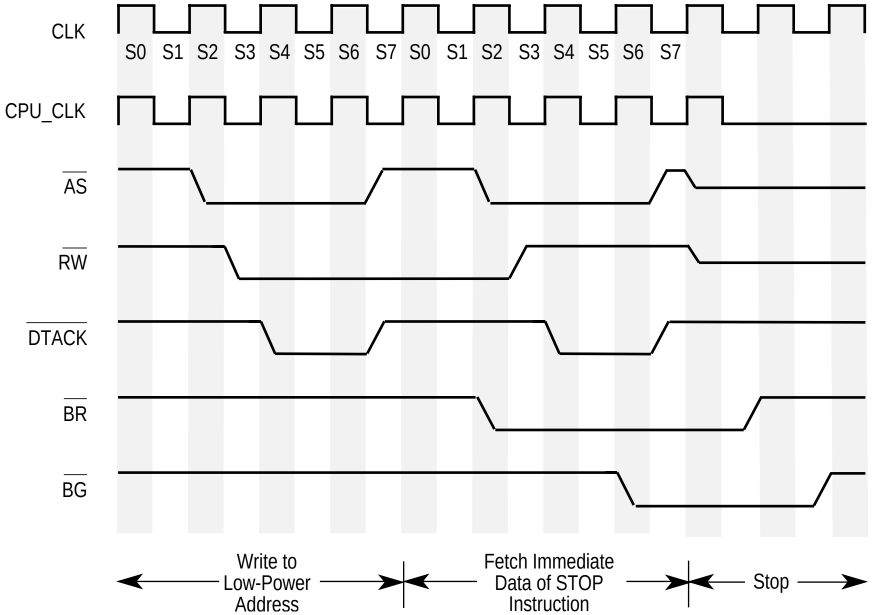


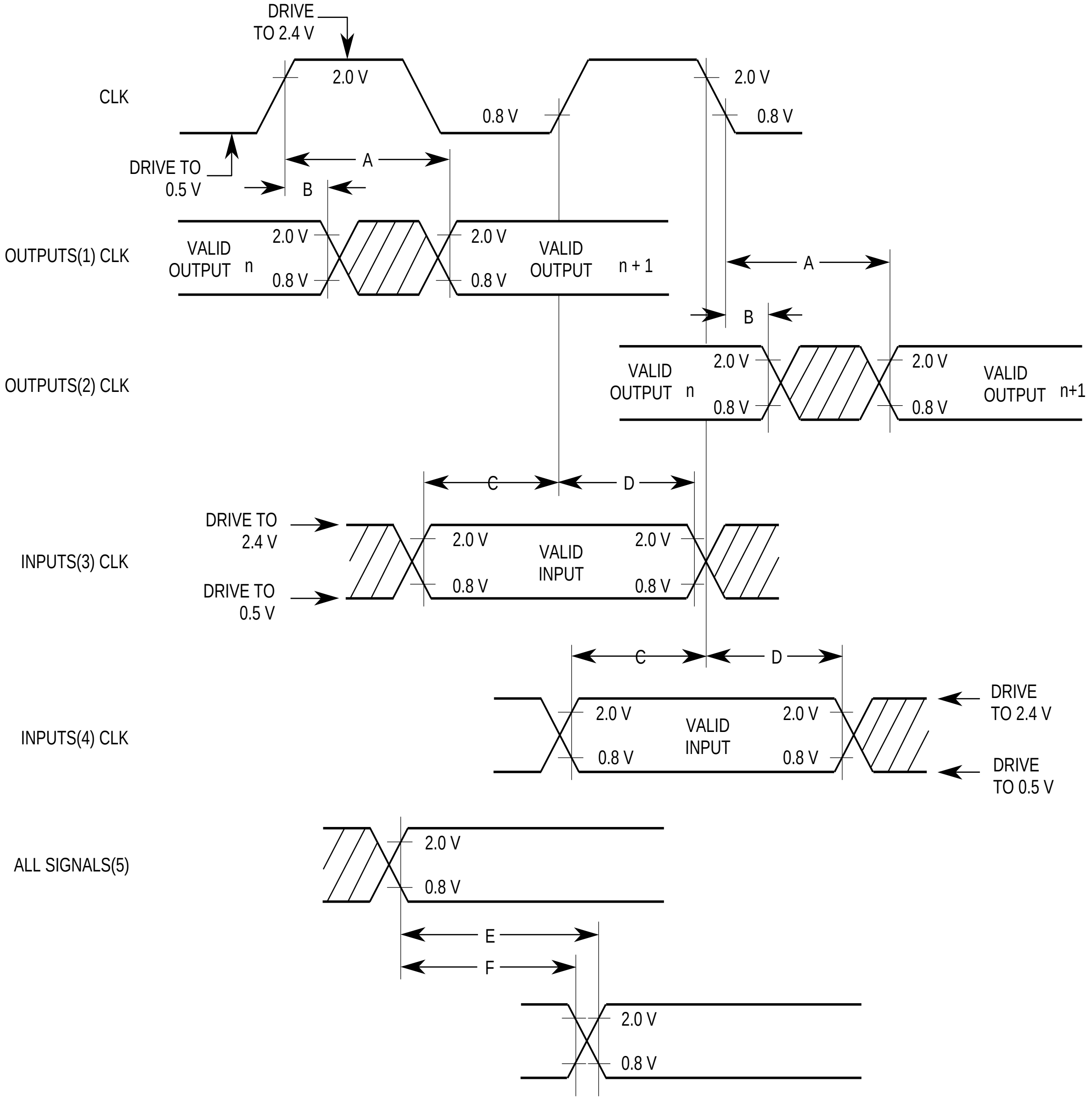
Figure 5. MC68SEC000 Clock Stop Timing with Bus Arbitration for 16-Bit Data Bus

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

4.0 MC68SEC000 AC ELECTRICAL SPECIFICATIONS

Replace Figure 10-2 on page 10-6 with Figure 7.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 7. Drive Levels and Test Points for AC Specifications - applies to all parts

Freescale Semiconductor, Inc.

5.0 MC68SEC000 DC ELECTRICAL SPECIFICATIONS

Add the following table to Section 10.13 on page 10-23.

(V_{CC} = 5.0 Vdc ±5%, 3.3 Vdc ±10%,; GND = 0 Vdc; $T_A = T_L$ to T_H)

CHARACTERISTIC	SYMBOL	3.3 V		5.0 V		UNIT
		MIN	MAX	MIN	MAX	
Input High Voltage	V_{IH}	2.0	V_{CC}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	GND – 0.5	0.8	V
Input Leakage Current $\overline{\text{BERR}}$, $\overline{\text{BR}}$, $\overline{\text{DTACK}}$, CLK, $\overline{\text{IPL2}}$-$\overline{\text{IPL0}}$, $\overline{\text{AVEC}}$ MODE, $\overline{\text{HALT}}$, $\overline{\text{RESET}}$	Iin	—	2.5 20	—	2.5 20	uA
Three-State (Off State) Input Current	I_{TSI}	—	2.5	—	2.5	uA
Output High Voltage	V_{OH}	2.4	—	V_{CC}–0.75	—	V
Output Low Voltage (IOL = 1.6 mA) $\overline{\text{HALT}}$ (IOL = 3.2 mA) A23–A0, $\overline{\text{BG}}$, FC2–FC0 (IOL = 5.0 mA) $\overline{\text{RESET}}$ (IOL = 5.3 mA) $\overline{\text{AS}}$, D15–D0, $\overline{\text{LDS}}$, R/$\overline{\text{W}}$, $\overline{\text{UDS}}$	V_{OL}	 — — — —	 0.5 0.5 0.5 0.5	 — — — —	 0.5 0.5 0.5 0.5	V
Current Dissipation* f = 0 Hz	I_D	—	0.7	—	1.0	mA
f=10MHz		—	10	—	15	mA
f=16 MHz		—	15	—	25	mA
f= 20 MHz		—	20	—	30	mA
Capacitance (Vin = 0 V, T_A = 25 °C, Frequency = 1 MHz)**	Cin	—	20.0	—	20.0	pF
Load Capacitance $\overline{\text{HALT}}$ All Others	CL	—	70 130	—	70 130	pF

*During normal operation, instantaneous Vcc current requirements may be as high as 1.5A.

Currents listed are with no loading.

**Capacitance is periodically sampled rather than 100% tested.

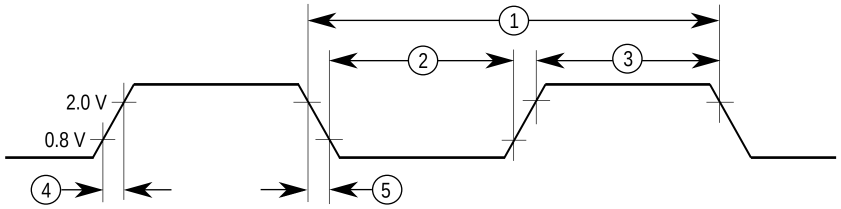
Freescale Semiconductor, Inc.

6.0 MC68SEC000 AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (See Figure 2)

Add the following table and Figure 8 to Section 10.9 on page 10-9.

			10MHz		16MHz		20MHz		
NUM.	CHARACTERISTIC	SYMBOL	MIN	MAX	min	max	min	max	UNIT
	Frequency of Operation	f	0	10.0	0	16.7	0	20.0	MHz
1	Cycle time	tcyc	100	—	60	—	50	—	ns
2,3	Clock Pulse Width	t_{CL} t_{CH}	45 45	— —	27 27	— —	21 21	— —	ns
4,5	Clock Rise and Fall Times	t_{Cr} t_{Cf}	— —	10 10	— —	5 5	— —	4 4	ns

Applies to 3.3V and 5V.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 V and 2.0 V.

Figure 8. MC68SEC000 Clock Input Timing Diagram

Freescale Semiconductor, Inc.

7.0 MC68SEC000 AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

Add the following table and Figures 9 and 10 to Section 10.16.

Applies to 3.3V and 5V.

(GND = 0 V; $T_A = T_L$ to T_H; see Figures 3 and 4)

NUM	CHARACTERISTIC	10MHz		16MHz		20MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
6	Clock Low to Address Valid	—	35	—	30	—	25	ns
6A	Clock High to FC Valid	0	35	0	30	0	25	ns
7	Clock High to Address, Data Bus High Impedance (Maximum) (Write)	—	55	—	50	—	42	ns
8	Clock High to Address, FC Invalid (Minimum)	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Asserted	3	35	3	30	3	25	ns
11[2]	Address Valid to $\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Asserted (Read)/ $\overline{\mathrm{AS}}$ Asserted (Write)	20	—	15	—	10	—	ns
11A[2]	FC Valid to $\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Asserted (Read)/ $\overline{\mathrm{AS}}$ Asserted (Write)	45	—	45	—	40	—	ns
12[1]	Clock Low to $\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Negated	3	35	3	30	3	25	ns
13[2]	$\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Negated to Address, FC Invalid	15	—	15	—	10	—	ns
14[2]	$\overline{\mathrm{AS}}$ (and $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Read) Width Asserted	195	—	120	—	100	—	ns
14A[2]	$\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Width Asserted (Write)	95	—	60	—	50	—	ns
15[2]	$\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Width Negated	105	—	60	—	50	—	ns
16	Clock High to Control Bus High Impedance	—	55	—	50	—	42	ns
17[2]	$\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Negated to R/$\overline{\mathrm{W}}$ Invalid	15	—	15	—	10	—	ns
18[1]	Clock High to R/$\overline{\mathrm{W}}$ High (Read)	0	35	0	30	0	25	ns
20[1]	Clock High to R/$\overline{\mathrm{W}}$ Low (Write)	0	35	0	30	0	25	ns
20A[2,6]	$\overline{\mathrm{AS}}$ Asserted to R/$\overline{\mathrm{W}}$ Low (Write)	—	10	—	10	—	10	ns
21[2]	Address Valid to R/$\overline{\mathrm{W}}$ Low (Write)	0	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{\mathrm{W}}$ Low (Write)	50	—	30	—	25	—	ns
22[2]	R/$\overline{\mathrm{W}}$ Low to $\overline{\mathrm{DS}}$ Asserted (Write)	50	—	30	—	25	—	ns
23	Clock Low to Data-Out Valid (Write)	—	35	—	30	—	25	ns
25[2]	$\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Negated to Data-Out Invalid (Write)	30	—	15	—	10	—	ns
26[2]	Data-Out Valid to $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Asserted (Write)	30	—	15	—	10	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time on Read)	5	—	5	—	5	—	ns
28[2]	$\overline{\mathrm{AS}}$, $\overline{\mathrm{LDS}}$, $\overline{\mathrm{UDS}}$ Negated to $\overline{\mathrm{DTACK}}$ Negated (Asynchronous Hold)	0	110	0	110	0	95	ns
28A	Clock High to $\overline{\mathrm{DTACK}}$ Negated	0	110	0	110	0	95	ns

For More Information On This Product,
Go to: www.freescale.com

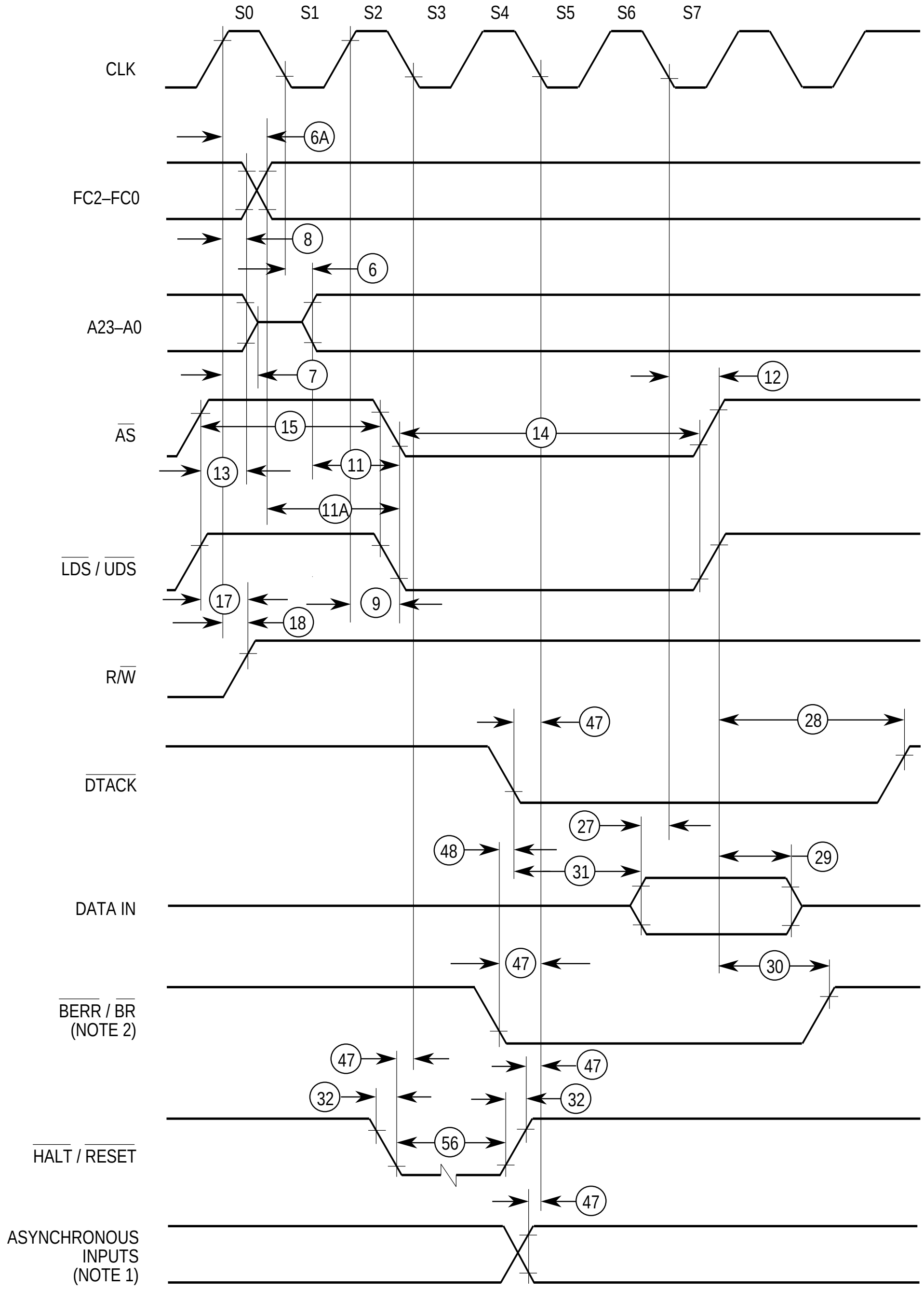
Freescale Semiconductor, Inc.

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Continued)

NUM	CHARACTERISTIC	10MHz		16MHz		20MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
29	$\overline{\text{AS}}$, $\overline{\text{LDS}}$, $\overline{\text{UDS}}$ Negated to Data-In Invalid (Hold Time on Read)	0	—	0	—	0	—	ns
29A	$\overline{\text{AS}}$, $\overline{\text{LDS}}$, $\overline{\text{UDS}}$ Negated to Data-In High Impedance (Read)	—	150	—	90	—	75	ns
30	$\overline{\text{AS}}$, $\overline{\text{LDS}}$, $\overline{\text{UDS}}$ Negated to $\overline{\text{BERR}}$ Negated	0	—	0	—	0	—	ns
31[2,5]	$\overline{\text{DTACK}}$ Asserted to Data-In Valid (Setup Time on Read)	—	65	—	50	—	42	ns
32	$\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ Input Transition Time	0	150	0	150	0	150	ns
33	Clock High to $\overline{\text{BG}}$ Asserted	—	35	—	30	—	25	ns
34	Clock High to $\overline{\text{BG}}$ Negated	—	35	—	30	—	25	ns
35	$\overline{\text{BR}}$ Asserted to $\overline{\text{BG}}$ Asserted	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[7]	$\overline{\text{BR}}$ Negated to $\overline{\text{BG}}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	Clks
38	$\overline{\text{BG}}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{\text{AS}}$ Negated)	—	55	—	50	—	42	ns
39	$\overline{\text{BG}}$ Width Negated	1.5	—	1.5	—	1.5	—	Clks
44	$\overline{\text{AS}}$, $\overline{\text{LDS}}$, $\overline{\text{UDS}}$ Negated to $\overline{\text{AVEC}}$ Negated	0	55	0	50	0	42	ns
47[5]	Asynchronous Input Setup Time	5	—	5	—	5	—	ns
48[2,3]	$\overline{\text{BERR}}$ Asserted to $\overline{\text{DTACK}}$ Asserted	20	—	10	—	10	—	ns
52	Data-In Hold from Clock High	0	—	0	—	0	—	ns
53	Data-Out Hold from Clock High (Write)	0	—	0	—	0	—	ns
55	R/$\overline{\text{W}}$ Asserted to Data Bus Impedance Change (Write)	20	—	10	—	0	—	ns
56[4]	$\overline{\text{HALT}}$, $\overline{\text{RESET}}$ Pulse Width	10	—	10	—	10	—	Clks
58[7]	$\overline{\text{BR}}$ Negated to $\overline{\text{AS}}$, $\overline{\text{LDS}}$, $\overline{\text{UDS}}$, R/$\overline{\text{W}}$ Driven	1.5	—	1.5	—	1.5	—	Clks
58A[7]	$\overline{\text{BR}}$ Negated to FC Driven	1	—	1	—	1	—	Clks

Applies to 3.3V and 5V.

NOTES:
1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$, #48 may be ignored. In the absence of $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$ is an asynchronous input using the asynchronous input setup time (#47).
4. For power-up, the MC68SEC000 must be held in the reset state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the controller.
5. If the asynchronous input setup time (#47) requirement is satisfied for $\overline{\text{DTACK}}$, the $\overline{\text{DTACK}}$ asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{\text{AS}}$ and R/$\overline{\text{W}}$ are equally loaded (±20%), subtract 5 ns from the values given in these columns.
7. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{\text{BG}}$ may be reasserted.

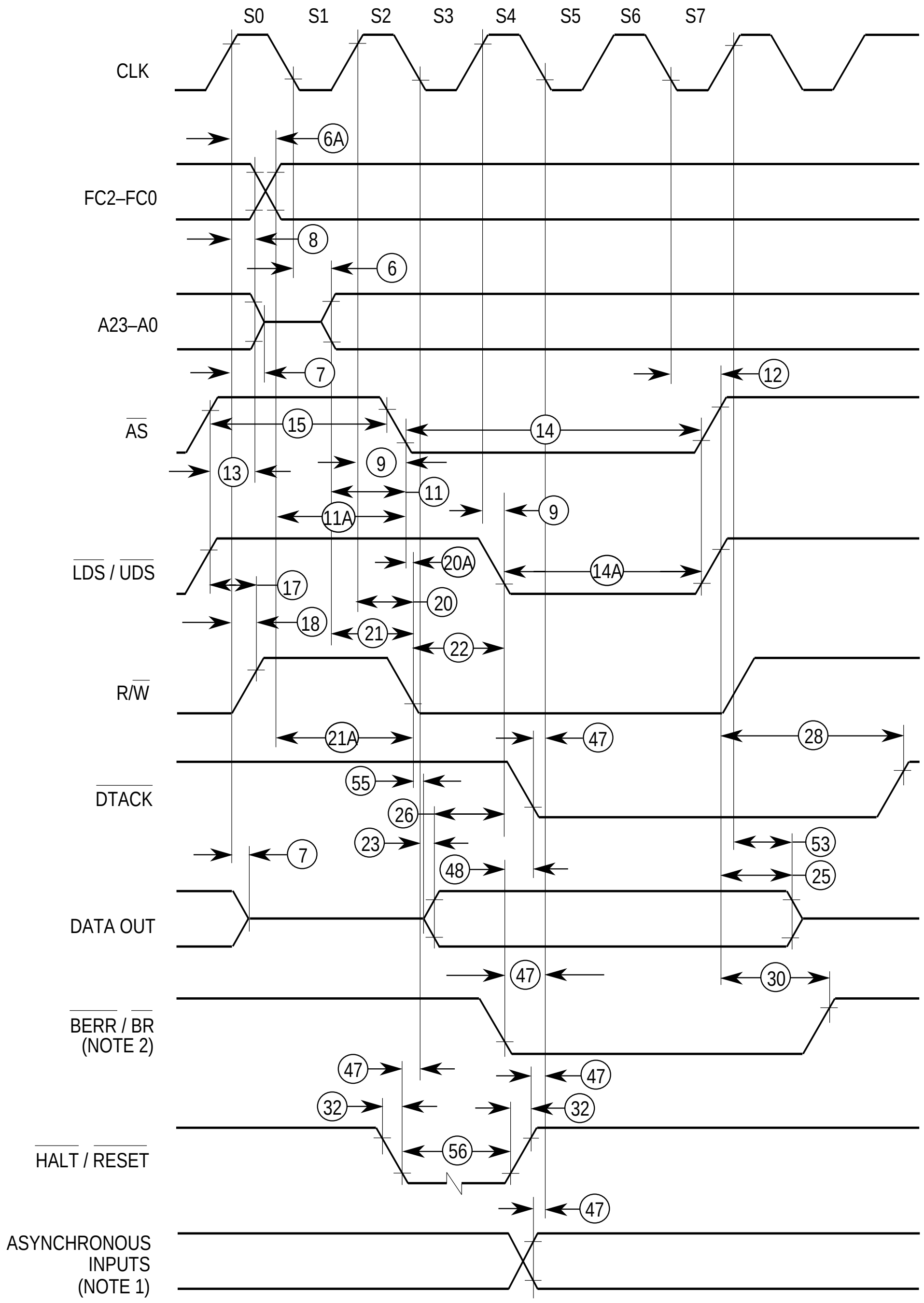


NOTES:
1. Setup time for the asynchronous inputs IPL2–IPL0 and AVEC (#47) guarantees their recognition at the next falling edge of the clock.
2. BR need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

Figure 9. MC68SEC000 Read Cycle Timing Diagram

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com



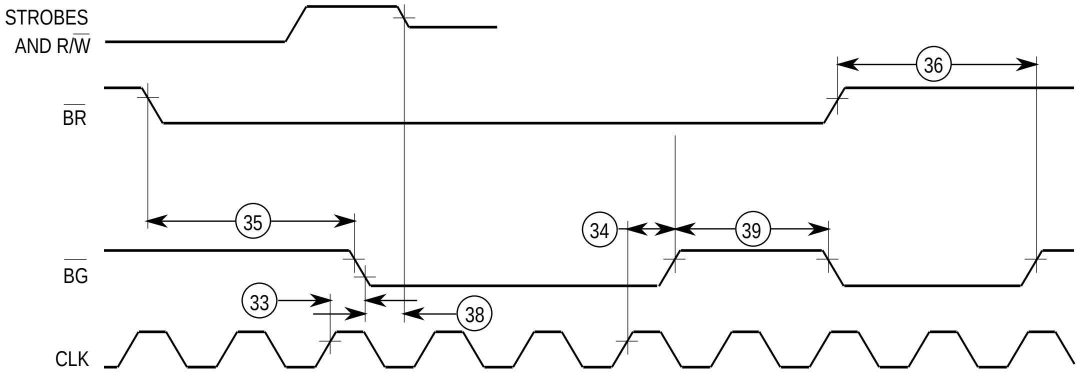
NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/W may be valid after AS even though both are initiated by the rising edge of S2 (specification #20A).

Figure 10. MC68SEC000 Write Cycle Timing Diagram

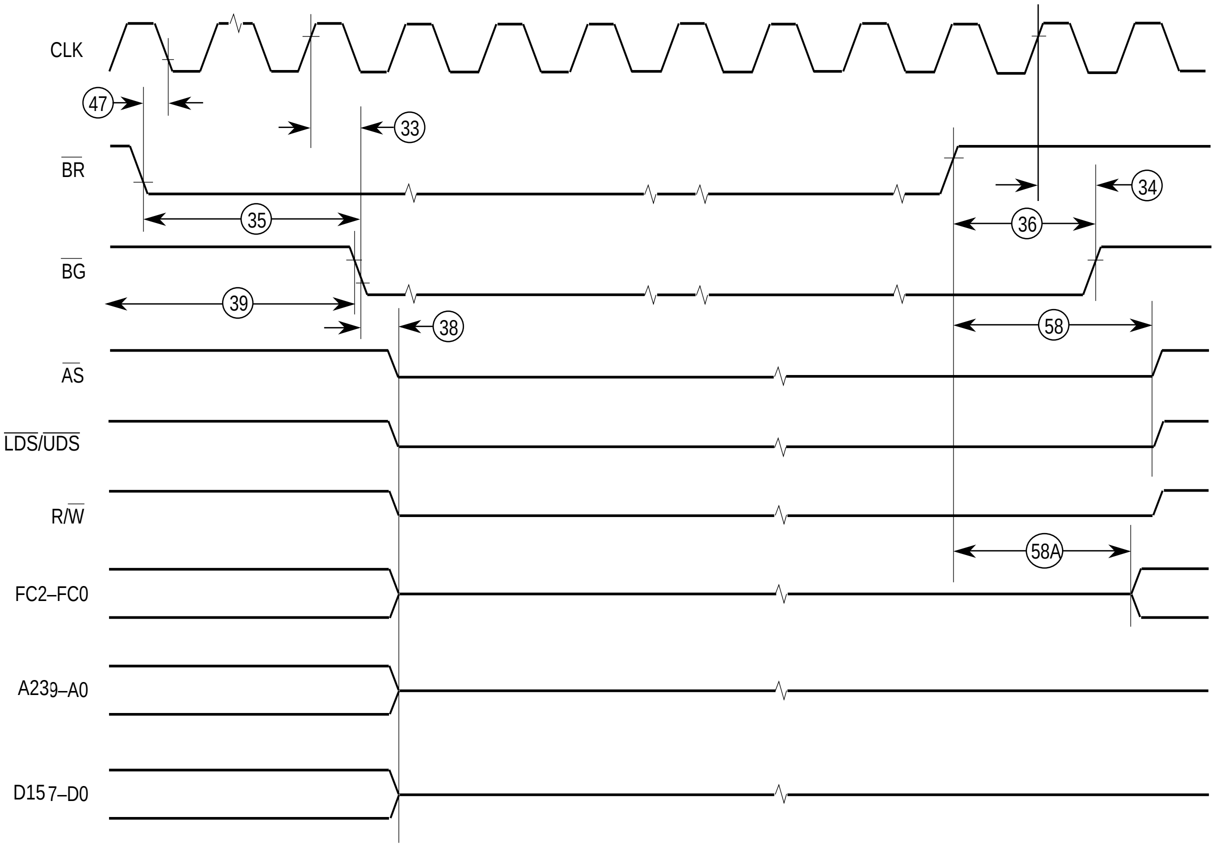
Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.



NOTE: Setup time to the clock (#47) for the asynchronous inputs $\overline{\text{BERR}}$, $\overline{\text{BR}}$, $\overline{\text{DTACK}}$, $\overline{\text{IPL2-IPL0}}$, and $\overline{\text{VPA}}$ guarantees their recognition at the next falling edge of the clock.

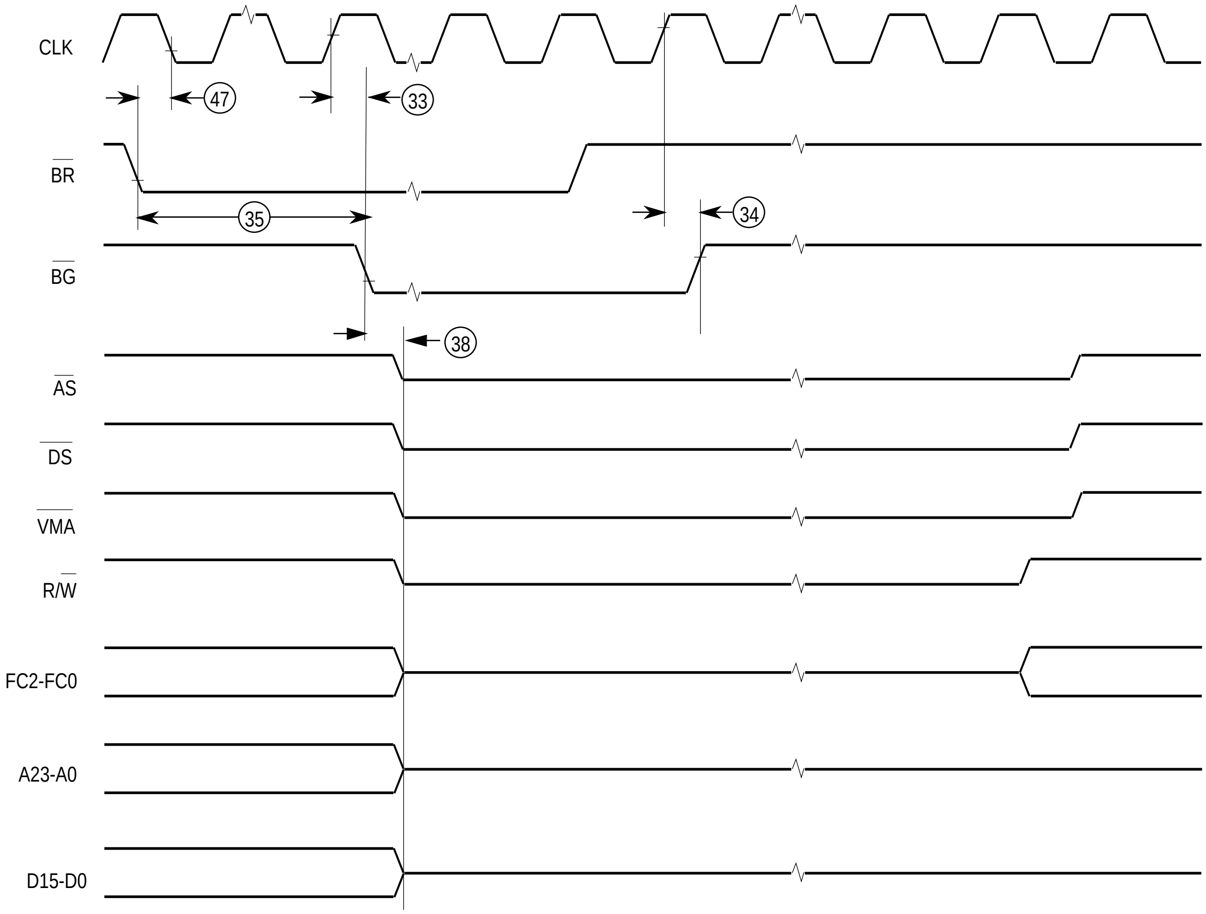
Figure 11. Bus Arbitration Timing



NOTE: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

Figure 12. MC68SEC000 Bus Arbitration Timing Diagram

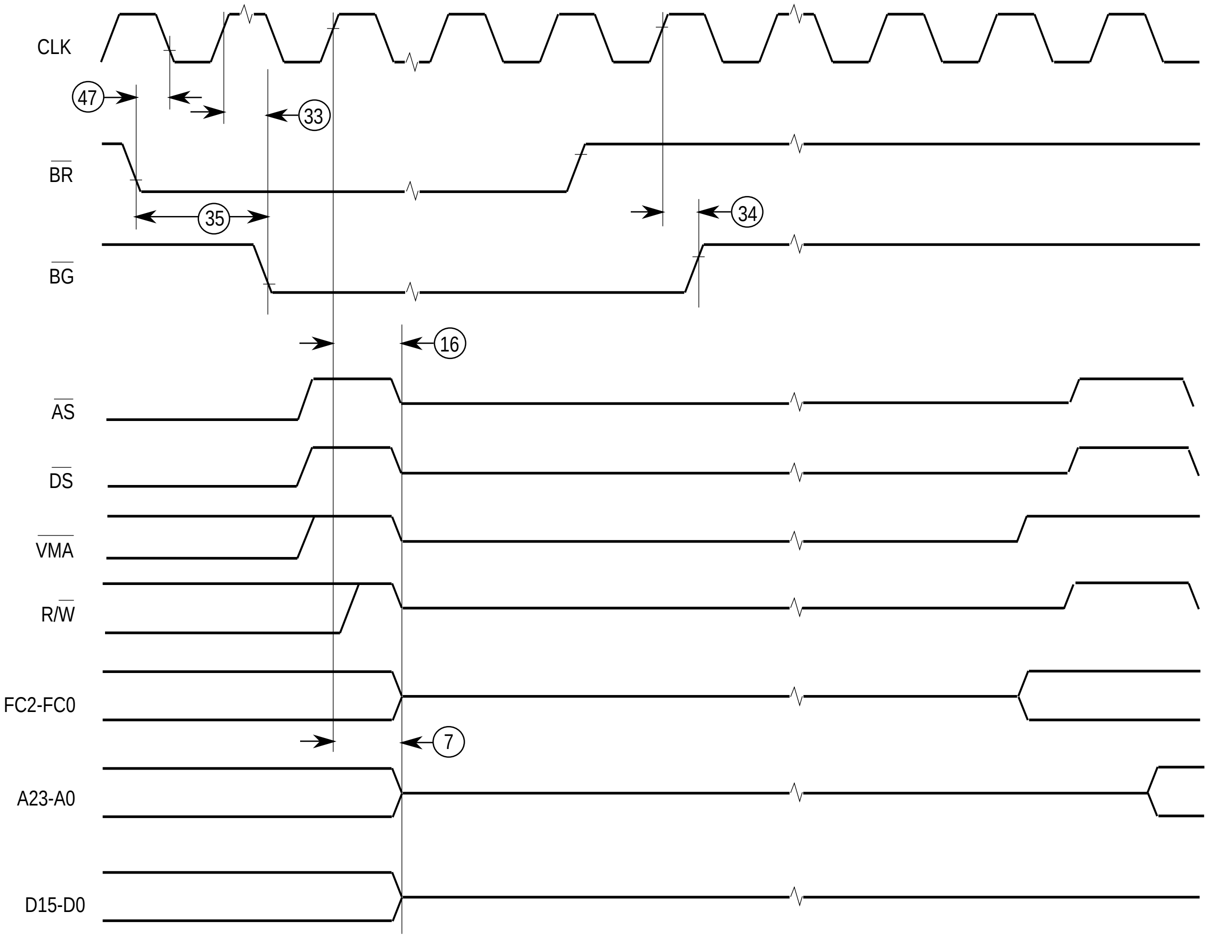
Freescale Semiconductor, Inc.



NOTES: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V. This diagram also applies to the 68EC000.

Figure 13. Bus Arbitration Timing—Idle Bus Case

For More Information On This Product,
Go to: www.freescale.com



NOTE: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.
This diagram also applies to the 68EC000.

Figure 14. Bus Arbitration Timing - Active Bus Case

Freescale Semiconductor, Inc.

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

9.0 MECHANICAL DATA

9.1 PIN ASSIGNMENTS

Add Figure 12 to Section 11.1.

The following defines the pin assignment and the package dimensions of the 64 lead QFP (FU package) and 64 lead TQFP (PB package) for the MC68SEC000. Note that it is pin-to-pin compatible with the MC68EC000.

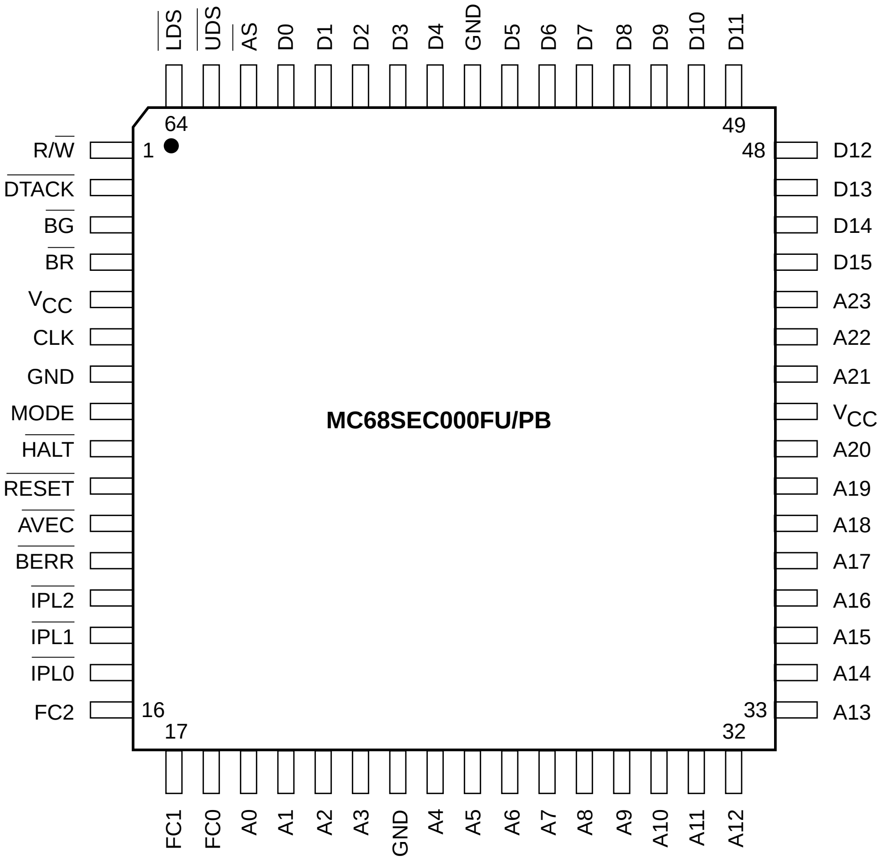


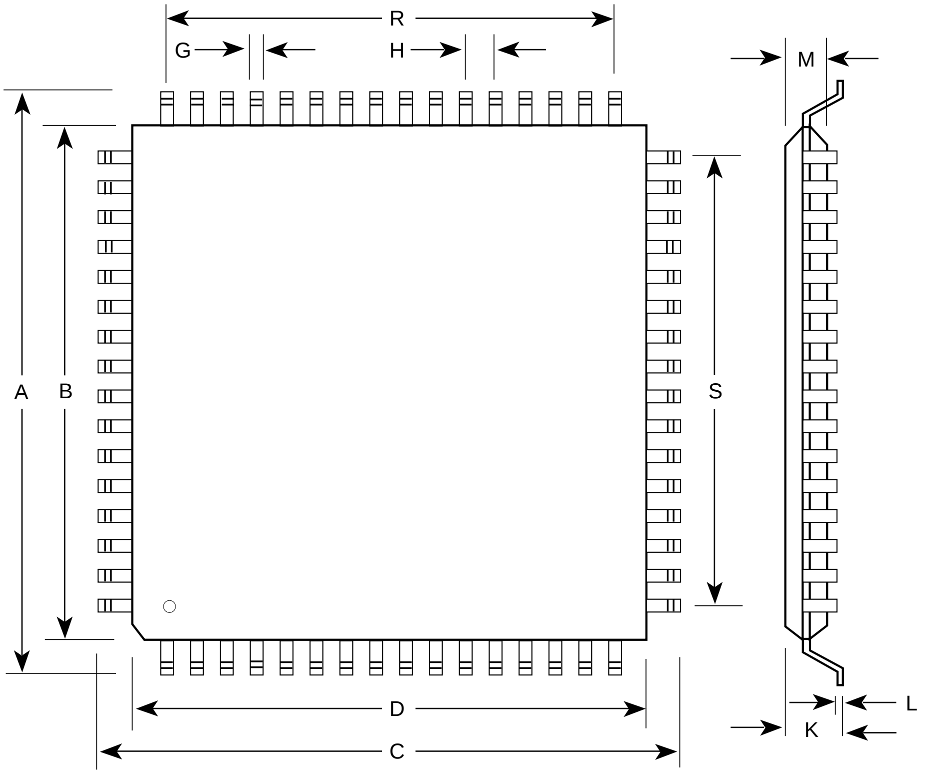
Figure 16. 64-Lead Quad Flat Pack and 64-Lead Thin Quad Flat Pack

Freescale Semiconductor, Inc.

10.0 PACKAGE DIMENSIONS - FU SUFFIX

This diagram replaces the one on Page 11-16

64 Lead Quad Flat Pack Case 840B-01

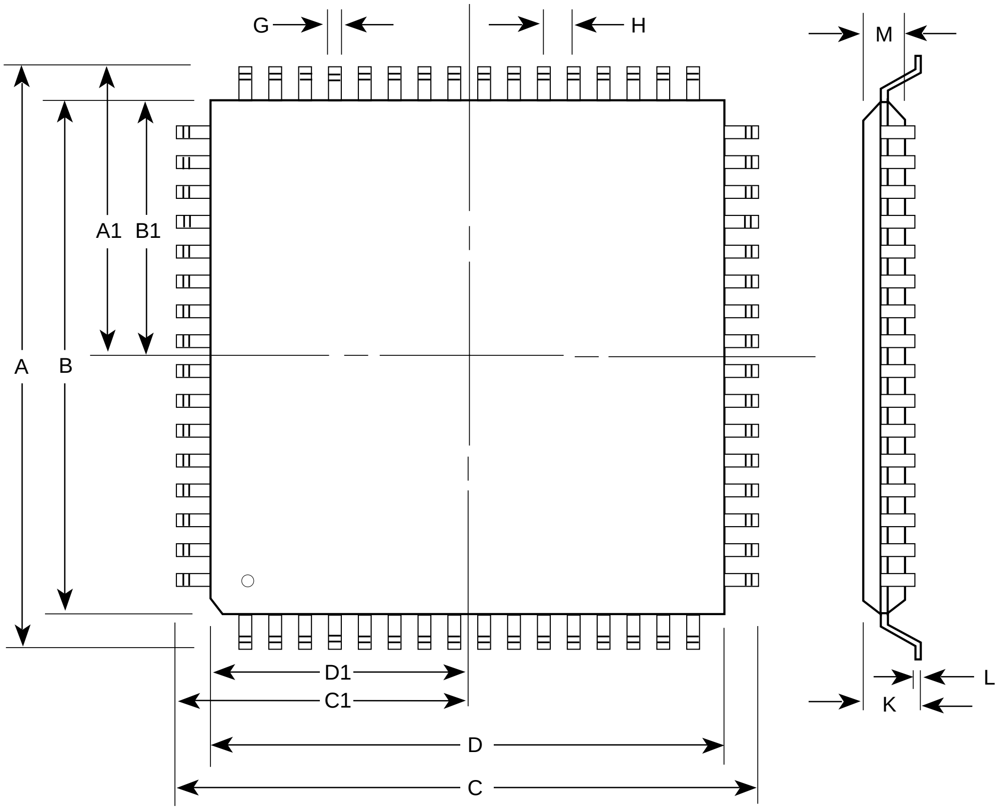


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.95	17.45	0.667	0.687
B	13.90	14.10	0.547	0.555
C	16.95	17.45	0.667	0.687
D	13.90	14.10	0.547	0.555
G	0.30	0.45	0.012	0.018
H	0.80 BSC		0.031 BSC	
K	2.15	2.45	0.085	0.096
L	0.13	0.23	0.005	0.009
M	2.00	2.40	0.79	0.094
R	12.00 REF		0.472 REF	
S	12.00 REF		0.472 REF	

11.0 PACKAGE DIMENSIONS - PB SUFFIX

Add the following to Section 11.2.

64 Lead Thin Quad Flat Pack Case 840F-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
A1	6.00 BSC		0.236 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	12.00 BSC		0.472 BSC	
C1	6.00 BSC		0.236 BSC	
D	10.00 BSC		0.394 BSC	
D1	5.00 BSC		0.197 BSC	
G	0.17	0.27	0.007	0.011
H	0.50 BSC		0.020 BSC	
K	---	1.60	---	0.063
L	0.09	0.20	0.004	0.008
M	1.35	1.45	0.053	0.057

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

12.0 PACKAGE/FREQUENCY AVAILABILITY

Replaces Section 11.1

The following tables identify the packages and operating frequencies available for the MC68HC000, MC68HC001, MC68EC000, and the MC68SEC000.

MC68SEC000 PACKAGE	FREQUENCY	VOLTAGE	
		3.3 V	5 V
Quad Flat Pack (FU)	10 MHz 16 MHz 20MHz	✓ ✓ ✓	✓ ✓ ✓
Thin Quad Flat Pack (PB)	10 MHz 16 MHz 20MHz	✓ ✓ ✓	✓ ✓ ✓

MC68HC000 PACKAGE	FREQUENCY	VOLTAGE 5V
Plastic DIP Plastic Quad Pack (PLCC) Plastic Quad (Gull Wing)** Pin Grid Array, Solder Lead Finish** Pin Grid Array, Gold Lead Finish**	8,10,12,16,20 MHz	3
	8,10,12,16,20 MHz	3
	8,10,12,16,20 MHz	3
	8,10,12,16,20 MHz	3
Plastic Quad Pack (PLCC)	8,10,12,16,20 MHz	3

MC68HC001** PACKAGE	FREQUENCY	VOLTAGE 5V
Plastic Quad Pack (PLCC) Plastic Quad (Gull Wing) Pin Grid Array, Gold Lead Finish	8,10,12,16 MHz	✓
	8,10,12,16 MHz	✓
	8,10,12,16 MHz	✓
	8,10,12,16 MHz	✓

MC68EC000 PACKAGE	FREQUENCY	VOLTAGE 5V
Plastic Quad Pack (PLCC) Plastic Quad Flat Pack	8 MHz	✓
	10 MHz	✓
	12 MHz	✓
	16 MHz	✓
	20 MHz	✓

NOTE : ** not recommended for new designs

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

ORDERING INFORMATION

Add the following to Section 11.

The following tables contains the ordering information for the MC68SEC000.

MC68SEC000 Ordering Information

PACKAGE	BODY SIZE	LEAD SPACING	SPEED (IN MH Z)	VOLTAGE	SUFFIX	TEMPERATURE RANGE
QFP	14.0 mm X 14.0mm	0.8mm	10/16/20 MHz	3.3V or 5.0V	FU	0C to +70C
					CFU	-40C to +85C
TQFP	10.0mm x 10.0mm	0.5mm			PB	0C to +70C
					CPB	-40C to +85C

MC68HC000 Ordering Information

PACKAGE	BODY SIZE	LEAD SPACING	SPEED (IN MHZ)	VOLTAGE	SUFFIX	TEMPERATURE RANGE
DIP	81.91mm X 20.57mm	2.54mm	8, 10, 12, 16	5.0V	P	0C to +70C
PLCC	25.57mm X 25.27mm	1.27mm	8, 10, 12, 16, 20		FN	0C to +70C
			8, 10, 12, 16		CFN	-40C to +85C

MC68EC000 Ordering Information

PACKAGE	BODY SIZE	LEAD SPACING	SPEED (IN MHZ)	VOLTAGE	SUFFIX	TEMPERATURE RANGE
PLCC	25.57mm X 25.27mm	1.27mm	8, 10,12, 16, 20	5.0V	FN	0C to +70C
PQFP	14.1mm X 14.1mm	0.8mm	8, 10,12, 16, 20		FU	

DOCUMENTATION

Add to Section 11.

The documents listed in the following table contain detailed information that pertain to the MC68SEC000 processor. You can obtain these documents from the Literature Distribution Centers listed on the last page of this document.

MC68SEC000 Documentation

MC68SEC000 DOCUMENTATION	DOCUMENT NUMBER
M68000 Family Programmer’s Reference Manual	M68000PM/AD
M68000 User’s Manual	M68000UM/AD
High Performance Embedded Systems Source Catalog“	BR729/D
MC68EC000 Product Brief	MC68EC000/D
MC68SEC000 Product Brief	MC68SEC000/D

Freescale Semiconductor, Inc.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong.

SEMICONDUCTOR PRODUCT INFORMATION