Renesas Electronics America Inc - R5F2136CWKFP#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136cwkfp-u0

Table 1.8 Specifications for R8C/36Z Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEBus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
A/D Converter		10-bit resolution × 16 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

Table 1.11 Product List for R8C/36Y Group **Current of Nov 2010**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21368YJFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	J version
R5F2136AYJFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2136CYJFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F21368YKFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	K version
R5F2136AYKFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2136CYKFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	

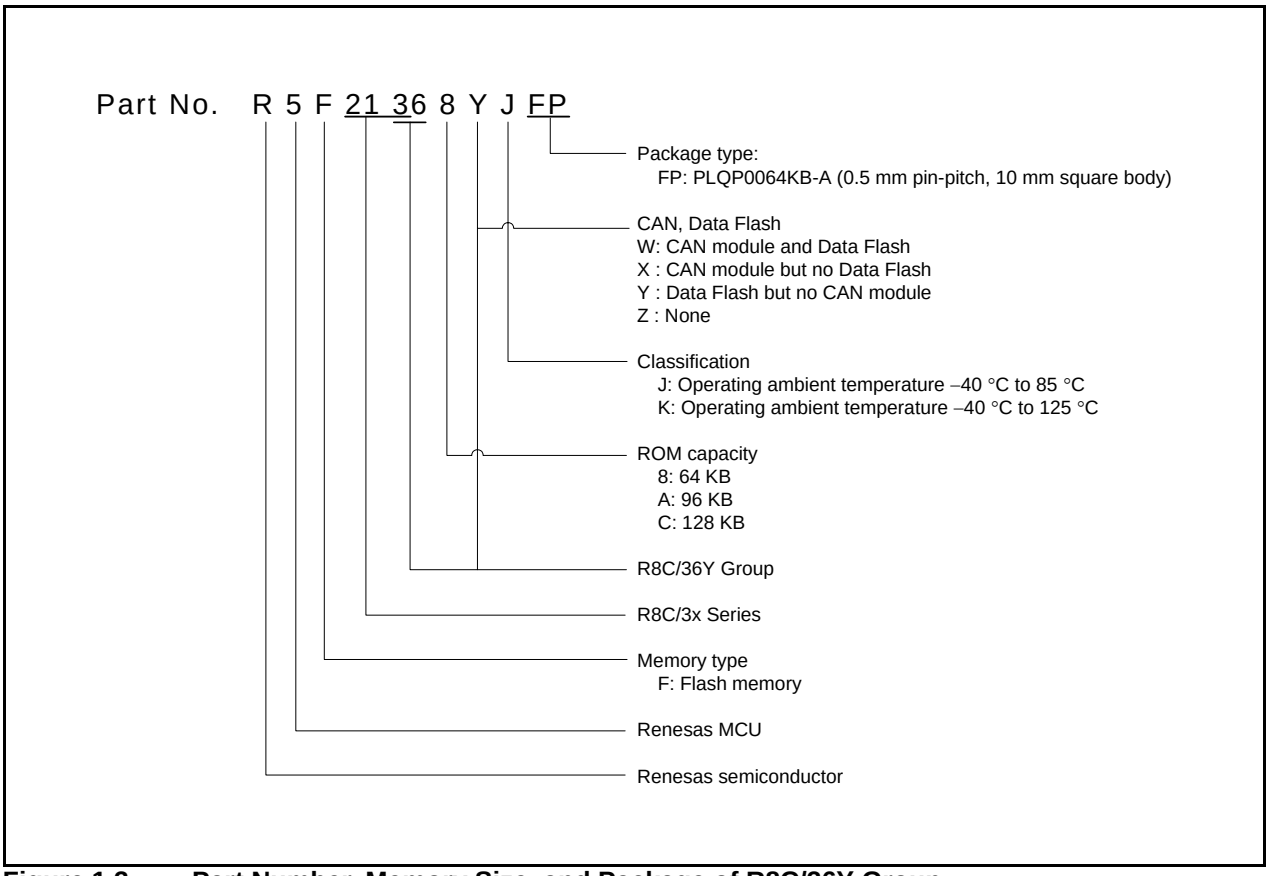
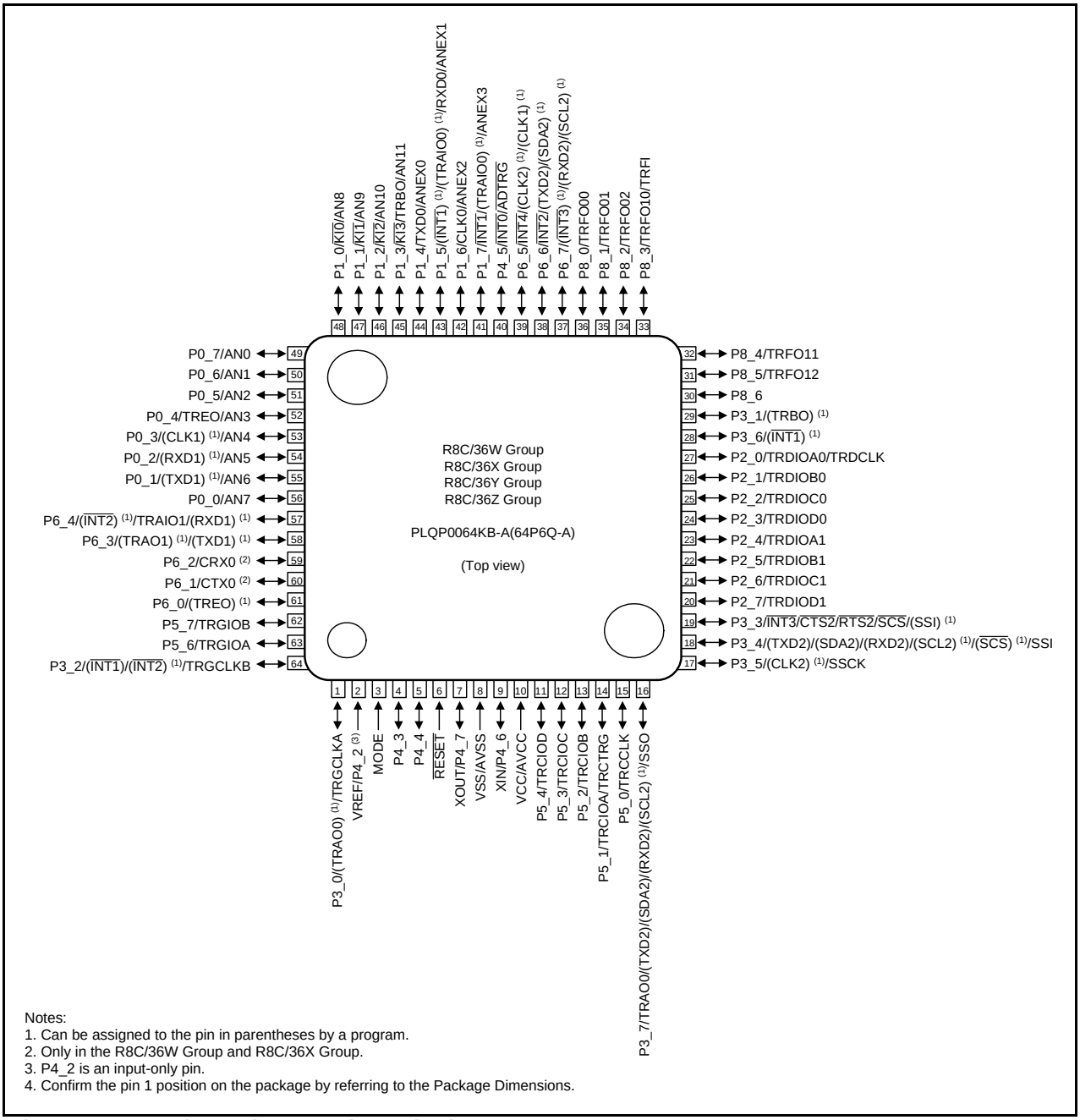


Figure 1.3 Part Number, Memory Size, and Package of R8C/36Y Group

1.4 Pin Assignment

Figure 1.6 shows Pin Assignment (Top View). Tables 1.13 and 1.14 outline the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Only in the R8C/36W Group and R8C/36X Group.
3. P4_2 is an input-only pin.
4. Confirm the pin 1 position on the package by referring to the Package Dimensions.

Figure 1.6 Pin Assignment (Top View)

Table 1.16 Pin Functions (2)

Item	Pin Name	I/O Type	Description
CAN module	CRX0 (1)	I	CAN data input pin
	CTX0 (1)	O	CAN data output pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11 ANEX0 to ANEX3	I	Analog input pins to A/D converter
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

Note:

1. Only in the R8C/36W Group and R8C/36X Group.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

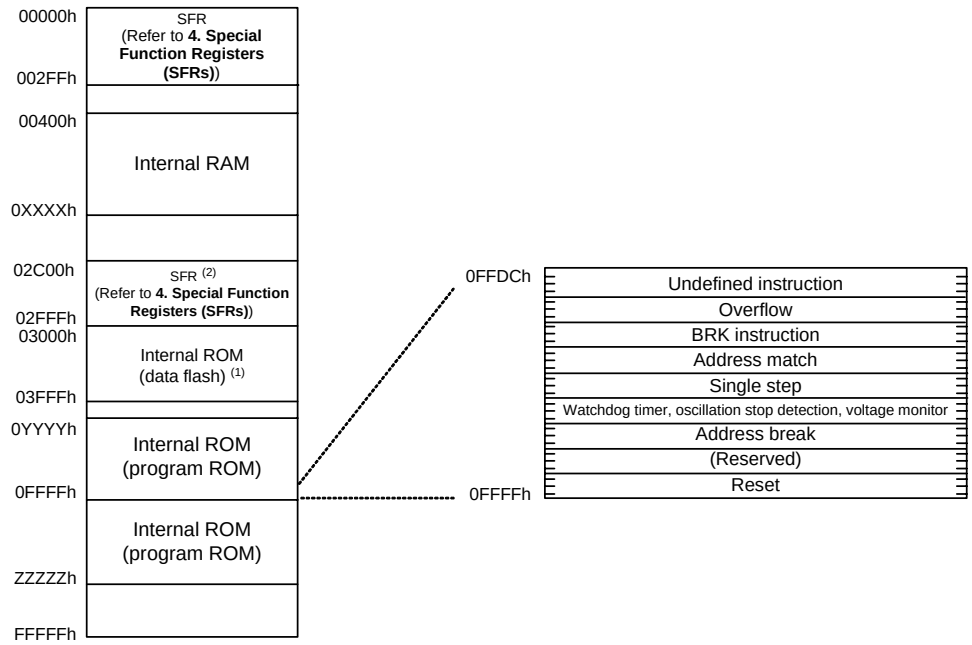
2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3. Memory

3.1 R8C/36W Group

Figure 3.1 is a Memory Map of R8C/36W Group. The R8C/36W Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



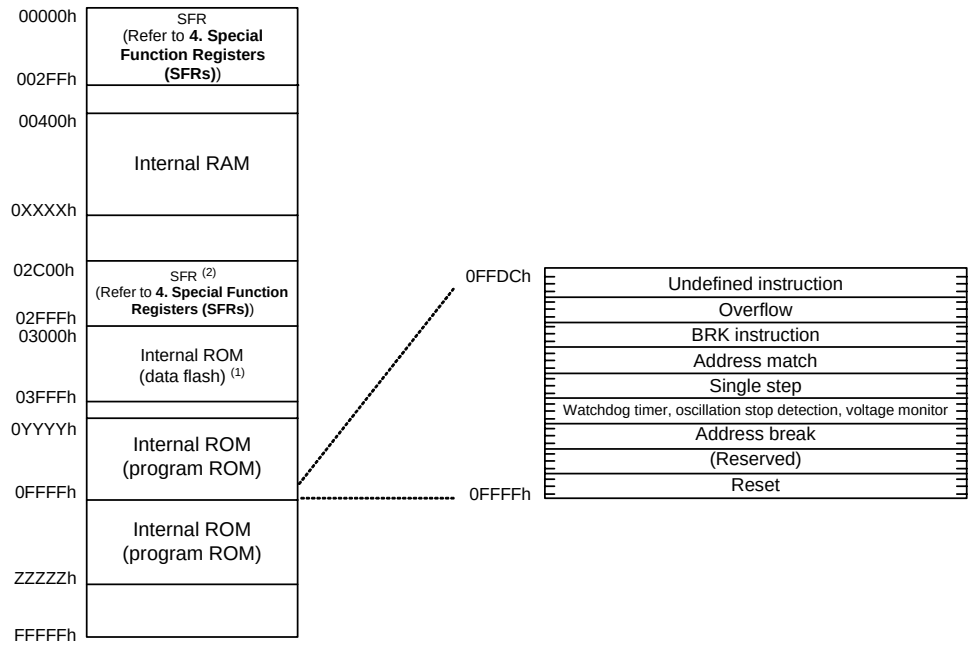
Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21368WJFP, R5F21368WKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136AWJFP, R5F2136AWKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CWJFP, R5F2136CWKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map of R8C/36W Group

3.3 R8C/36Y Group

Figure 3.3 is a Memory Map of R8C/36Y Group. The R8C/36Y Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



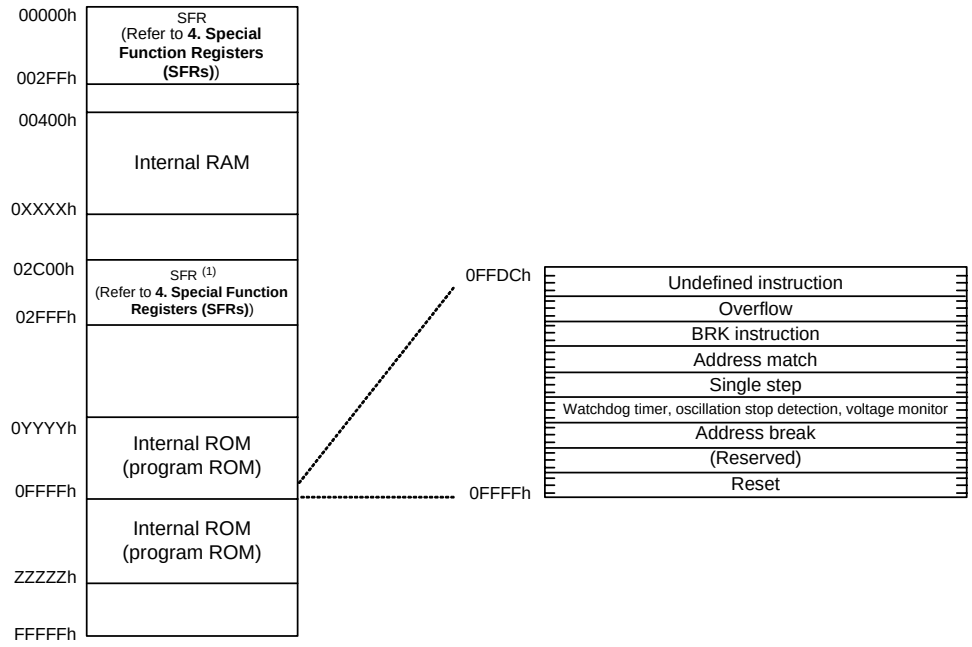
Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21368YJFP, R5F21368YKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136AYJFP, R5F2136AYKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CYJFP, R5F2136CYKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.3 Memory Map of R8C/36Y Group

3.4 R8C/36Z Group

Figure 3.4 is a Memory Map of R8C/36Z Group. The R8C/36Z Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21368ZJFP, R5F21368ZKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136AZJFP, R5F2136AZKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CZJFP, R5F2136CZKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.4 Memory Map of R8C/36Z Group

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh			00h
009Eh	Compare 1 Register	TRFM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After reset
0100h	Timer RA0 Control Register	TRA0CR	00h
0101h	Timer RA0 I/O Control Register	TRA0IOC	00h
0102h	Timer RA0 Mode Register	TRA0MR	00h
0103h	Timer RA0 Prescaler Register	TRA0PRE	FFh
0104h	Timer RA0 Register	TRA0	FFh
0105h	LIN0 Control Register 2	LIN0CR2	00h
0106h	LIN0 Control Register	LIN0CR	00h
0107h	LIN0 Status Register	LIN0ST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h	Timer RA1 Control Register	TRA1CR	00h
0111h	Timer RA1 I/O Control Register	TRA1IOC	00h
0112h	Timer RA1 Mode Register	TRA1MR	00h
0113h	Timer RA1 Prescaler Register	TRA1PRE	FFh
0114h	Timer RA1 Register	TRA1	FFh
0115h	LIN1 Control Register 2	LIN1CR2	00h
0116h	LIN1 Control Register	LIN1CR	00h
0117h	LIN1 Status Register	LIN1ST	00h
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After reset
2E70h	CAN0 Mailbox 7: Message ID	C0MB7	XXh
2E71h			XXh
2E72h			XXh
2E73h			XXh
2E74h			
2E75h	CAN0 Mailbox 7: Data length		XXh
2E76h	CAN0 Mailbox 7: Data field		XXh
2E77h			XXh
2E78h			XXh
2E79h			XXh
2E7Ah			XXh
2E7Bh			XXh
2E7Ch			XXh
2E7Dh			XXh
2E7Eh	CAN0 Mailbox 7: Time stamp		XXh
2E7Fh			XXh
2E80h	CAN0 Mailbox 8: Message ID	C0MB8	XXh
2E81h			XXh
2E82h			XXh
2E83h			XXh
2E84h			
2E85h	CAN0 Mailbox 8: Data length		XXh
2E86h	CAN0 Mailbox 8: Data field		XXh
2E87h			XXh
2E88h			XXh
2E89h			XXh
2E8Ah			XXh
2E8Bh			XXh
2E8Ch			XXh
2E8Dh			XXh
2E8Eh	CAN0 Mailbox 8: Time stamp		XXh
2E8Fh			XXh
2E90h	CAN0 Mailbox 9: Message ID	C0MB9	XXh
2E91h			XXh
2E92h			XXh
2E93h			XXh
2E94h			
2E95h	CAN0 Mailbox 9: Data length		XXh
2E96h	CAN0 Mailbox 9: Data field		XXh
2E97h			XXh
2E98h			XXh
2E99h			XXh
2E9Ah			XXh
2E9Bh			XXh
2E9Ch			XXh
2E9Dh			XXh
2E9Eh	CAN0 Mailbox 9: Time stamp		XXh
2E9Fh			XXh
2EA0h	CAN0 Mailbox 10: Message ID	C0MB10	XXh
2EA1h			XXh
2EA2h			XXh
2EA3h			XXh
2EA4h			
2EA5h	CAN0 Mailbox 10: Data length		XXh
2EA6h	CAN0 Mailbox 10: Data field		XXh
2EA7h			XXh
2EA8h			XXh
2EA9h			XXh
2EAAh			XXh
2EABh			XXh
2EACh			XXh
2EADh			XXh
2EAEh	CAN0 Mailbox 10: Time stamp		XXh
2EAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					2.7	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage					–	0	–	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	–	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	–	V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	–	V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	–	V_{CC}	V
		External clock input (XOUT)				1.2	–	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	–	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.3 V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.45 V_{CC}	V
		External clock input (XOUT)				0	–	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				–	–	–80	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				–	–	–40	mA
$I_{OH(peak)}$	Peak output “H” current					–	–	–10	mA
$I_{OH(avg)}$	Average output “H” current					–	–	–5	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				–	–	80	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				–	–	40	mA
$I_{OL(peak)}$	Peak output “L” current					–	–	10	mA
$I_{OL(avg)}$	Average output “L” current					–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
fOCO40M	Count source for timer RC, timer RD, or timer RG				2.7 V ≤ V_{CC} ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
–	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.4 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input ANEX0 to ANEX3 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input ANEX0 to ANEX3 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input ANEX0 to ANEX3 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input ANEX0 to ANEX3 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	20	MHz
			2.7 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	10	MHz
–	Tolerance level impedance				–	3	–	kΩ
I_{vref}	V_{ref} current		V_{CC} = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
V_{ref}	Reference voltage				2.7	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.14	1.34	1.54	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (2)		10,000 (3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	160	950	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	300	950	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	1	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	3+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	µs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		–40	–	85 (J version) 125 (K version)	°C
–	Data hold time (7)	Ambient temperature = 55 °C (8)	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000, 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.
8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.

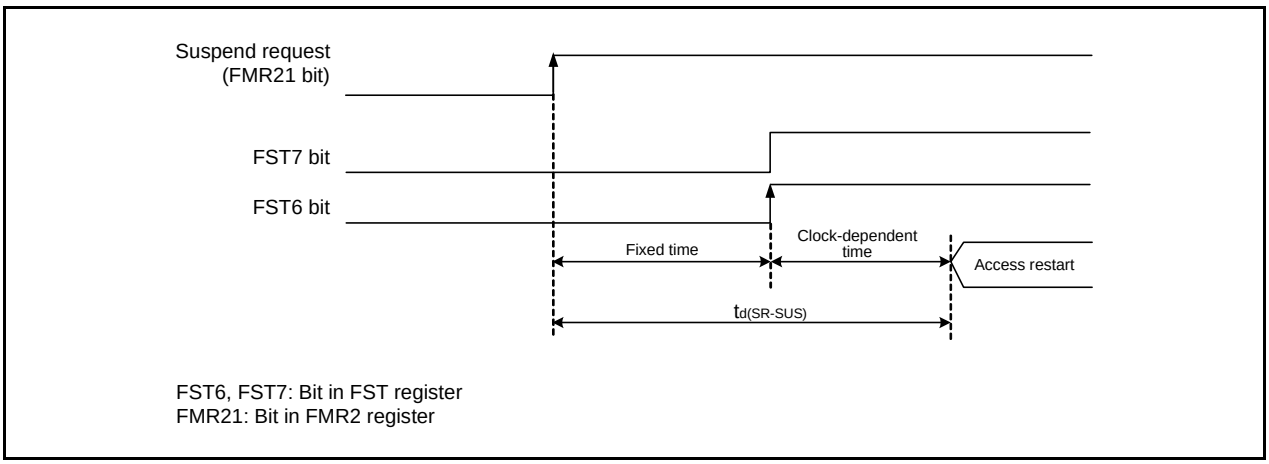
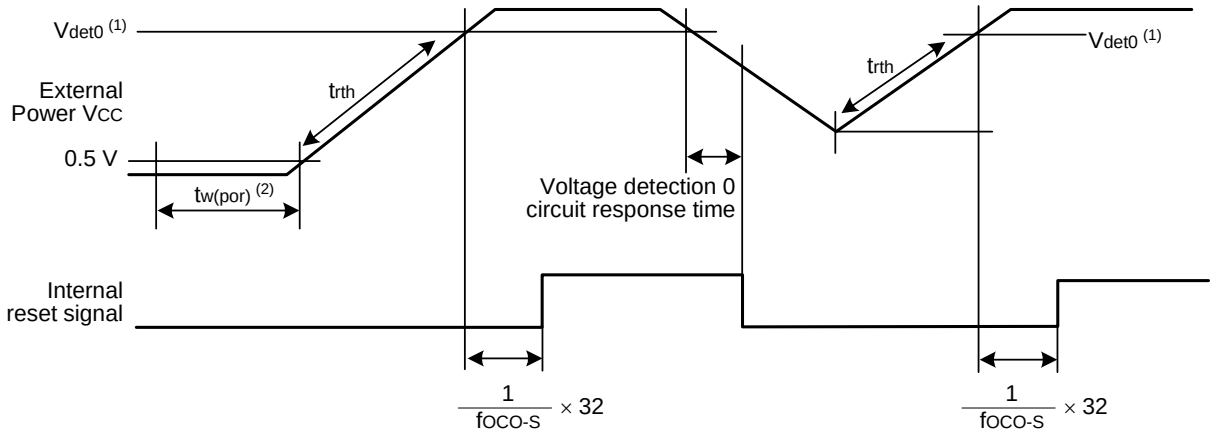


Figure 5.2 Time delay until Suspend

Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	–	50000	mV/msec

Notes:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware (R01UH0064EJ) for details.
2. tw(por) indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.15 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA	V_{CC} – 0.3	–	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	I_{OL} = 5 mA	–	–	2.0	V
			I_{OL} = 200 μA	–	–	0.45	V
		XOUT	I_{OH} = –200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO0, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, $\overline{TRGCLKB}$, TRCTRG, $\overline{ADTRG}$, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO		0.1	1.2	–	V
		$\overline{RESET}$		0.1	1.2	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5.0 V	–	–	1.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V	–	–	–1.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V	25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN		–	0.3	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

Note:
1. 4.2 V ≤ Vcc ≤ 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.23 Electrical Characteristics (4) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO0, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, TRGCLKB, TRCTRG, $\overline{ADTRG}$, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO		0.1	0.4	–	V
		$\overline{RESET}$		0.1	0.5	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3.0 V	–	–	1.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3.0 V	–	–	–1.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3.0 V	42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN		–	0.3	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

Note:
1. 2.7 V ≤ Vcc < 4.2 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.25 Electrical Characteristics (6) [2.7 V ≤ Vcc < 3.3 V] (Topr = −40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	85	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	320	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	310	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	55.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Timing requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = –40°C to 85°C (J ver)/–40°C to 125°C (K ver))

Table 5.26 External clock input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns

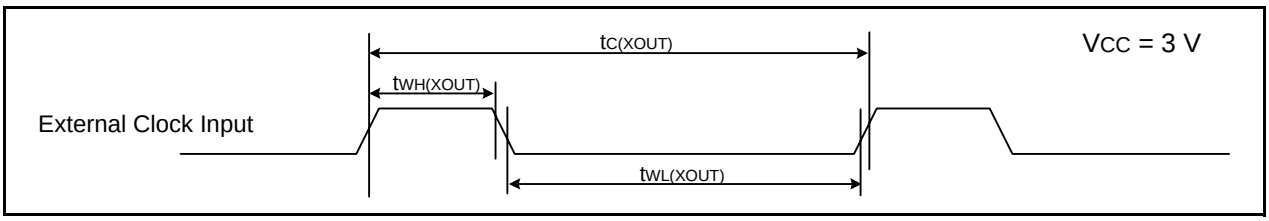


Figure 5.12 External Clock Input Timing Diagram when Vcc = 3 V

Table 5.27 TRAIOi (i = 0 to 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIOi (i = 0 to 1) input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIOi (i = 0 to 1) input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIOi (i = 0 to 1) input “L” width	120	–	ns

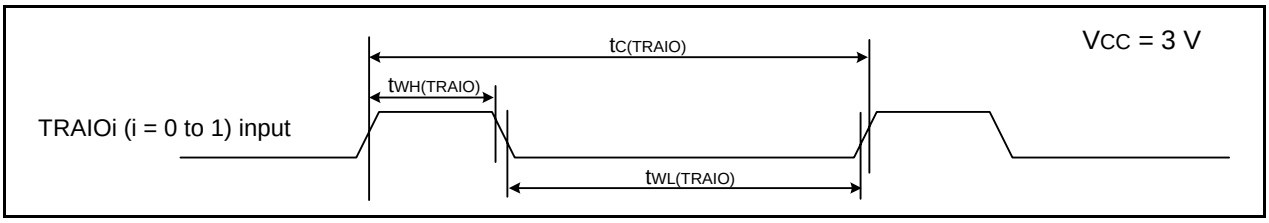


Figure 5.13 TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 3 V

Table 5.28 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400 (1)	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	200 (2)	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	200 (2)	–	ns

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

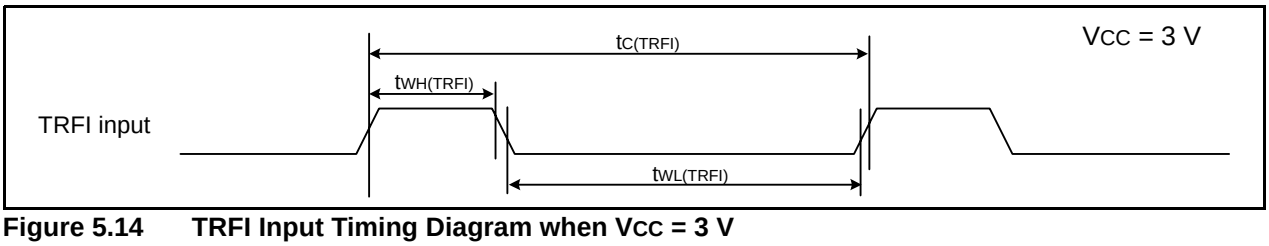


Figure 5.14 TRFI Input Timing Diagram when Vcc = 3 V

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