# Renesas Electronics America Inc - R5F2136CWKFP#W4 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | CANbus, I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 59 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136cwkfp-w4 |

**Table 1.2 Specifications for R8C/36W Group (2)**

| Item | Function | Specification |
|---|---|---|
| Timer | Timer RA0 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RA1 | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits (with 8-bit prescaler) × 1<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits (with 4 capture/compare registers) × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits (with 4 capture/compare registers) × 2<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
| | Timer RE | 8 bits × 1<br>Output compare mode |
| | Timer RF | 16 bits × 1<br>Input capture mode (input capture circuit), output compare mode (output compare circuit) |
| | Timer RG | 16 bits × 1<br>Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder) |
| Serial Interface | UART0, 1 | 2 channels<br>Clock synchronous serial I/O, UART |
| | UART2 | 1 channel<br>Clock synchronous serial I/O, UART, $I^2C$ mode ($I^2C$-bus), IE mode (IEBus), multiprocessor communication function |
| Synchronous Serial Communication Unit (SSU) | | 1 channel |
| LIN Module | | Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1) |
| CAN Module | | 1 channel, 16 Mailboxes (conforms to the ISO 11898-1) |
| A/D Converter | | 10-bit resolution × 16 channels, includes sample and hold function, with sweep mode |
| Flash Memory | | • Programming and erasure voltage: VCC = 2.7 to 5.5 V<br>• Programming and erasure endurance: 10,000 times (data flash)<br>1,000 times (program ROM)<br>• Program security: ROM code protect, ID code check<br>• Debug functions: On-chip debug, on-board flash rewrite function<br>• Background operation (BGO) function (data flash) |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) |
| Current Consumption | | Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) |
| Operating Ambient Temperature | | -40 to 85°C (J version)<br>-40 to 125°C (K version) (1) |
| Package | | 64-pin LQFP<br>Package code: PLQP0064KB-A (previous code: 64P6Q-A) |

Note:
1. Specify the K version if K version functions are to be used.

**Table 1.5 Specifications for R8C/36Y Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operating mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.11 Product List for R8C/36Y Group**. |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 59, selectable pull-up resistor |
| Clock | Clock generation circuits | 3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),<br>High-speed on-chip oscillator (with frequency adjustment function),<br>Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| Interrupts | | • Interrupt vectors: 69<br>• External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 40<br>• Transfer modes: 2 (normal mode, repeat mode) |

**Table 1.11 Product List for R8C/36Y Group** **Current of Nov 2010**

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data flash | | | |
| R5F21368YJFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0064KB-A | J version |
| R5F2136AYJFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0064KB-A | |
| R5F2136CYJFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0064KB-A | |
| R5F21368YKFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0064KB-A | K version |
| R5F2136AYKFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0064KB-A | |
| R5F2136CYKFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0064KB-A | |

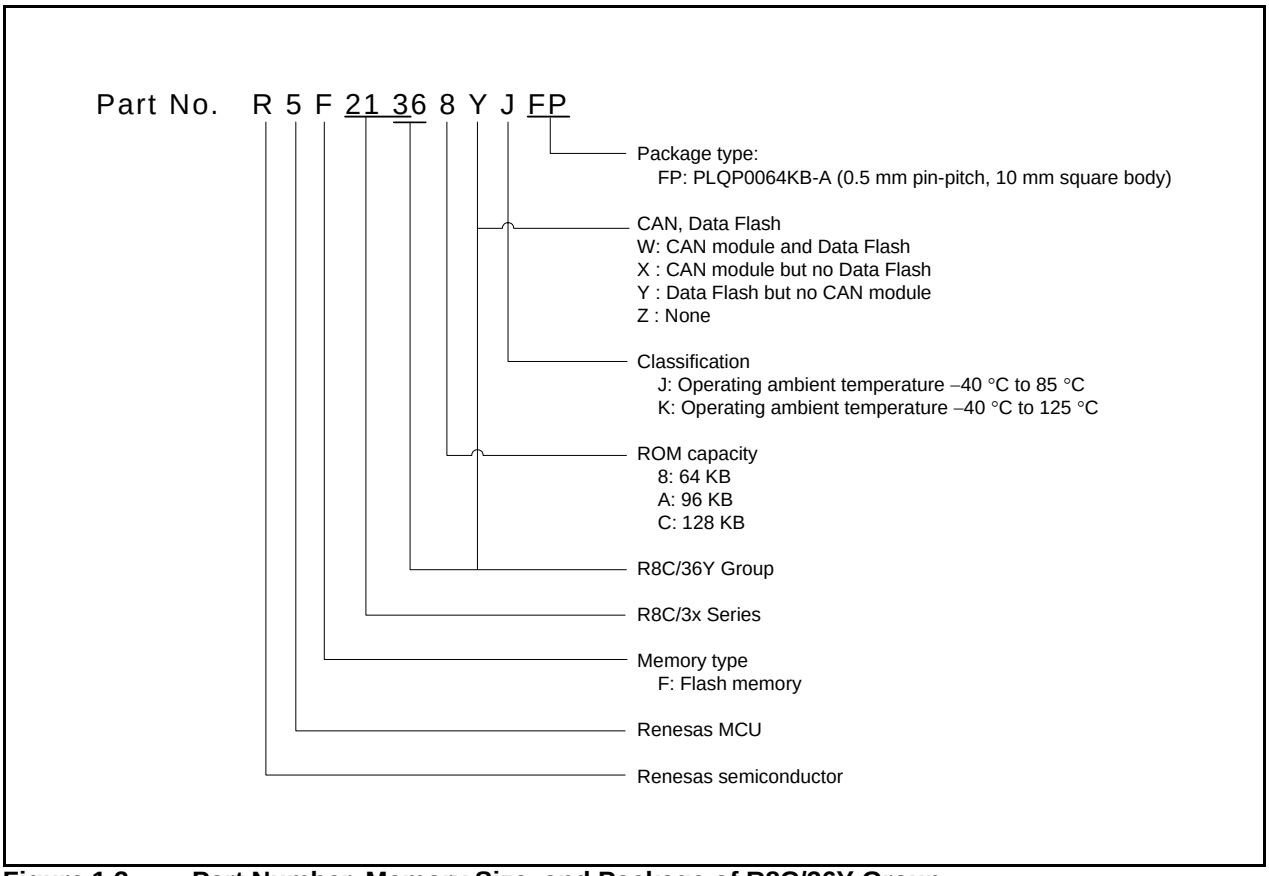



**Figure 1.3 Part Number, Memory Size, and Package of R8C/36Y Group**

**Table 1.13 Pin Name Information by Pin Number (1)**

| Pin Number | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | SSU | CAN Module (2) | A/D Converter Voltage Detection Circuit |
| 1 | | P3_0 | | (TRAO0) (1)/ TRGCLKA | | | | |
| 2 | | P4_2 | | | | | | VREF |
| 3 | MODE | | | | | | | |
| 4 | | P4_3 | | | | | | |
| 5 | | P4_4 | | | | | | |
| 6 | $\overline{\text{RESET}}$ | | | | | | | |
| 7 | XOUT | P4_7 | | | | | | |
| 8 | VSS/AVSS | | | | | | | |
| 9 | XIN | P4_6 | | | | | | |
| 10 | VCC/AVCC | | | | | | | |
| 11 | | P5_4 | | TRCIOD | | | | |
| 12 | | P5_3 | | TRCIOC | | | | |
| 13 | | P5_2 | | TRCIOB | | | | |
| 14 | | P5_1 | | TRCIOA/ TRCTRG | | | | |
| 15 | | P5_0 | | TRCCLK | | | | |
| 16 | | P3_7 | | TRAO0 | (TXD2)/(SDA2)/ (RXD2)/(SCL2) (1) | SSO | | |
| 17 | | P3_5 | | | (CLK2) (1) | SSCK | | |
| 18 | | P3_4 | | | (TXD2)/(SDA2)/ (RXD2)/(SCL2) (1) | ($\overline{\text{SCS}}$) (1)/SSI | | |
| 19 | | P3_3 | $\overline{\text{INT3}}$ | | $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ | $\overline{\text{SCS}}$/(SSI) (1) | | |
| 20 | | P2_7 | | TRDIOD1 | | | | |
| 21 | | P2_6 | | TRDIOC1 | | | | |
| 22 | | P2_5 | | TRDIOB1 | | | | |
| 23 | | P2_4 | | TRDIOA1 | | | | |
| 24 | | P2_3 | | TRDIOD0 | | | | |
| 25 | | P2_2 | | TRDIOC0 | | | | |
| 26 | | P2_1 | | TRDIOB0 | | | | |
| 27 | | P2_0 | | TRDIOA0/ TRDCLK | | | | |
| 28 | | P3_6 | ($\overline{\text{INT1}}$) (1) | | | | | |
| 29 | | P3_1 | | (TRBO) (1) | | | | |
| 30 | | P8_6 | | | | | | |
| 31 | | P8_5 | | TRFO12 | | | | |
| 32 | | P8_4 | | TRFO11 | | | | |
| 33 | | P8_3 | | TRFO10/TRFI | | | | |
| 34 | | P8_2 | | TRFO02 | | | | |
| 35 | | P8_1 | | TRFO01 | | | | |
| 36 | | P8_0 | | TRFO00 | | | | |
| 37 | | P6_7 | ($\overline{\text{INT3}}$) (1) | | (RXD2)/(SCL2) (1) | | | |
| 38 | | P6_6 | $\overline{\text{INT2}}$ | | (TXD2)/(SDA2) (1) | | | |
| 39 | | P6_5 | $\overline{\text{INT4}}$ | | (CLK2) (1)/(CLK1) (1) | | | |
| 40 | | P4_5 | $\overline{\text{INT0}}$ | | | | | $\overline{\text{ADTRG}}$ |
| 41 | | P1_7 | $\overline{\text{INT1}}$ | (TRAIO0) (1) | | | | ANEX3 |
| 42 | | P1_6 | | | CLK0 | | | ANEX2 |
| 43 | | P1_5 | ($\overline{\text{INT1}}$) (1) | (TRAIO0) (1) | RXD0 | | | ANEX1 |
| 44 | | P1_4 | | | TXD0 | | | ANEX0 |
| 45 | | P1_3 | $\overline{\text{KI3}}$ | TRBO | | | | AN11 |

Notes:
1. This can be assigned to the pin in parentheses by a program.
2. Only for the R8C/36W Group and R8C/36X Group.

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

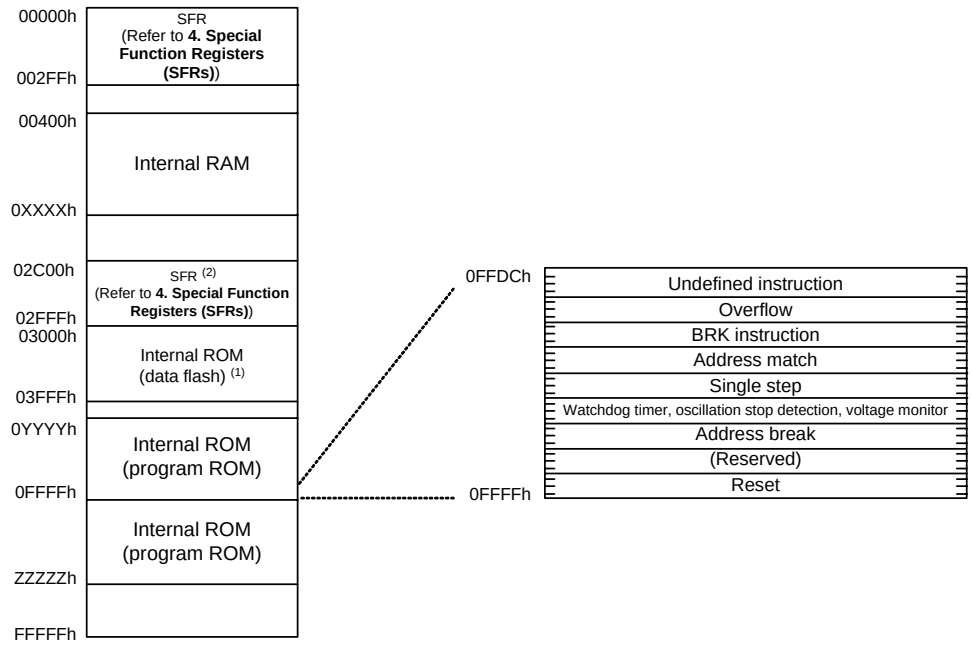
### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

# 3. Memory

## 3.1 R8C/36W Group

Figure 3.1 is a Memory Map of R8C/36W Group. The R8C/36W Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



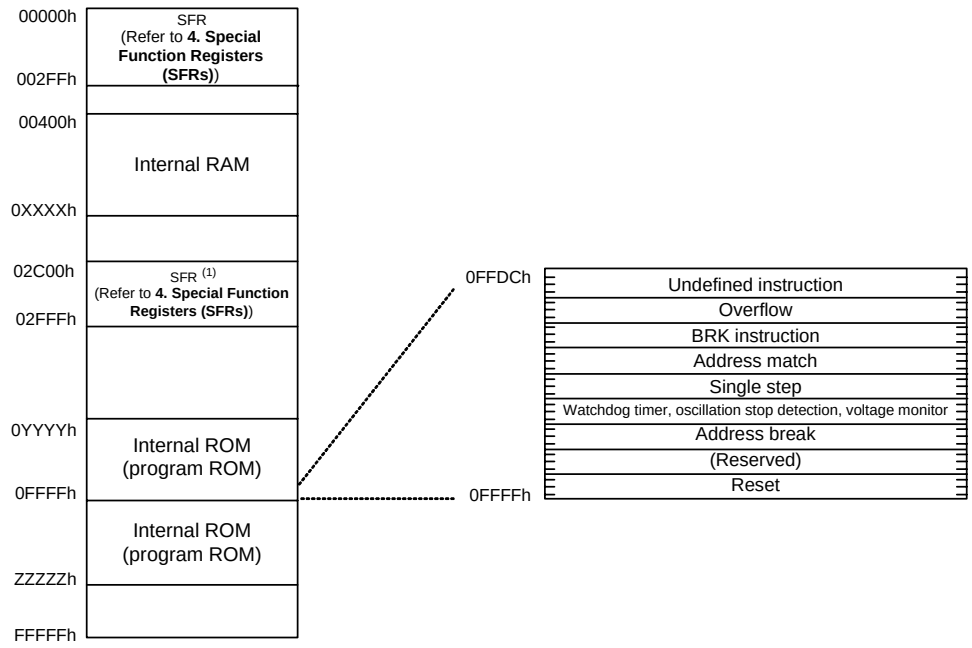

Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21368WJFP, R5F21368WKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2136AWJFP, R5F2136AWKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2136CWJFP, R5F2136CWKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.1 Memory Map of R8C/36W Group**

## 3.2 R8C/36X Group

Figure 3.2 is a Memory Map of R8C/36X Group. The R8C/36X Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



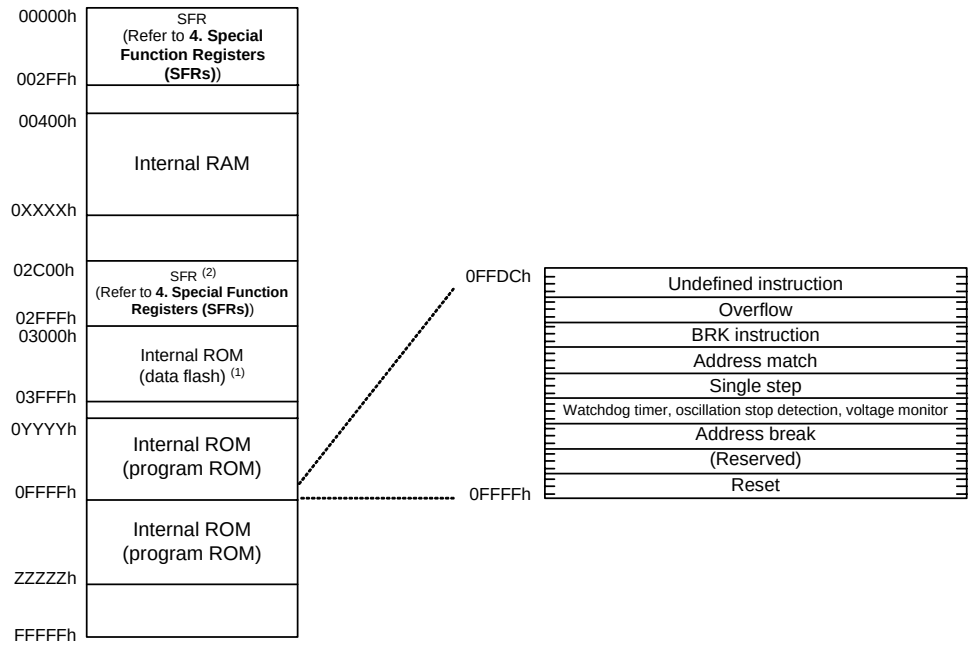

Notes:
1. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21368XJFP, R5F21368XKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2136AXJFP, R5F2136AXKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2136CXJFP, R5F2136CXKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.2 Memory Map of R8C/36X Group**

## 3.3 R8C/36Y Group

Figure 3.3 is a Memory Map of R8C/36Y Group. The R8C/36Y Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



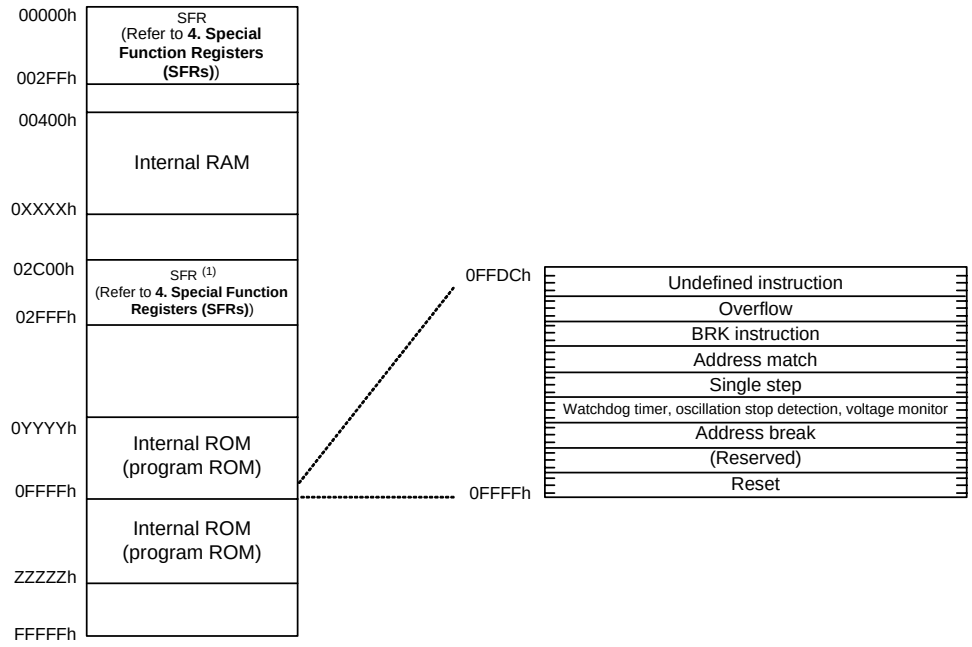

Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21368YJFP, R5F21368YKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2136AYJFP, R5F2136AYKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2136CYJFP, R5F2136CYKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.3 Memory Map of R8C/36Y Group**

## 3.4 R8C/36Z Group

Figure 3.4 is a Memory Map of R8C/36Z Group. The R8C/36Z Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.




Notes:
1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

| Part Number | Internal ROM | | | Internal RAM | |
|---|---|---|---|---|---|
| | Size | Address 0YYYYh | Address ZZZZZh | Size | Address 0XXXXh |
| R5F21368ZJFP, R5F21368ZKFP | 64 Kbytes | 04000h | 13FFFh | 6 Kbytes | 01BFFh |
| R5F2136AZJFP, R5F2136AZKFP | 96 Kbytes | 04000h | 1BFFFh | 8 Kbytes | 023FFh |
| R5F2136CZJFP, R5F2136CZKFP | 128 Kbytes | 04000h | 23FFFh | 10 Kbytes | 02BFFh |

**Figure 3.4 Memory Map of R8C/36Z Group**

**Table 4.4 SFR Information (4) (1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 00C0h | A/D Register 0 | AD0 | XXh |
| 00C1h | | | 000000XXb |
| 00C2h | A/D Register 1 | AD1 | XXh |
| 00C3h | | | 000000XXb |
| 00C4h | A/D Register 2 | AD2 | XXh |
| 00C5h | | | 000000XXb |
| 00C6h | A/D Register 3 | AD3 | XXh |
| 00C7h | | | 000000XXb |
| 00C8h | A/D Register 4 | AD4 | XXh |
| 00C9h | | | 000000XXb |
| 00CAh | A/D Register 5 | AD5 | XXh |
| 00CBh | | | 000000XXb |
| 00CCh | A/D Register 6 | AD6 | XXh |
| 00CDh | | | 000000XXb |
| 00CEh | A/D Register 7 | AD7 | XXh |
| 00CFh | | | 000000XXb |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Mode Register | ADMOD | 00h |
| 00D5h | A/D Input Select Register | ADINSEL | 11000000b |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | Port P5 Register | P5 | XXh |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | Port P5 Direction Register | PD5 | 00h |
| 00ECh | Port P6 Register | P6 | XXh |
| 00EDh | | | |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | | | |
| 00F0h | Port P8 Register | P8 | XXh |
| 00F1h | | | |
| 00F2h | Port P8 Direction Register | PD8 | 00h |
| 00F3h | | | |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | | | |
| 00F9h | | | |
| 00FAh | | | |
| 00FBh | | | |
| 00FCh | | | |
| 00FDh | | | |
| 00FEh | | | |
| 00FFh | | | |

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

**Table 4.5 SFR Information (5) (1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0100h | Timer RA0 Control Register | TRA0CR | 00h |
| 0101h | Timer RA0 I/O Control Register | TRA0IOC | 00h |
| 0102h | Timer RA0 Mode Register | TRA0MR | 00h |
| 0103h | Timer RA0 Prescaler Register | TRA0PRE | FFh |
| 0104h | Timer RA0 Register | TRA0 | FFh |
| 0105h | LIN0 Control Register 2 | LIN0CR2 | 00h |
| 0106h | LIN0 Control Register | LIN0CR | 00h |
| 0107h | LIN0 Status Register | LIN0ST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | Timer RA1 Control Register | TRA1CR | 00h |
| 0111h | Timer RA1 I/O Control Register | TRA1IOC | 00h |
| 0112h | Timer RA1 Mode Register | TRA1MR | 00h |
| 0113h | Timer RA1 Prescaler Register | TRA1PRE | FFh |
| 0114h | Timer RA1 Register | TRA1 | FFh |
| 0115h | LIN1 Control Register 2 | LIN1CR2 | 00h |
| 0116h | LIN1 Control Register | LIN1CR | 00h |
| 0117h | LIN1 Status Register | LIN1ST | 00h |
| 0118h | Timer RE Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Compare Data Register | TREMIN | 00h |
| 011Ah | | | |
| 011Bh | | | |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Count Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011000b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | Timer RC Trigger Control Register | TRCADCR | 00h |
| 0134h | | | |
| 0135h | | | |
| 0136h | Timer RD Trigger Control Register | TRDADCR | 00h |
| 0137h | Timer RD Start Register | TRDSTR | 11111100b |
| 0138h | Timer RD Mode Register | TRDMR | 00001110b |
| 0139h | Timer RD PWM Mode Register | TRDPMR | 10001000b |
| 013Ah | Timer RD Function Control Register | TRDFCR | 10000000b |
| 013Bh | Timer RD Output Master Enable Register 1 | TRDOER1 | FFh |
| 013Ch | Timer RD Output Master Enable Register 2 | TRDOER2 | 01111111b |
| 013Dh | Timer RD Output Control Register | TRDOCR | 00h |
| 013Eh | Timer RD Digital Filter Function Select Register 0 | TRDDF0 | 00h |
| 013Fh | Timer RD Digital Filter Function Select Register 1 | TRDDF1 | 00h |

Note:
1. The blank areas are reserved and cannot be accessed by users.

**Table 4.9 SFR Information (9) (1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2C00h | DTC Transfer Vector Area | | XXh |
| 2C01h | DTC Transfer Vector Area | | XXh |
| 2C02h | DTC Transfer Vector Area | | XXh |
| 2C03h | DTC Transfer Vector Area | | XXh |
| 2C04h | DTC Transfer Vector Area | | XXh |
| 2C05h | | | |
| 2C06h | | | |
| 2C07h | | | |
| 2C08h | DTC Transfer Vector Area | | XXh |
| 2C09h | DTC Transfer Vector Area | | XXh |
| 2C0Ah | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| : | DTC Transfer Vector Area | | XXh |
| 2C3Ah | | | |
| 2C3Bh | | | |
| 2C3Ch | | | |
| 2C3Dh | | | |
| 2C3Eh | | | |
| 2C3Fh | | | |
| 2C40h | DTC Control Data 0 | DTCD0 | XXh |
| 2C41h | | | XXh |
| 2C42h | | | XXh |
| 2C43h | | | XXh |
| 2C44h | | | XXh |
| 2C45h | | | XXh |
| 2C46h | | | XXh |
| 2C47h | | | XXh |
| 2C48h | DTC Control Data 1 | DTCD1 | XXh |
| 2C49h | | | XXh |
| 2C4Ah | | | XXh |
| 2C4Bh | | | XXh |
| 2C4Ch | | | XXh |
| 2C4Dh | | | XXh |
| 2C4Eh | | | XXh |
| 2C4Fh | | | XXh |
| 2C50h | DTC Control Data 2 | DTCD2 | XXh |
| 2C51h | | | XXh |
| 2C52h | | | XXh |
| 2C53h | | | XXh |
| 2C54h | | | XXh |
| 2C55h | | | XXh |
| 2C56h | | | XXh |
| 2C57h | | | XXh |
| 2C58h | DTC Control Data 3 | DTCD3 | XXh |
| 2C59h | | | XXh |
| 2C5Ah | | | XXh |
| 2C5Bh | | | XXh |
| 2C5Ch | | | XXh |
| 2C5Dh | | | XXh |
| 2C5Eh | | | XXh |
| 2C5Fh | | | XXh |
| 2C60h | DTC Control Data 4 | DTCD4 | XXh |
| 2C61h | | | XXh |
| 2C62h | | | XXh |
| 2C63h | | | XXh |
| 2C64h | | | XXh |
| 2C65h | | | XXh |
| 2C66h | | | XXh |
| 2C67h | | | XXh |
| 2C68h | DTC Control Data 5 | DTCD5 | XXh |
| 2C69h | | | XXh |
| 2C6Ah | | | XXh |
| 2C6Bh | | | XXh |
| 2C6Ch | | | XXh |
| 2C6Dh | | | XXh |
| 2C6Eh | | | XXh |
| 2C6Fh | | | XXh |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.17 SFR Information (17) (1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 2F3Ah | CAN0 Message Control Register 10 | C0MCTL10 | 00h |
| 2F3Bh | CAN0 Message Control Register 11 | C0MCTL11 | 00h |
| 2F3Ch | CAN0 Message Control Register 12 | C0MCTL12 | 00h |
| 2F3Dh | CAN0 Message Control Register 13 | C0MCTL13 | 00h |
| 2F3Eh | CAN0 Message Control Register 14 | C0MCTL14 | 00h |
| 2F3Fh | CAN0 Message Control Register 15 | C0MCTL15 | 00h |
| 2F40h | CAN0 Control Register | C0CTLR | 00000101b |
| 2F41h | | | 00h |
| 2F42h | CAN0 Status Register | C0STR | 00000101b |
| 2F43h | | | 00h |
| 2F44h | CAN0 Bit Configuration Register | C0BCR | 00h |
| 2F45h | | | 00h |
| 2F46h | | | 00h |
| 2F47h | | | |
| 2F48h | CAN0 Receive FIFO Control Register | C0RFCR | 10000000b |
| 2F49h | CAN0 Receive FIFO Pointer Control Register | C0RFPCR | XXh |
| 2F4Ah | CAN0 Transmit FIFO Control Register | C0TFCR | 10000000b |
| 2F4Bh | CAN0 Transmit FIFO Pointer Control Register | C0TFPCR | XXh |
| 2F4Ch | CAN0 Error Interrupt Enable Register | C0EIER | 00h |
| 2F4Dh | CAN0 Error Interrupt Factor Judge Register | C0EIFR | 00h |
| 2F4Eh | CAN0 Reception Error Count Register | C0RECR | 00h |
| 2F4Fh | CAN0 Transmission Error Count Register | C0TECR | 00h |
| 2F50h | CAN0 Error Code Store Register | C0ECSR | 00h |
| 2F51h | CAN0 Channel Search Support Register | C0CSSR | XXh |
| 2F52h | CAN0 Mailbox Search Status Register | C0MSSR | 10000000b |
| 2F53h | CAN0 Mailbox Search Mode Register | C0MSMR | 00h |
| 2F54h | CAN0 Time Stamp Register | C0TSR | 00h |
| 2F55h | | | 00h |
| 2F56h | CAN0 Acceptance Filter Support Register | C0AFSR | XXh |
| 2F57h | | | XXh |
| 2F58h | CAN0 Test Control Register | C0TCR | 00h |
| : | | | |
| 2FFFh | | | |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

### Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | High-speed on-chip oscillator frequency after reset | $V_{CC}$ = 2.7 to 5.5 V, −40°C ≤ $T_{opr}$ ≤ 85°C (J version) / −40°C ≤ $T_{opr}$ ≤ 125°C (K version) | – | 40 | – | MHz |
| | High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (3) | | – | 36.864 | – | MHz |
| | High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register | | – | 32 | – | MHz |
| | High-speed on-chip oscillator frequency temperature • supply voltage dependence (2) | | –5 | – | 5 | % |
| – | Oscillation stabilization time | | – | 200 | – | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 400 | – | µA |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = –40 to 85°C (J version) / –40 to 125°C (K version).
2. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.
3. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

### Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 112.5 | 125 | 137.5 | kHz |
| fOCO-WDT | Low-speed on-chip oscillator frequency for watchdog timer | | 112.5 | 125 | 137.5 | kHz |
| – | Oscillation stabilization time | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 30 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 3 | – | µA |

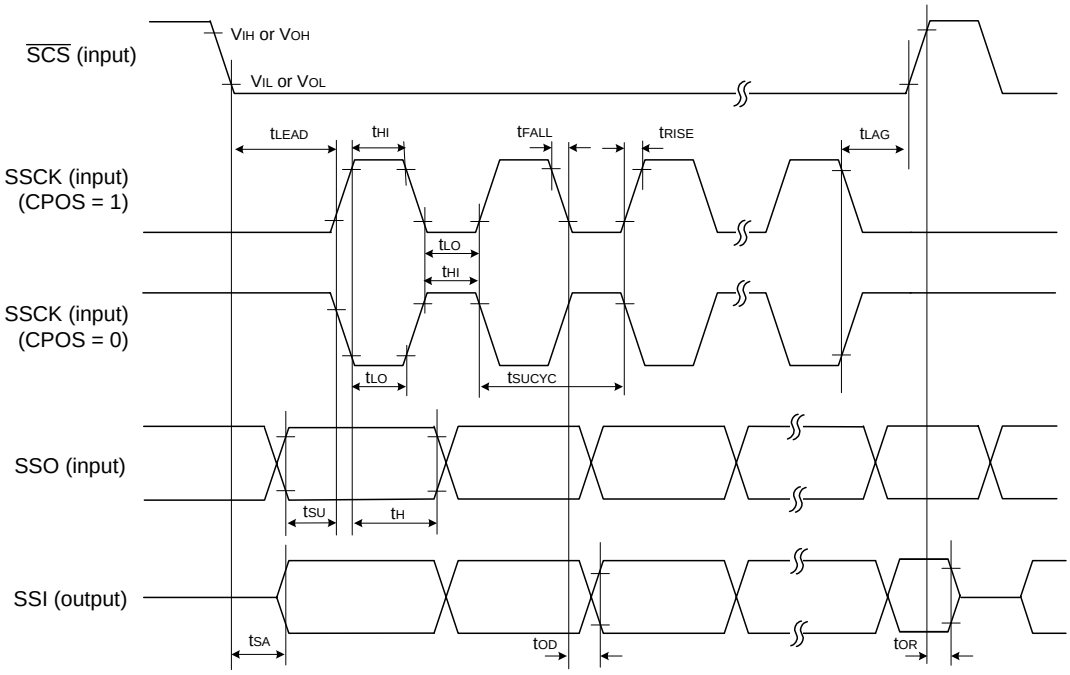
Note:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = –40 to 85°C (J version) / –40 to 125°C (K version).

### Table 5.13 Power Supply Circuit Timing Characteristics

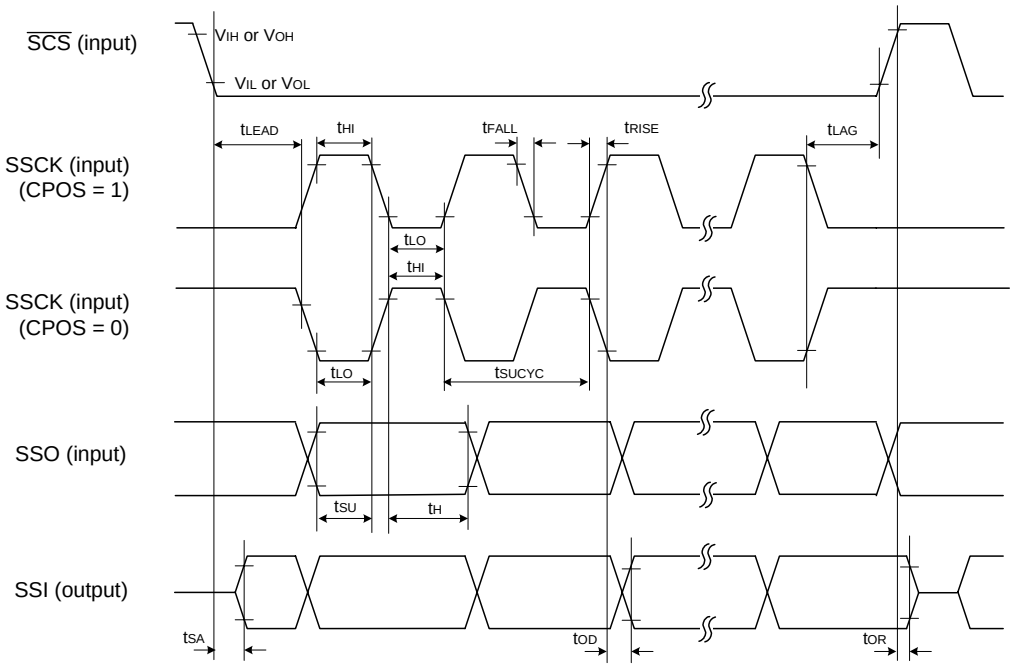
| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on (2) | | – | – | 2000 | µs |

Notes:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = –40 to 85°C (J version) / –40 to 125°C (K version).
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

4-Wire Bus Communication Mode, Slave, CPHS = 1




4-Wire Bus Communication Mode, Slave, CPHS = 0




CPHS, CPOS: Bits in SSMR register

**Figure 5.5 I/O Timing of SSU (Slave)**

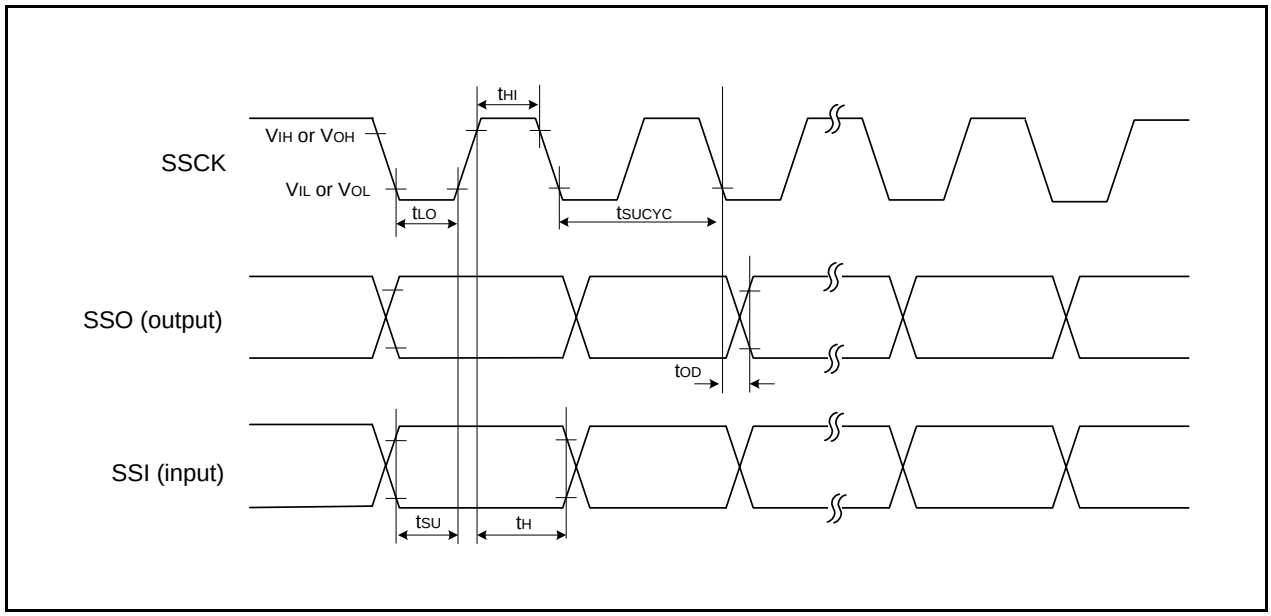



**Figure 5.6 I/O Timing of SSU (Clock Synchronous Communication Mode)**

**Table 5.17 Electrical Characteristics (3) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = −40 to 125°C (K version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode (1) | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 7.0 | 15 | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5.6 | 12.5 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.6 | – | mA |
| | | | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.2 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | High-speed on-chip oscillator mode (1) | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 7.0 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3.0 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | – | 90 | 400 | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 15 | 330 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 5 | 320 | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 2.0 | 5.0 | µA |
| | | | XIN clock off, Topr = 125°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 60.0 | – | µA |

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

### Timing Requirements
**(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = –40°C to 85°C (J ver)/–40°C to 125°C (K ver))**

**Table 5.18 External clock input (XOUT)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 50 | – | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 24 | – | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 24 | – | ns |

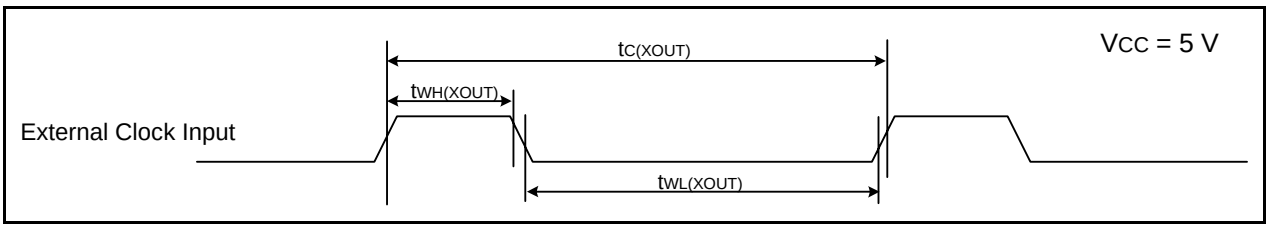



**Figure 5.7 External Clock Input Timing Diagram when Vcc = 5 V**

**Table 5.19 TRAIOi (i = 0 to 1) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIOi (i = 0 to 1) input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIOi (i = 0 to 1) input “H” width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIOi (i = 0 to 1) input “L” width | 40 | – | ns |

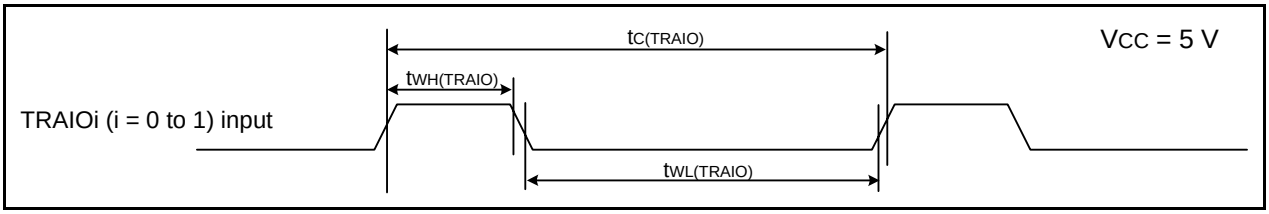



**Figure 5.8 TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 5 V**

**Table 5.20 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRFI)}$ | TRFI input cycle time | 1200 (1) | – | ns |
| $t_{WH(TRFI)}$ | TRFI input “H” width | 600 (2) | – | ns |
| $t_{WL(TRFI)}$ | TRFI input “L” width | 600 (2) | – | ns |

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

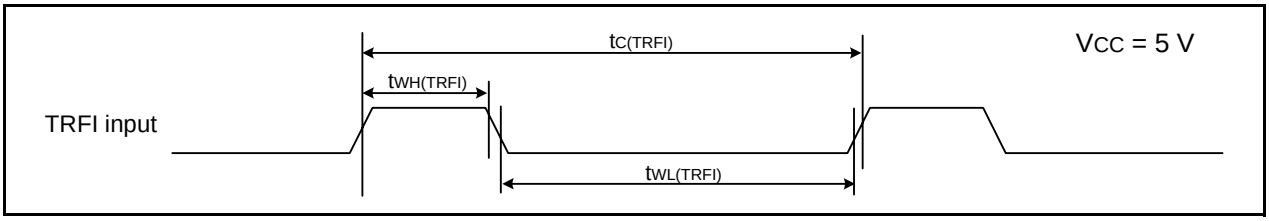



**Figure 5.9 TRFI Input Timing Diagram when Vcc = 5 V**

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