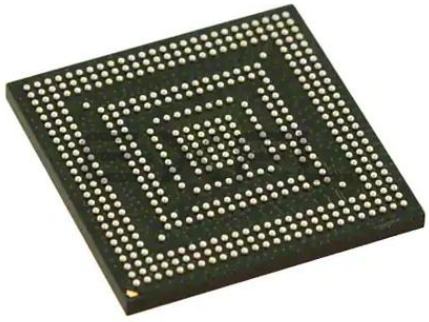

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31cvkn5c

minimal power consumption using the most advanced techniques for power saving (DPTC, DVFS, power gating, clock gating). With 90 nm technology and dual-Vt transistors (two threshold voltages), the MCIMX31 provides the optimal performance versus leakage current balance.

The performance of the MCIMX31 is boosted by a multi-level cache system, and features peripheral devices such as an MPEG-4 Hardware Encoder (VGA, 30 fps), an Autonomous Image Processing Unit, a Vector Floating Point (VFP11) co-processor, and a RISC-based SDMA controller.

The MCIMX31 supports connections to various types of external memories, such as DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The MCIMX31 can be connected to a variety of external devices using technology, such as high-speed USB2.0 OTG, ATA, MMC/SDIO, and compact flash.

1.1 Features

The MCIMX31 is designed for the high-tier, mid-tier smartphone markets, and portable media players. They provide low-power solutions for high-performance demanding multimedia and graphics applications.

The MCIMX31 is built around the ARM11 MCU core and implemented in the 90 nm technology.

The systems include the following features:

- Multimedia and floating-point hardware acceleration supporting:
  - MPEG-4 real-time encode of up to VGA at 30 fps
  - MPEG-4 real-time video post-processing of up to VGA at 30 fps
  - Video conference call of up to QCIF-30 fps (decoder in software), 128 kbps
  - Video streaming (playback) of up to VGA-30 fps, 384 kbps
  - 3D graphics and other applications acceleration with the ARM® tightly-coupled Vector Floating Point co-processor
  - On-the-fly video processing that reduces system memory load (for example, the power-efficient viewfinder application with no involvement of either the memory system or the ARM CPU)
- Advanced power management
  - Dynamic voltage and frequency scaling
  - Multiple clock and power domains
  - Independent gating of power domains
- Multiple communication and expansion ports including a fast parallel interface to an external graphic accelerator (supporting major graphic accelerator vendors)
- Security

1.3 Block Diagram

Figure 1 shows the MCIMX31 simplified interface block diagram.

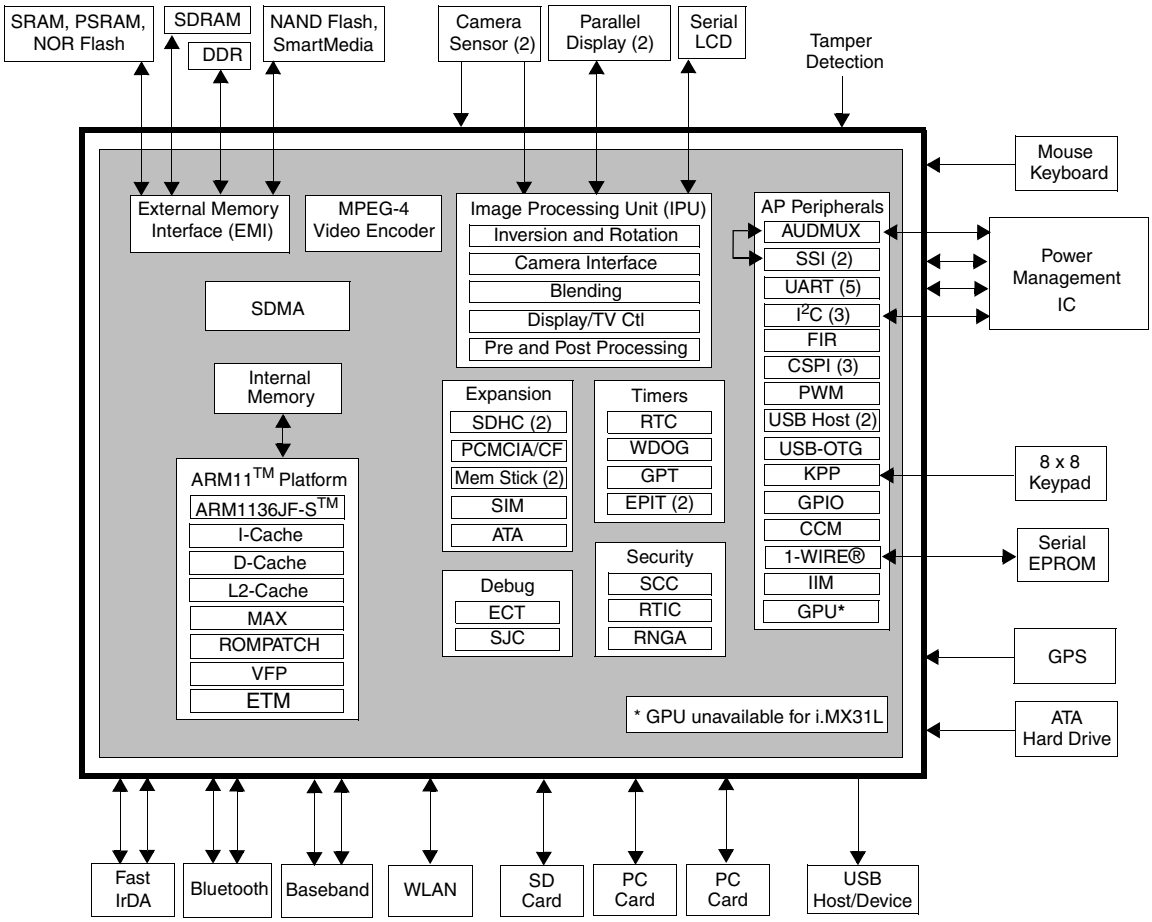


Figure 1. MCIMX31 Simplified Interface Block Diagram

2 Functional Description and Application Information

2.1 ARM11 Microprocessor Core

The CPU of the MCIMX31 is the ARM1136JF-S core based on the ARM v6 architecture. It supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes), and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline
- Branch prediction with return stack
- Low-interrupt latency

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
SCC	Security Controller Module	Security	The SCC is a hardware component composed of two blocks—the Secure RAM module, and the Security Monitor. The Secure RAM provides a way of securely storing sensitive information.	—
SDHC	Secured Digital Host Controller	Connectivity Peripheral	The SDHC controls the MMC (MultiMediaCard), SD (Secure Digital) memory, and I/O cards by sending commands to cards and performing data accesses to and from the cards.	4.3.19/89
SDMA	Smart Direct Memory Access	System Control Peripheral	The SDMA controller maximizes the system's performance by relieving the ARM core of the task of bulk data transfer from memory to memory or between memory and on-chip peripherals.	—
SIM	Subscriber Identification Module	Connectivity Peripheral	The SIM interfaces to an external Subscriber Identification Card. It is an asynchronous serial interface adapted for Smart Card communication for e-commerce applications.	4.3.20/90
SJC	Secure JTAG Controller	Debug	The SJC provides debug and test control with maximum security and provides a flexible architecture for future derivatives or future multi-cores architecture.	4.3.21/94
SSI	Synchronous Serial Interface	Multimedia Peripheral	The SSI is a full-duplex, serial port that allows the device to communicate with a variety of serial devices, such as standard codecs, Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.	4.3.22/96
UART	Universal Asynchronous Receiver/Transmitter	Connectivity Peripheral	The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.	—
USB	Universal Serial Bus— 2 Host Controllers and 1 OTG (On-The-Go)	Connectivity Peripherals	• USB Host 1 is designed to support transceiverless connection to the on-board peripherals in Low Speed and Full Speed mode, and connection to the ULPI (UTMI+ Low-Pin Count) and Legacy Full Speed transceivers. • USB Host 2 is designed to support transceiverless connection to the Cellular Modem Baseband Processor. • The USB-OTG controller offers HS/FS/LS capabilities in Host mode and HS/FS in device mode. In Host mode, the controller supports direct connection of a FS/LS device (without external hub). In device (bypass) mode, the OTG port functions as gateway between the Host 1 Port and the OTG transceiver.	4.3.23/104
WDOG	Watchdog Timer Module	Timer Peripheral	The WDOG module protects against system failures by providing a method for the system to recover from unexpected events or programming errors.	—

Table 8 provides the operating ranges.

NOTE

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

Table 8. Operating Ranges

Symbol	Parameter	Min	Max	Units
QVCC, QVCC1, QVCC4	Core Operating Voltage[1,2,3]			V
	Silicon rev 1.15, 1.2, and 2.0 — $0 \le f_{ARM} \le 400$ MHz, non-overdrive	1.22	1.47	
	$0 \le f_{ARM} \le 400$ MHz, overdrive[4]	>1.47	1.65	
	$0 \le f_{ARM} \le 532$ MHz, overdrive[4]	1.55	1.65	
	State Retention Voltage[5]	0.95	—	
NVCC1, NVCC3–10	I/O Supply Voltage, except DDR[6] non-overdrive	1.75	3.1	V
	overdrive[7]	>3.1	3.3	
NVCC2, NVCC21, NVCC22	I/O Supply Voltage, DDR only	1.75	1.95	V
FVCC, MVCC, SVCC, UVCC	PLL (Phase-Locked Loop) and FPM (Frequency Pre-multiplier) Supply Voltage[8]			V
	non-overdrive	1.3	1.47	
	overdrive[4]	>1.47	1.6	
IOQVDD	On-device Level Shifter Supply Voltage	1.6	1.9	V
FUSE_VDD	Fusebox read Supply Voltage[9, 10]	1.65	1.95	V
	Fusebox write (program) Supply Voltage[11]	3.0	3.3	V
T_A	Operating Ambient Temperature Range[12]	0	70	°C

1 Measured at package balls, including peripherals, ARM, and L2 cache supplies (QVCC, QVCC1, QVCC4, respectively).

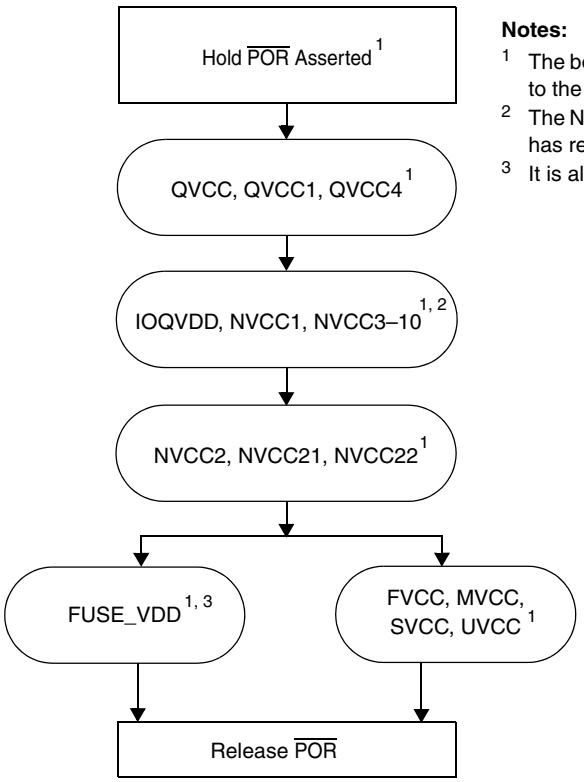
2 The core voltage must be higher than 1.38V to avoid corrupted data during transfers from the USB HS. Please refer to Errata file ENGcm02610 ID.

3 If the Core voltage is supplied by the MC13738, it will be 1.6 ± 0.05 V during the power-up sequence. This is allowed. After power-up the voltage should be reduced to avoid operation in overdrive mode.

4 Supply voltage is considered “overdrive” for voltages above 1.47 V. Operation time in overdrive—whether switching or not—must be limited to a cumulative duration of 1.25 years (10,950 hours) or less to sustain the maximum operating voltage without significant device degradation—for example, 25% (average 6 hours out of 24 yours per day) duty cycle for 5-year rated equipment. To tolerate the maximum operating overdrive voltage for 10 years, the device must have a duty cycle of 12.5% or less in overdrive (for example 3 out of 24 hours per day). Below 1.47V, duty cycle restrictions may apply for equipment rated above 5 years.

5 The SR voltage is applied to QVCC, QVCC1, and QVCC4 after the device is placed in SR mode. The Real-Time Clock (RTC) is operational in State Retention (SR) mode.

6 Overshoot and undershoot conditions (transitions above NVCC and below GND) on I/O must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.



Notes:

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. It is allowable for FVCC, MVCC, SVCC, and UVCC to be up after FUSE_VDD.

Figure 2. Power-Up Sequence for Silicon Revisions 1.2 and Previous

4.2.1.1 Power-Up Sequence for Silicon Revision 2

Silicon revision 2.0 offers two options for power-up sequencing. Option 1 is backwards compatible with silicon revision 1.2 and earlier versions of the IC. It should be noted that using option 1 on silicon Rev. 2.0 introduces a slight increase in current drain on IOQVDD when IOQVDD is raised before NVCC21. The expected resulting increase is in the range of 3 mA to 5 mA, which does not pose a risk to the IC.

Option 2 is an alternative power-up sequence that allows the powering up of NVCC2, NVCC21, NVCC22 with IOQVDD, NVCC1, and NVCC3-10 without producing a current drain increase on IOQVDD.

These two power-up options on the 2.0 silicon allow the user to select the optimum power-up sequence for their application.

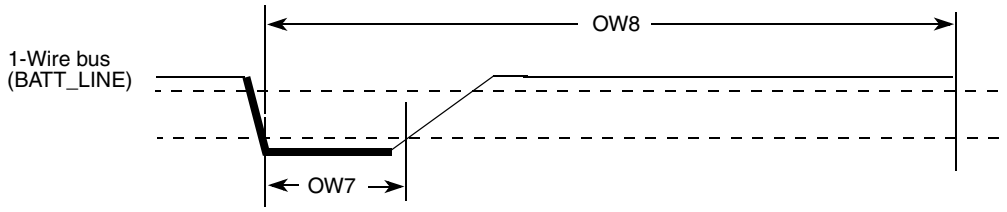


Figure 9. Write 1 Sequence Timing Diagram

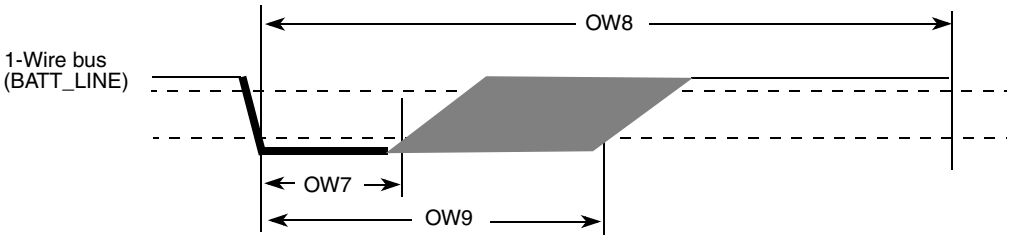


Figure 10. Read Sequence Timing Diagram

Table 23. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Units
OW7	Write 1 / Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.3.5 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA specification.

The user needs to use level shifters for 3.3 Volt or 5.0 Volt compatibility on the ATA interface.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

Table 33. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{OE}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{EB}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{EB}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{LBA}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{LBA}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{ECB}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{ECB}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{DTACK}$ setup time[1]	0	—	ns
WE20	$\overline{DTACK}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing

2 BCLK parameters are being measured from the 50% VDD.

3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 28, Figure 29, Figure 30, Figure 31, Figure 32, and Figure 33 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

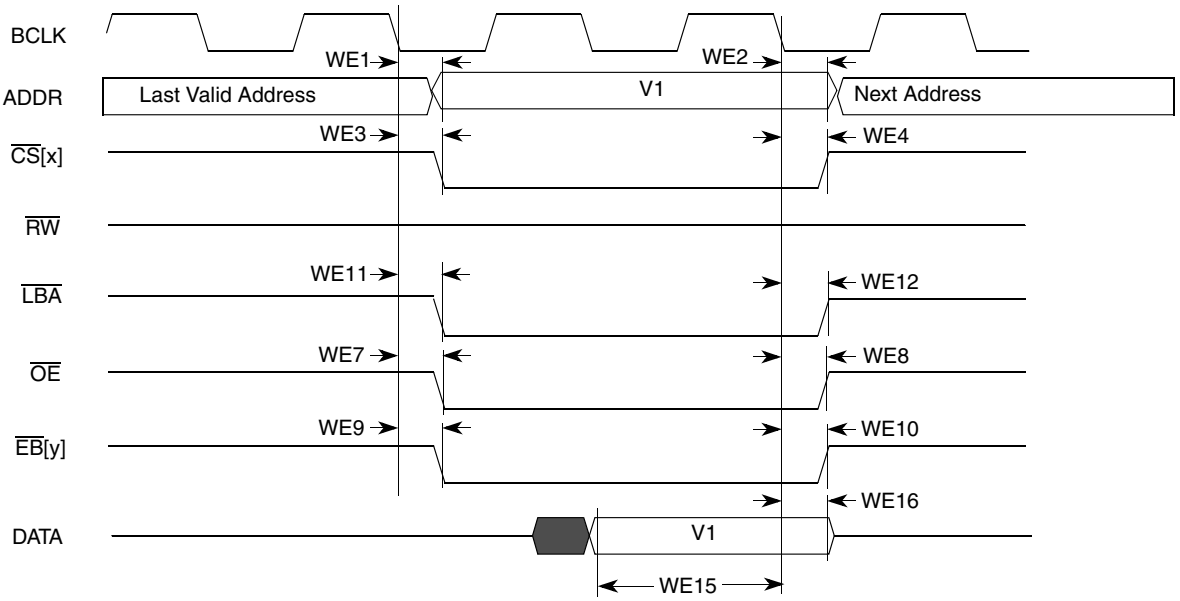


Figure 28. Asynchronous Memory Timing Diagram for Read Access—WSC=1

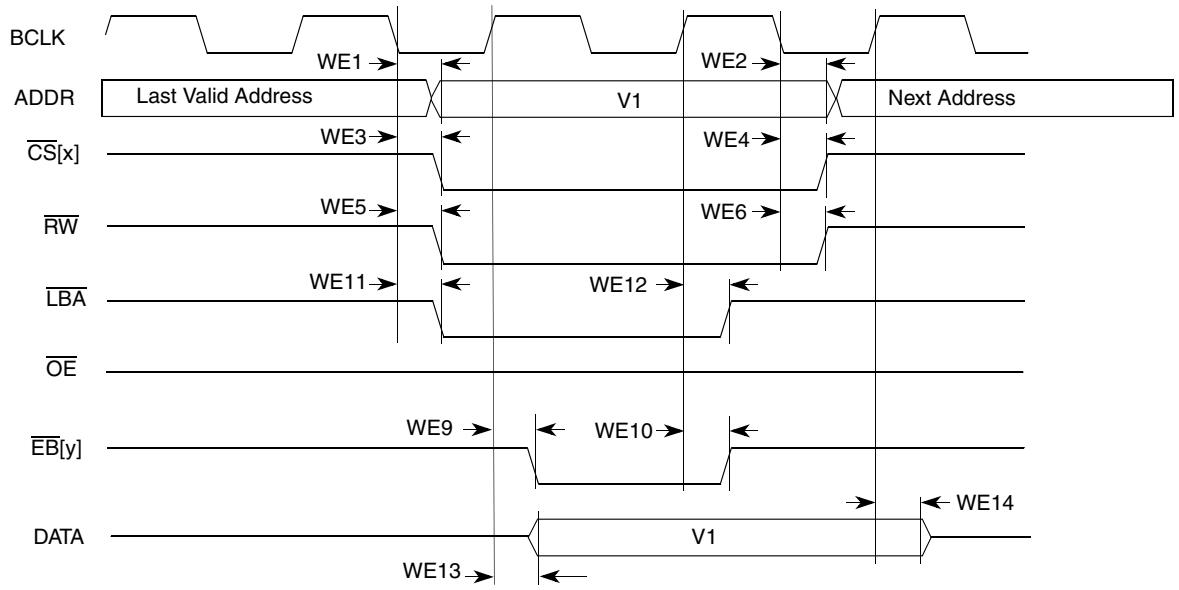


Figure 29. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

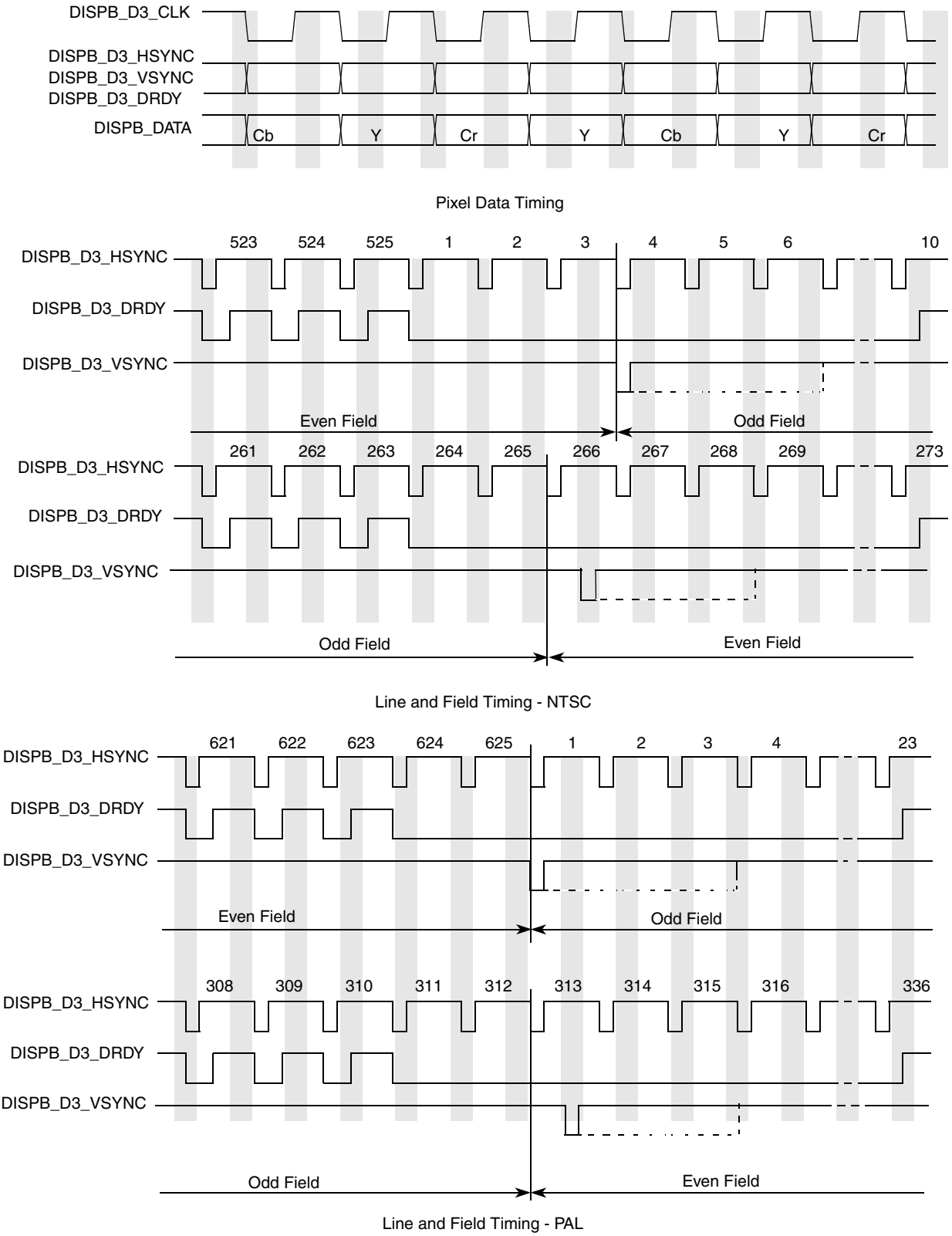


Figure 51. TV Encoder Interface Timing Diagram

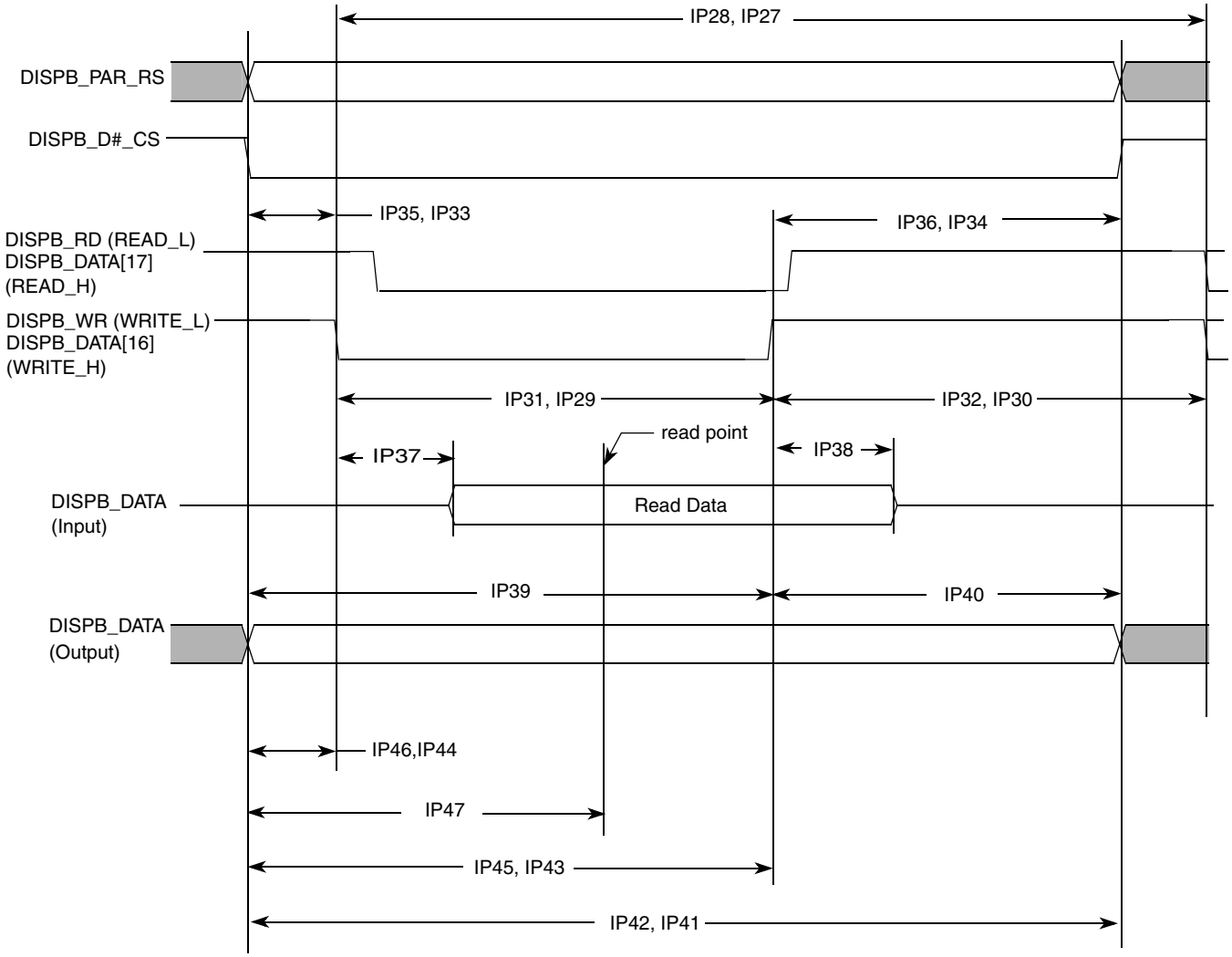


Figure 58. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the aim card will be used by the SIM card to recover the clock from the data much like a standard UART. All six (or 5 in case bi-directional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other.

There are no required timing relationships between the signals in normal mode, but there are some in two specific cases: reset and power down sequences.

4.3.20.1 General Timing Requirements

Figure 73 shows the timing of the SIM module, and Figure 57 lists the timing parameters.

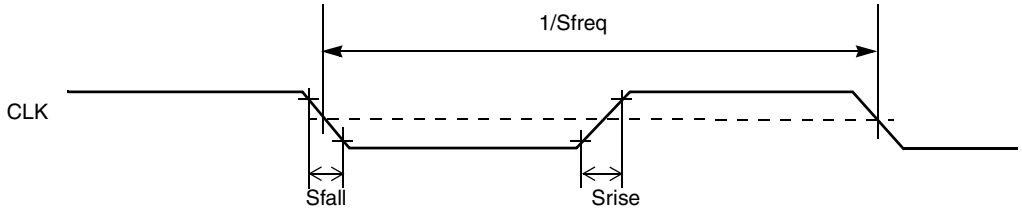


Figure 73. SIM Clock Timing Diagram

Table 57. SIM Timing Specification—High Drive Strength

Num	Description	Symbol	Min	Max	Unit
1	SIM Clock Frequency (CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM CLK Rise Time [2]	S_{rise}	—	20	ns
3	SIM CLK Fall Time [3]	S_{fall}	—	20	ns
4	SIM Input Transition Time (RX, SIMPD)	S_{trans}	—	25	ns

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

4.3.20.2 Reset Sequence

4.3.20.2.1 Cards with Internal Reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 74):

- After powerup, the clock signal is enabled on SGCLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.

4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 76 and Table 58 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

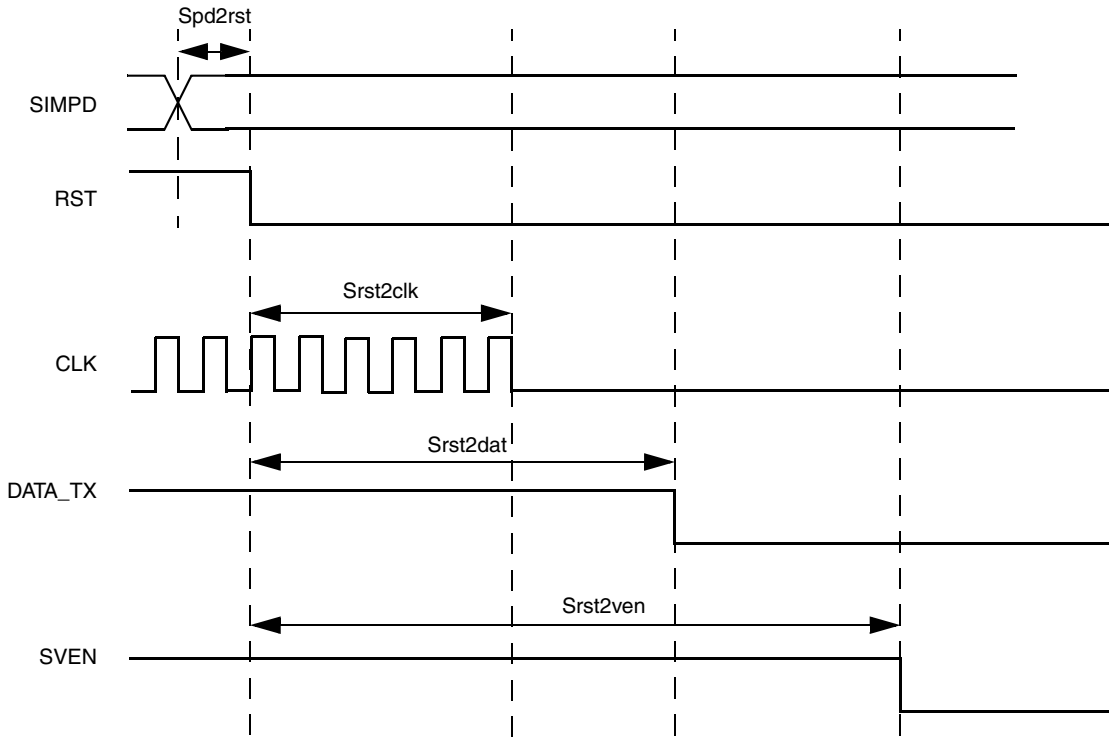


Figure 76. SmartCard Interface Power Down AC Timing

Table 58. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9*1/FCKIL	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8*1/FCKIL	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7*1/FCKIL	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9*1/FCKIL	25	ns

4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 77 depicts the SJC test clock input timing. Figure 78 depicts the SJC boundary scan timing, Figure 79 depicts the SJC test access port, Figure 80 depicts the SJC TRST timing, and Table 59 lists the SJC timing parameters.

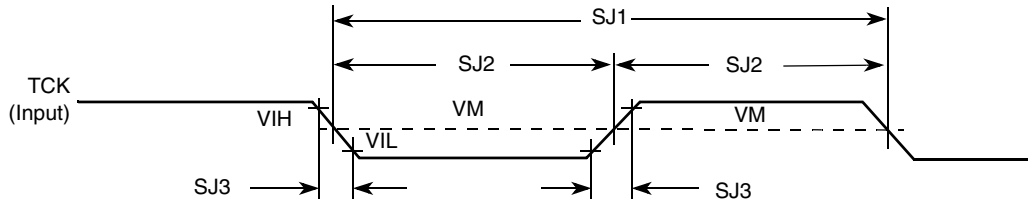


Figure 77. Test Clock Input Timing Diagram

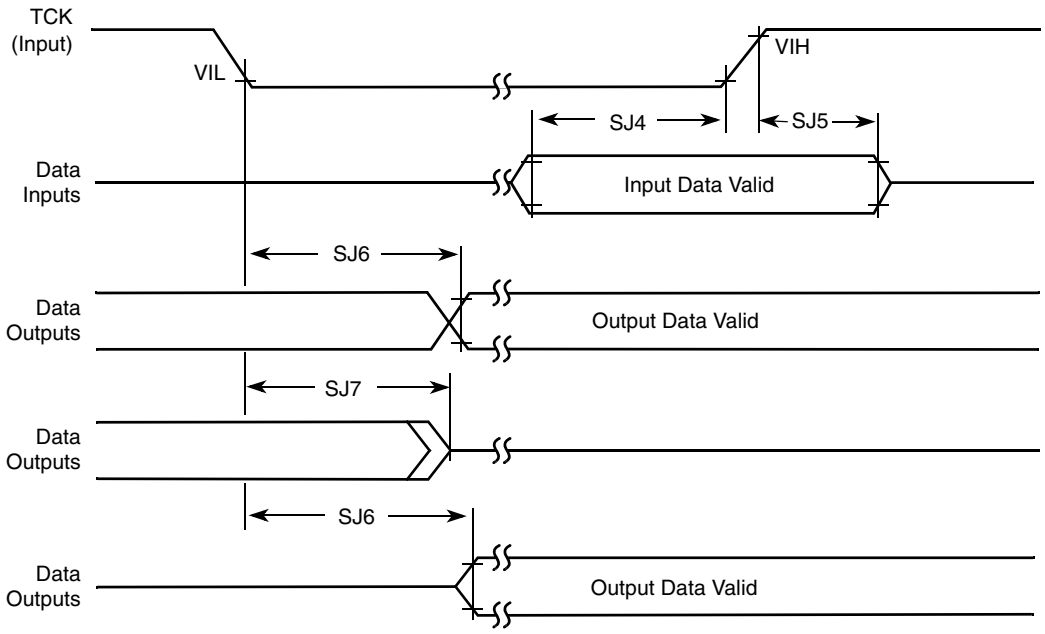
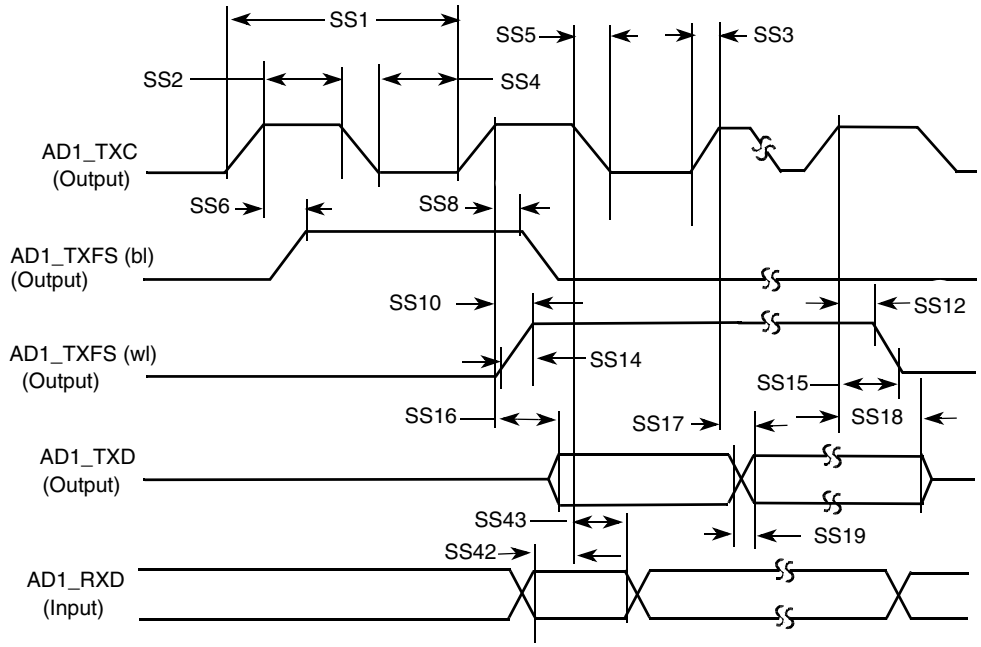
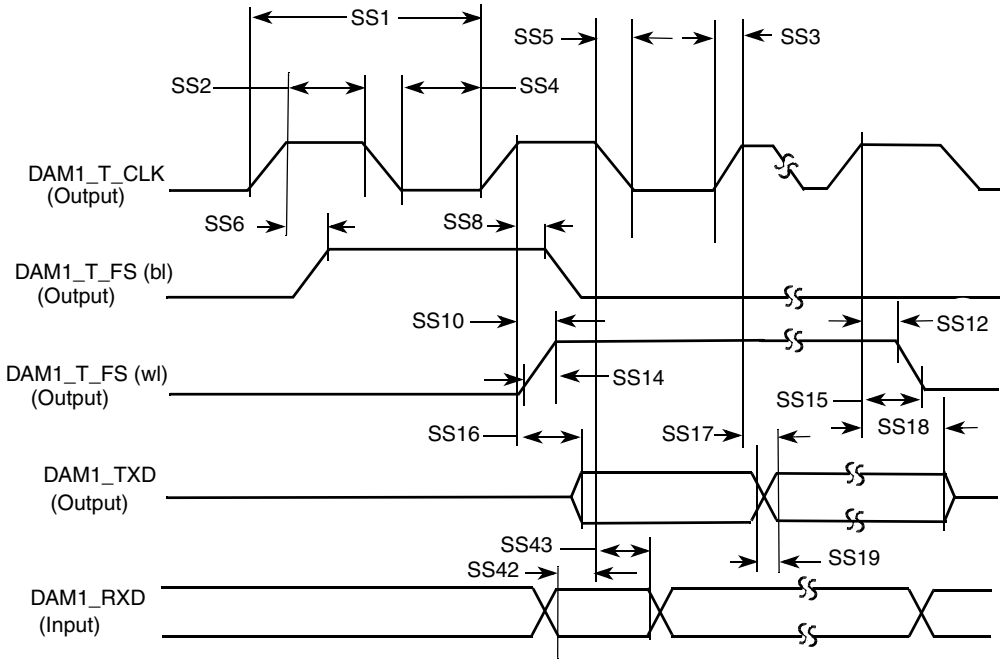


Figure 78. Boundary Scan (JTAG) Timing Diagram



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 81. SSI Transmitter with Internal Clock Timing Diagram

Table 60. SSI Transmitter with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6	ns
SS15	(Tx/Rx) Internal FS fall time	—	6	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0	—	ns
SS52	Loading	—	25	pF

4.3.22.2 SSI Receiver Timing with Internal Clock

Figure 82 depicts the SSI receiver timing with internal clock, and Table 61 lists the timing parameters.

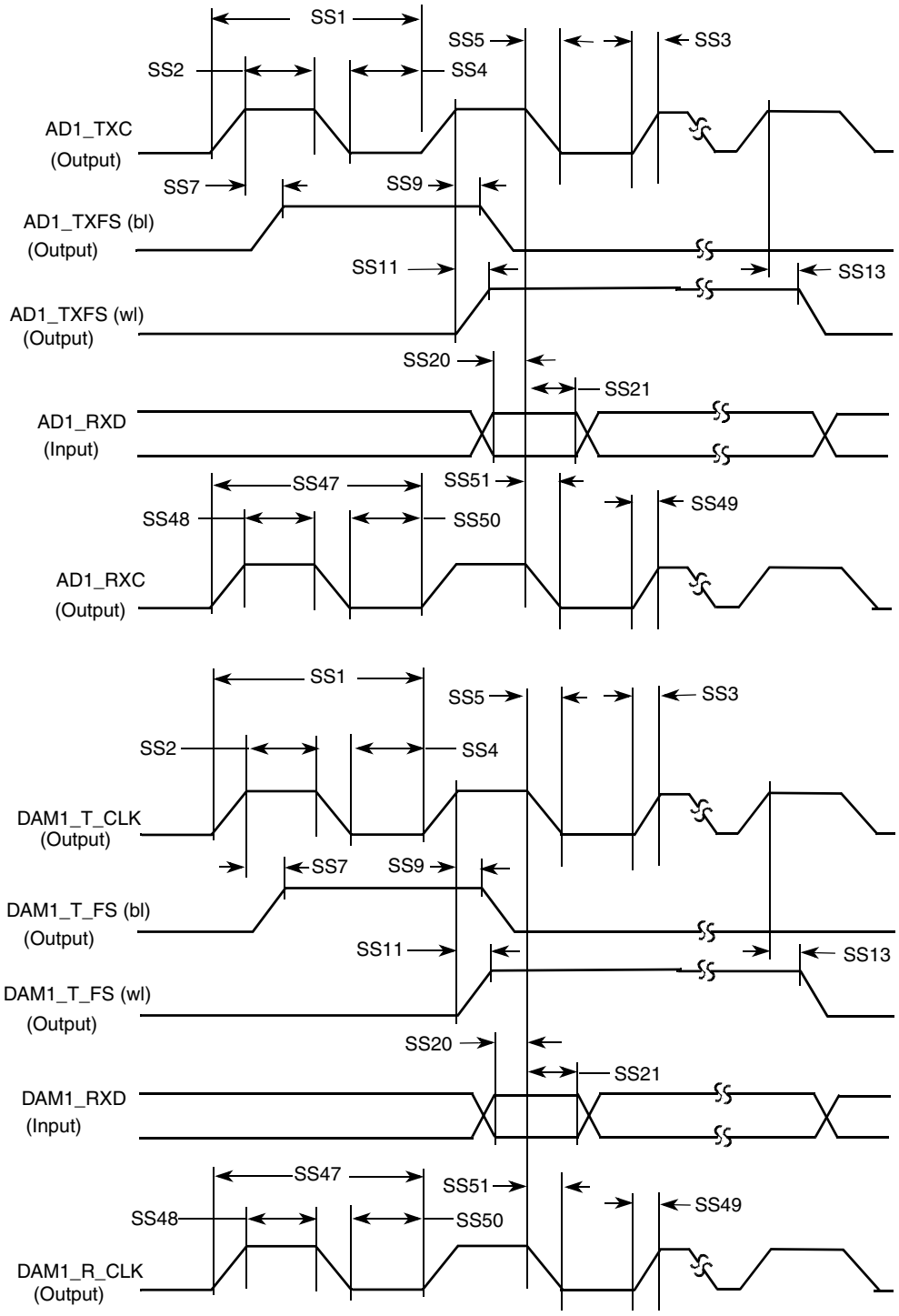


Figure 82. SSI Receiver with Internal Clock Timing Diagram

Table 62. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
SDCLK	AA21
$\overline{\text{SDCLK}}$	AE20
SDQS0	AD16
SDQS1	AE12
SDQS2	AD11
SDQS3	AD8
SDWE	AF20
SER_RS	T25
SFS3	R6
SFS4	F3
SFS5	A3
SFS6	T3
SIMPD0	G17
SJC_MOD	A20
SRST0	C19
SRX0	B21
SRXD3	R3
SRXD4	C3
SRXD5	B4
SRXD6	R7
STX0	F17
STXD3	R1
STXD4	B3
STXD5	C5
STXD6	T1
SVEN0	A21
TCK	B19
TDI	F16
TDO	A19
TMS	G16

Signal ID	Ball Location
TXD1	F10
TXD2	C13
USB_BYP	A9
USB_OC	C10
USB_PWR	B10
USBH2_CLK	N1
USBH2_DATA0	M1
USBH2_DATA1	M3
USBH2_DIR	N7
USBH2_NXT	N6
USBH2_STP	M2
USBOTG_CLK	G10
USBOTG_DATA0	F9
USBOTG_DATA1	B8
USBOTG_DATA2	G9
USBOTG_DATA3	A7
USBOTG_DATA4	C8
USBOTG_DATA5	B7
USBOTG_DATA6	F8
USBOTG_DATA7	A6
USBOTG_DIR	B9
USBOTG_NXT	A8
USBOTG_STP	C9
VPG0	G25
VPG1	J20
VSTBY	F26
VSYNC0	N24
VSYNC3	R26
WATCHDOG_RST	A24
WRITE	R25

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
EB1	W21
ECB	Y21
FPSHIFT	M23
GPIO1_0	C19
GPIO1_1	G17
GPIO1_2	B20
LD7	T20
LD8	R17
LD9	U23
M_GRANT	U18
M_REQUEST	T17
MA10	Y2
MCUPG	See VPG0
NFALE	T2
$\overline{\text{NFCE}}$	R4
NFCLE	T1
NFRB	R3
$\overline{\text{NFRE}}$	T4
$\overline{\text{NFWE}}$	T3
$\overline{\text{NFWP}}$	P6
OE	T18
PAR_RS	P22
PC_BVD1	G2
PC_BVD2	H4
$\overline{\text{PC\_CD1}}$	J3
$\overline{\text{PC\_CD2}}$	H1
PC_POE	J6
PC_PWRON	K6
PC_READY	H2
PC_RST	F1
$\overline{\text{PC\_RW}}$	G3
PC_VS1	H3
PC_VS2	G1
$\overline{\text{PC\_WAIT}}$	J4
$\overline{\text{POR}}$	F21
POWER_FAIL	F20
PWMO	F2
RAS	AA19
READ	N18
$\overline{\text{RESET\_IN}}$	F22
RI_DCE1	D10
RI_DTE1	B11
RTCK	D15
RTS1	B9
RTS2	B12
RW	V18

Signal ID	Ball Location
LD17	W23
LD2	R21
LD3	R20
LD4	T23
LD5	T22
LD6	T21
SCK6	R2
SCLK0	B19
SD_D_CLK	M21
SD_D_I	M20
SD_D_IO	M18
SD0	AC18
SD1	AA17
SD1_CLK	K2
SD1_CMD	K3
SD1_DATA0	K4
SD1_DATA1	J1
SD1_DATA2	J2
SD1_DATA3	L6
SD10	AB14
SD11	AC14
SD12	AA13
SD13	AB13
SD14	AC13
SD15	AA12
SD16	AC12
SD17	AA11
SD18	AB11
SD19	AC11
SD2	AB17
SD20	AA10
SD21	AB10
SD22	AC10
SD23	AC9
SD24	AA9
SD25	AC8
SD26	AB8
SD27	AC7
SD28	AA8
SD29	AB7
SD3	AC17
SD30	AA7
SD31	AC6
SD4	AA16
SD5	AC16
SD6	AA15

Table 73. Product Differentiation (continued)

Item	Location	MCIMX31/MCIMX31L	MCIMX31C/MCIMX31LC
GPIO maximum input current (100 kΩ PU)	Table 15, "GPIO DC Electrical Parameters," on page 22	V_I = 0, I_{IN} = 25 μA V_I = NVCC, I_{IN} = 0.1 μA	N/A N/A
Core operating speed	Table 8, "Operating Ranges," on page 13	532 MHz	400 MHz
Package	Table 70, "Ball Map—14 x 14 0.5 mm Pitch," on page 117 and Table 71, "Ball Map—19 x 19 0.8 mm Pitch," on page 118	MAPBGA Packages 457 14 x 14 mm, 0.5 mm Pitch 473 19 x 19 mm, 0.8 mm Pitch	MAPBGA Package 473 19 x 19 mm, 0.8 mm Pitch
Pin Assignment	Table 66, "14 x 14 BGA Signal ID by Ball Grid Location," on page 107 and Table 69, "19 x 19 BGA Signal ID by Ball Grid Location," on page 113	MAPBGA Packages 457 14 x 14 mm, 0.5 mm Pitch 473 19 x 19 mm, 0.8 mm Pitch	MAPBGA Package 473 19 x 19 mm, 0.8 mm Pitch

7 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

MCIMX31 Product Brief (order number MCIMX31PB)

MCIMX31 Reference Manual (order number MCIMX31RM)

MCIMX31 Chip Errata (order number MCIMX31CE)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. ARM Ltd. documentation is available from http://www.arm.com.

8 Revision History

Table 74 summarizes revisions to this document since the release of Rev. 3.4.

Table 74. Revision History

Rev.	Location	Revision
4	Figure 87, Table 73	Updated.
4.1	Table 1, "Ordering Information," on page 3	Added note about JTAG compliance.
4.1	Section 1.2.1/3	Updated with new operating frequencies
4.1	Table 8, "Operating Ranges," on page 13	Added new operating frequencies