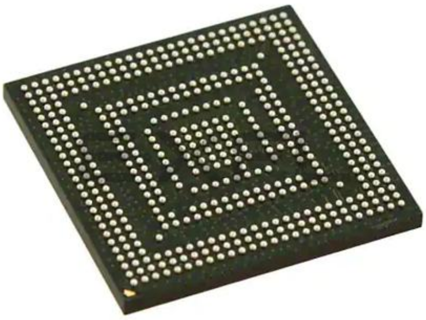

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31lvkn5

4 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the MCIMX31.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

Table 4. MCIMX31 Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 5, "Absolute Maximum Ratings"	on page 10
Table 7, "Thermal Resistance Data—19 × 19 mm Package"	on page 11
Table 8, "Operating Ranges"	on page 13
Table 9, "Specific Operating Ranges for Silicon Revision 2.0"	on page 14
Table 10, "Interface Frequency"	on page 14
Section 4.1.1, "Supply Current Specifications"	on page 16
Section 4.2, "Supply Power-Up/Power-Down Requirements and Restrictions"	on page 19

CAUTION

Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 8, "Operating Ranges," on page 13 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Core)	$QVCC_{max}$	–0.5	1.65	V
Supply Voltage (I/O)	$NVCC_{max}$	–0.5	3.3	V
Input Voltage Range	V_{Imax}	–0.5	NVCC +0.3	V
Storage Temperature	$T_{storage}$	–40	125	°C
ESD Damage Immunity:	V_{esd}			V
Human Body Model (HBM)		—	1500	
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	500	
Offset voltage allowed in run mode between core supplies.	V_{core_offset}[1]	—	15	mV

[1] The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

Table 11. Fusebox Supply Current Parameters

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	eFuse Program Current.[1] Current to program one eFuse bit: efuse_pgm = 3.0 V	$I_{program}$	—	35	60	mA
2	eFuse Read Current[2] Current to read an 8-bit eFuse word vdd_fusebox = 1.875 V	I_{read}	—	5	8	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word, and only applies to Silicon Rev. 1.2 and previous.

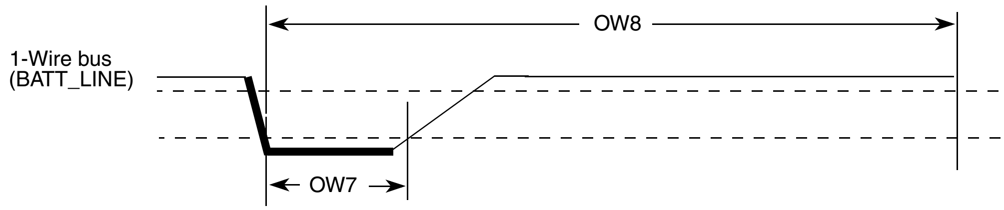

Figure 9. Write 1 Sequence Timing Diagram

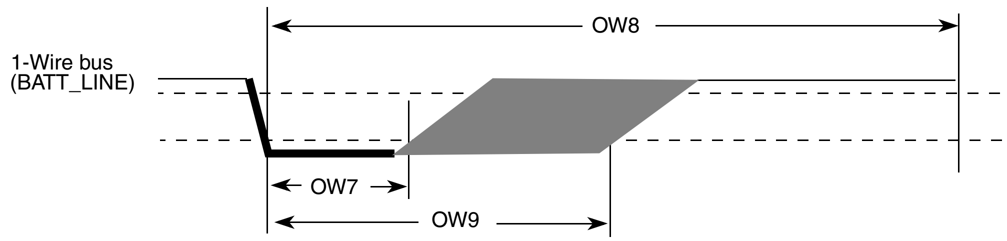

Figure 10. Read Sequence Timing Diagram

Table 23. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Units
OW7	Write 1 / Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.3.5 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA specification.

The user needs to use level shifters for 3.3 Volt or 5.0 Volt compatibility on the ATA interface.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

4.3.5.2 PIO Mode Timing

Figure 11 shows timing for PIO read, and Table 25 lists the timing parameters for PIO read.

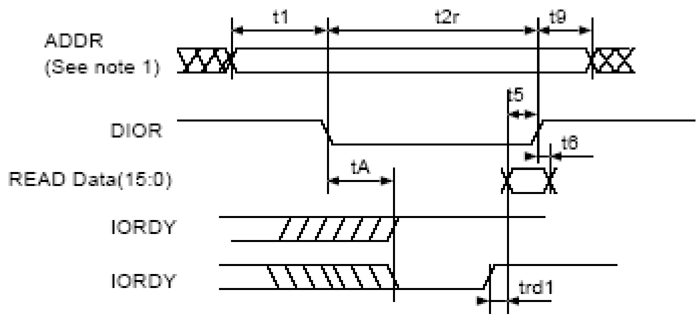

Figure 11. PIO Read Timing Diagram

Table 25. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 11	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9

Figure 12 shows timing for PIO write, and Table 26 lists the timing parameters for PIO write.

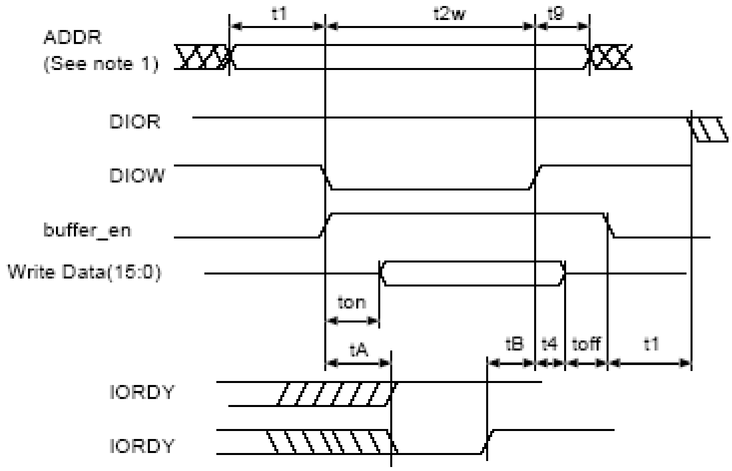

Figure 12. Multiword DMA (MDMA) Timing

Table 26. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 12	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w * T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 * T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 13 shows timing for MDMA read, Figure 14 shows timing for MDMA write, and Table 27 lists the timing parameters for MDMA read and write.

4.3.5.4 UDMA Out Timing

Figure 18 shows timing when the UDMA out transfer starts, Figure 19 shows timing when the UDMA out host terminates transfer, Figure 20 shows timing when the UDMA out device terminates transfer, and Table 29 lists the timing parameters for UDMA out burst.

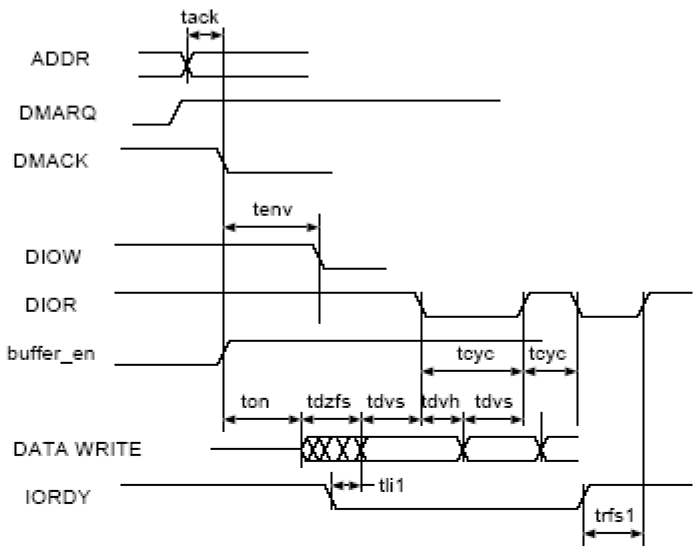

Figure 18. UDMA Out Transfer Starts Timing Diagram

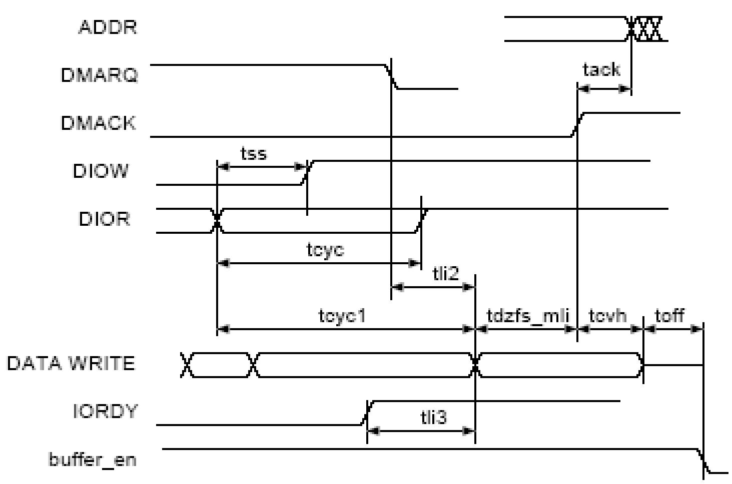

Figure 19. UDMA Out Host Terminates Transfer Timing Diagram

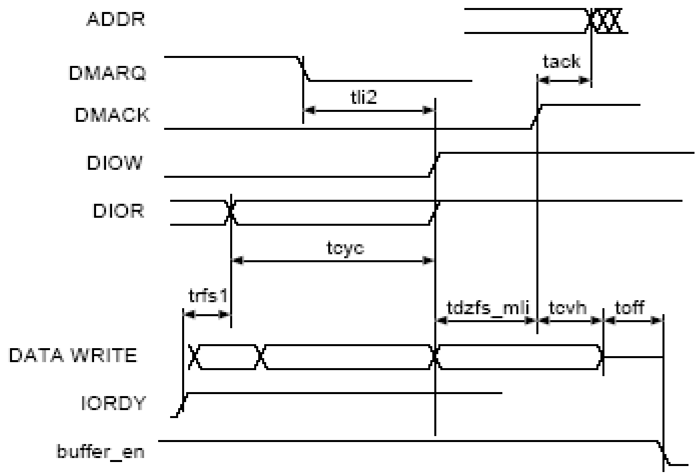

Figure 20. UDMA Out Device Terminates Transfer Timing Diagram

Table 29. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 18, Figure 19, Figure 20	Value	Controlling Variable
tack	tack	tack (min) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env * T) – (tskew1 + tskew2) tenv (max) = (time_env * T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs * T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh * T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc * T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc * 2 * T	time_cyc
trfs1	trfs	trfs = 1.6 * T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs * T – (tskew1)	time_dzfs
tss	tss	tss = time_ss * T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) * T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

Table 33. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{\text{OE}}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{\text{EB}}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{\text{EB}}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{\text{LBA}}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{\text{LBA}}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{\text{ECB}}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{\text{ECB}}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{\text{DTACK}}$ setup time[1]	0	—	ns
WE20	$\overline{\text{DTACK}}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing
2 BCLK parameters are being measured from the 50% VDD.
3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 28, Figure 29, Figure 30, Figure 31, Figure 32, and Figure 33 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

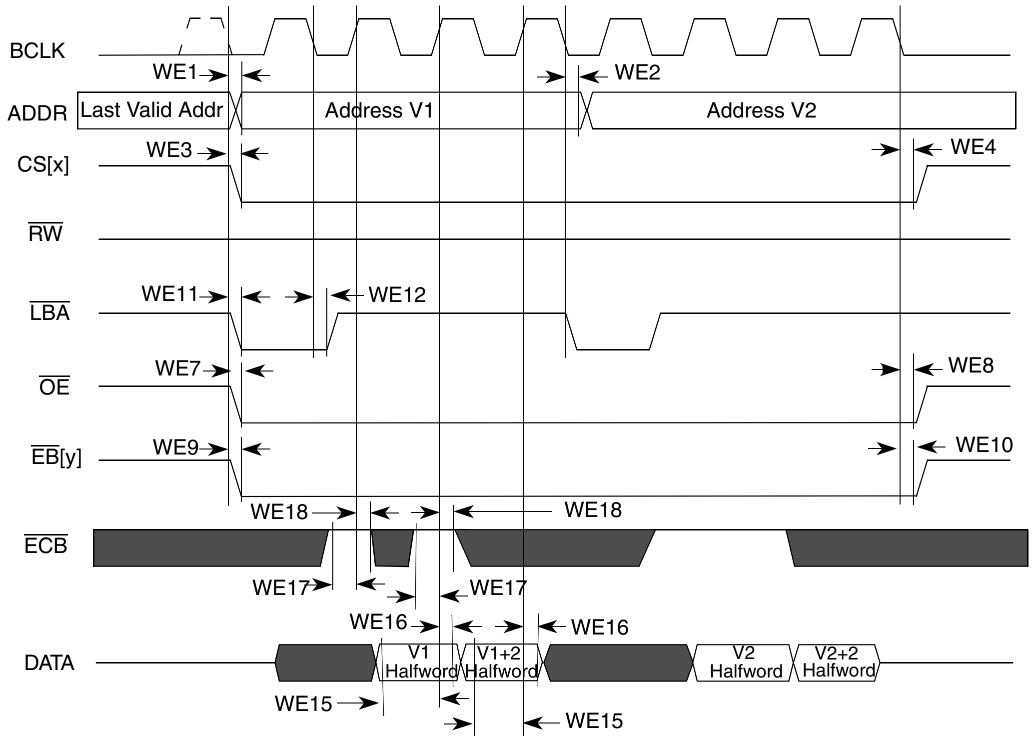

Figure 30. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses— WSC=2, SYNC=1, DOL=0

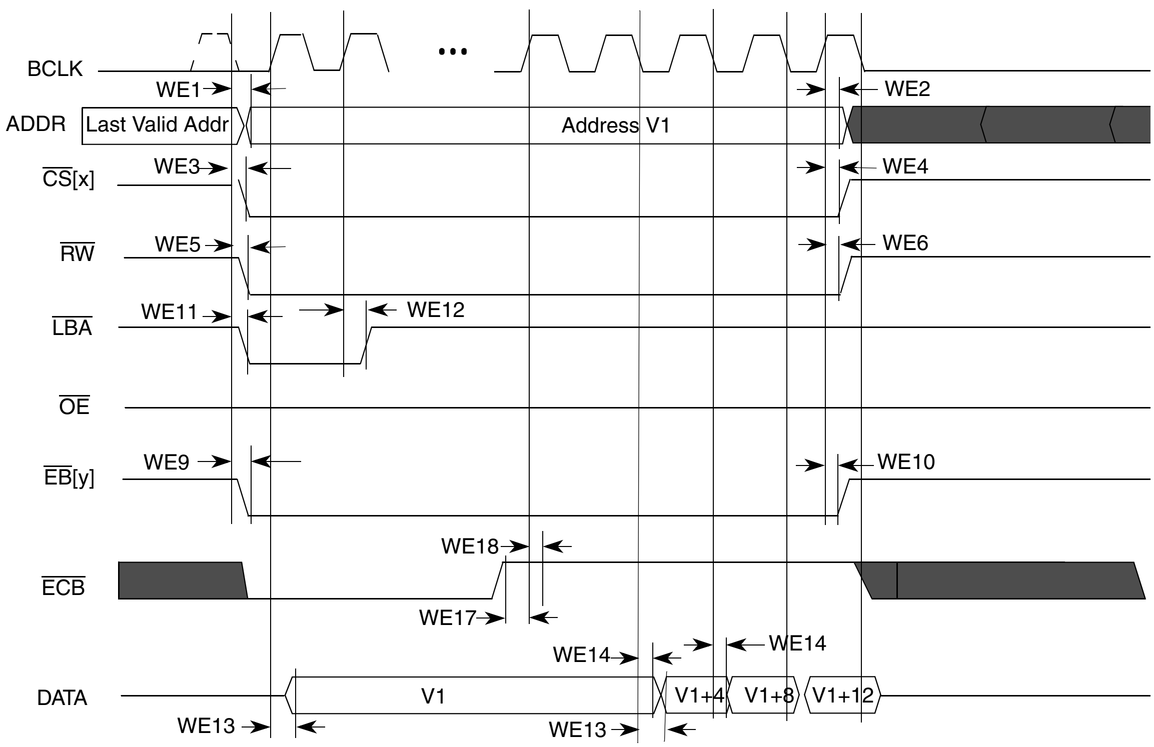

Figure 31. Synchronous Memory TIming Diagram for Burst Write Access— BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1

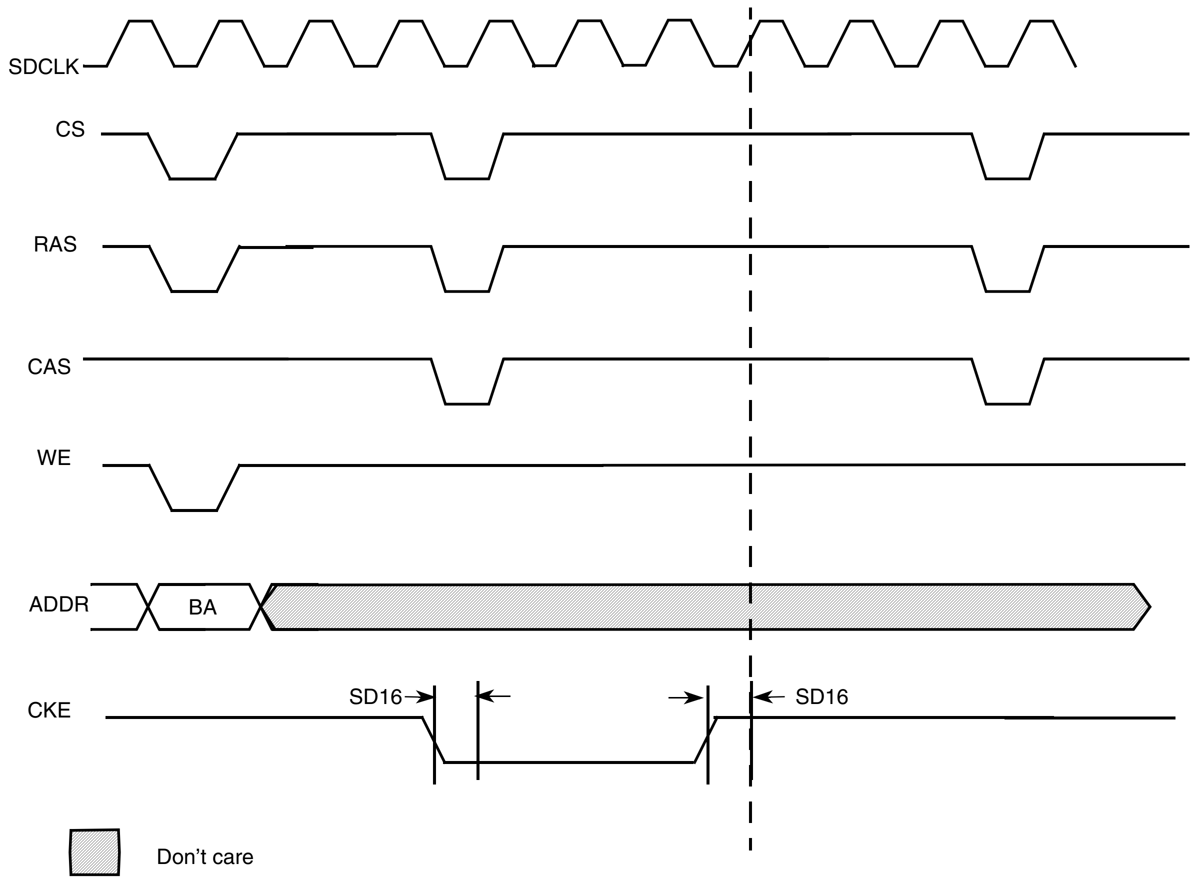

Figure 37. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 37. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

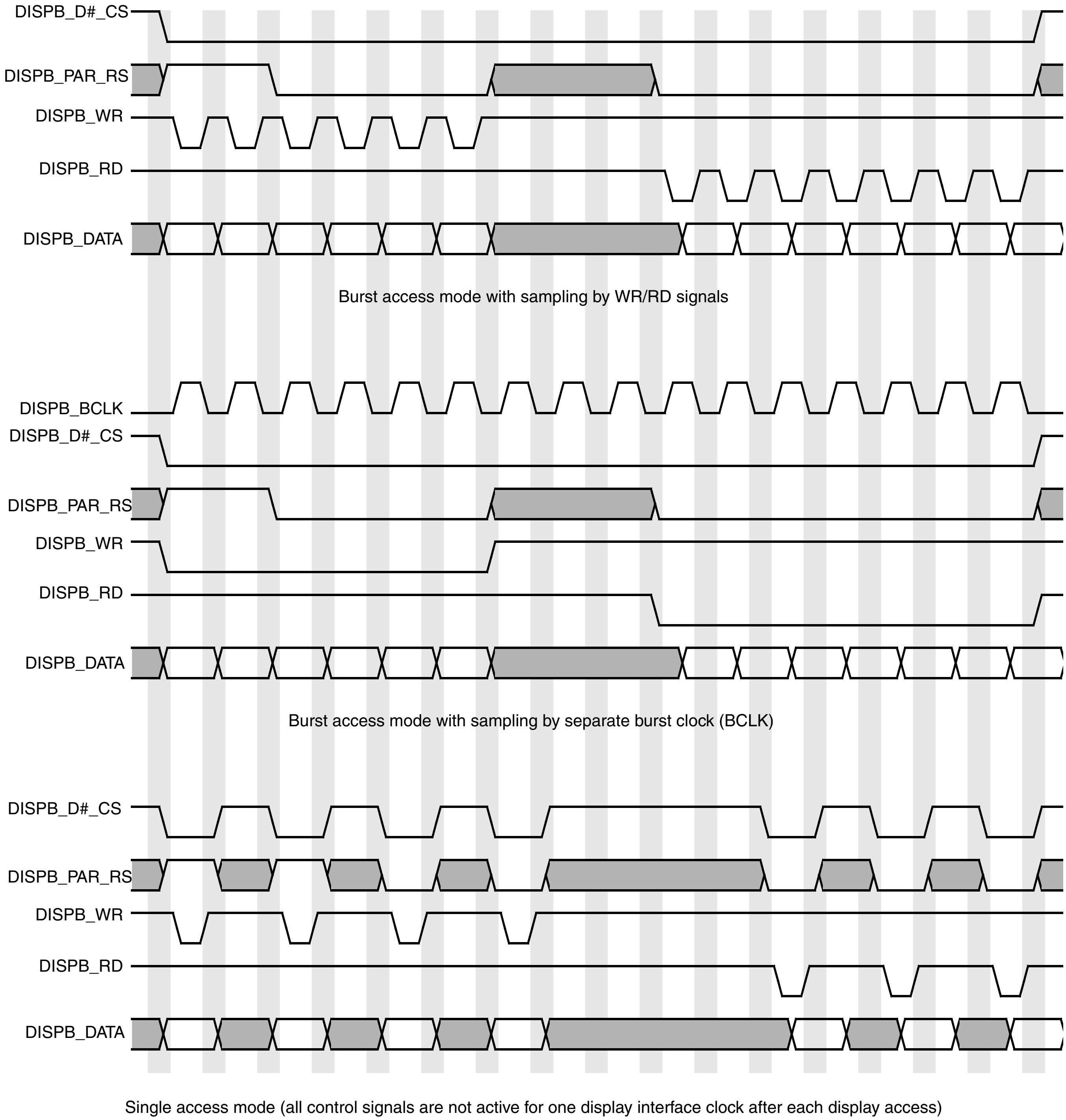

Figure 53. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

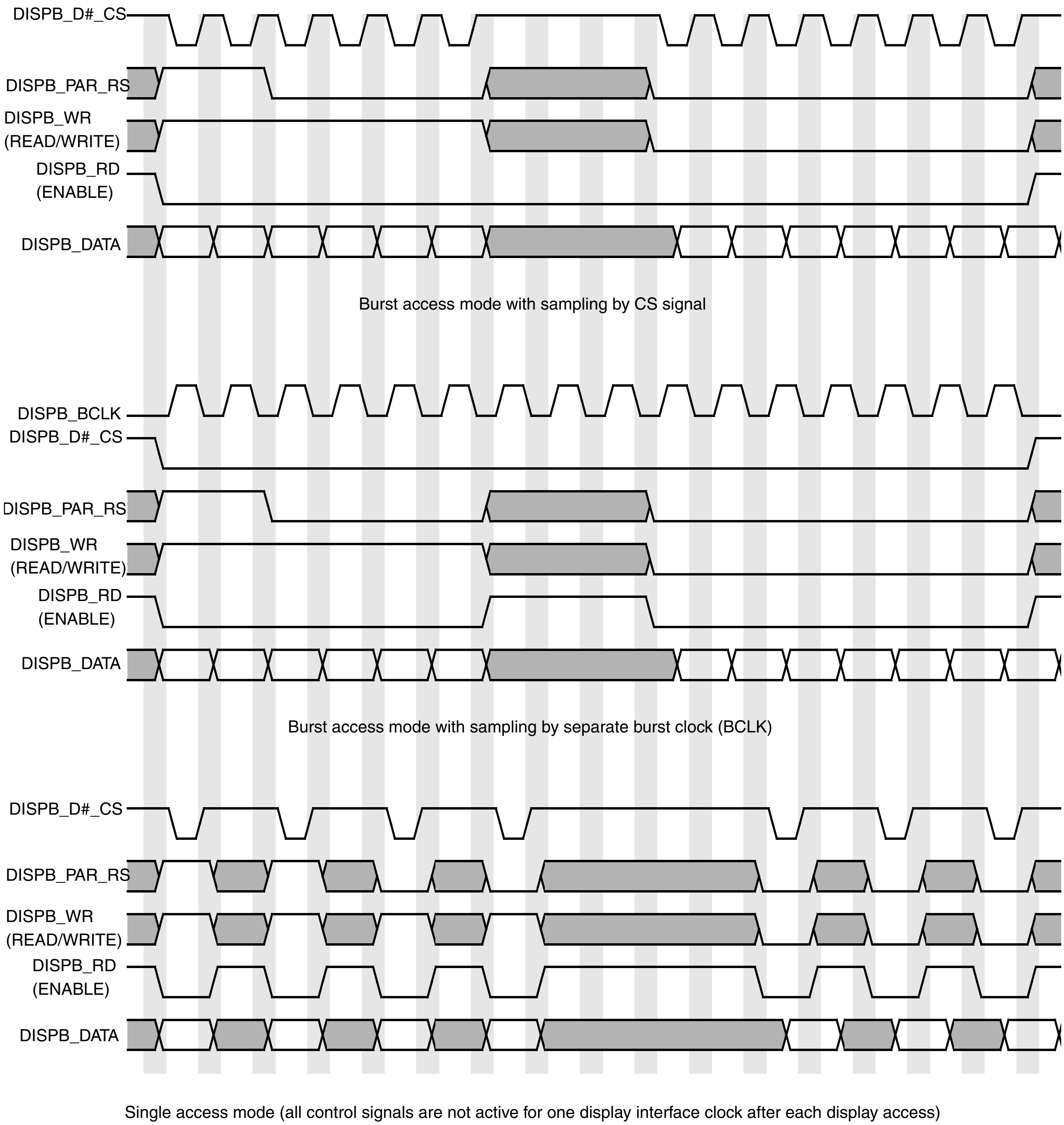

Figure 54. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

4.3.16 Memory Stick Host Controller (MSHC)

Figure 66, Figure 67, and Figure 68 depict the MSHC timings, and Table 52 and Table 53 list the timing parameters.

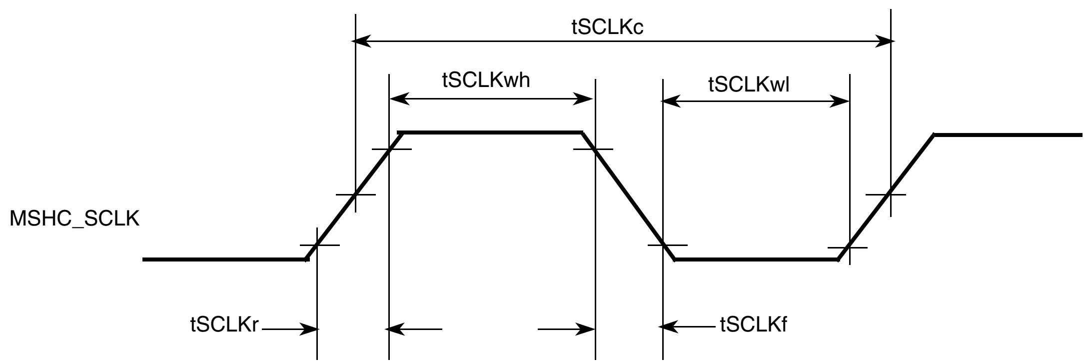

Figure 66. MSHC_CLK Timing Diagram

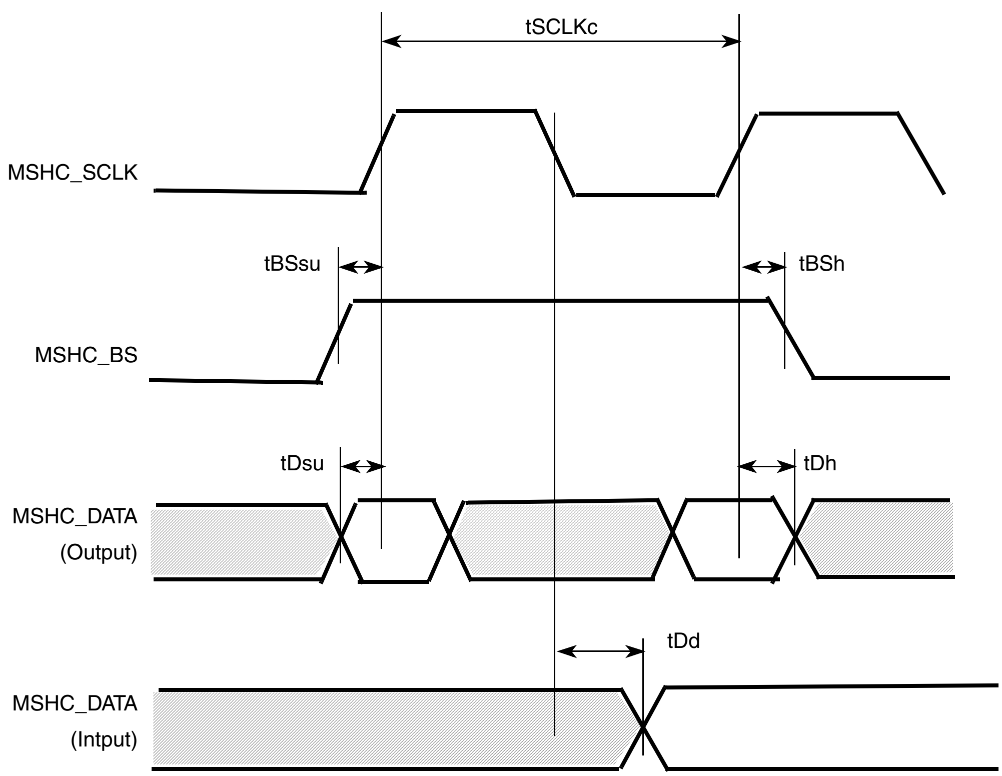

Figure 67. Transfer Operation Timing Diagram (Serial)

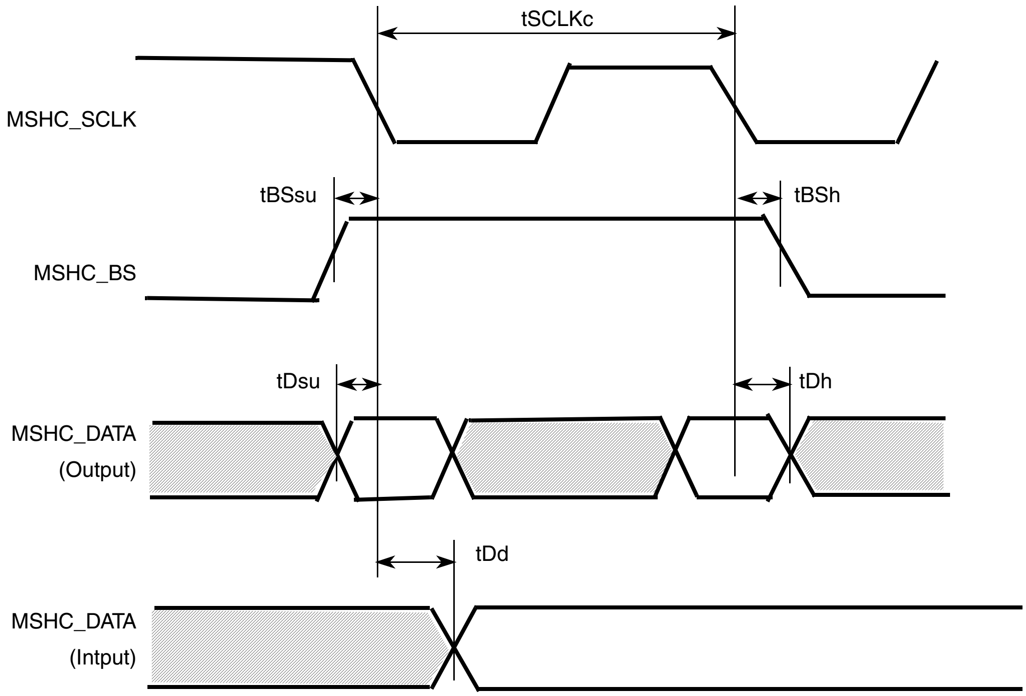

Figure 68. Transfer Operation Timing Diagram (Parallel)

NOTE

The Memory Stick Host Controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications* document. Tables in this section details the specifications requirements for parallel and serial modes, and not the MCIMX31 timing.

Table 52. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

[1] Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 8, "Operating Ranges," on page 13.

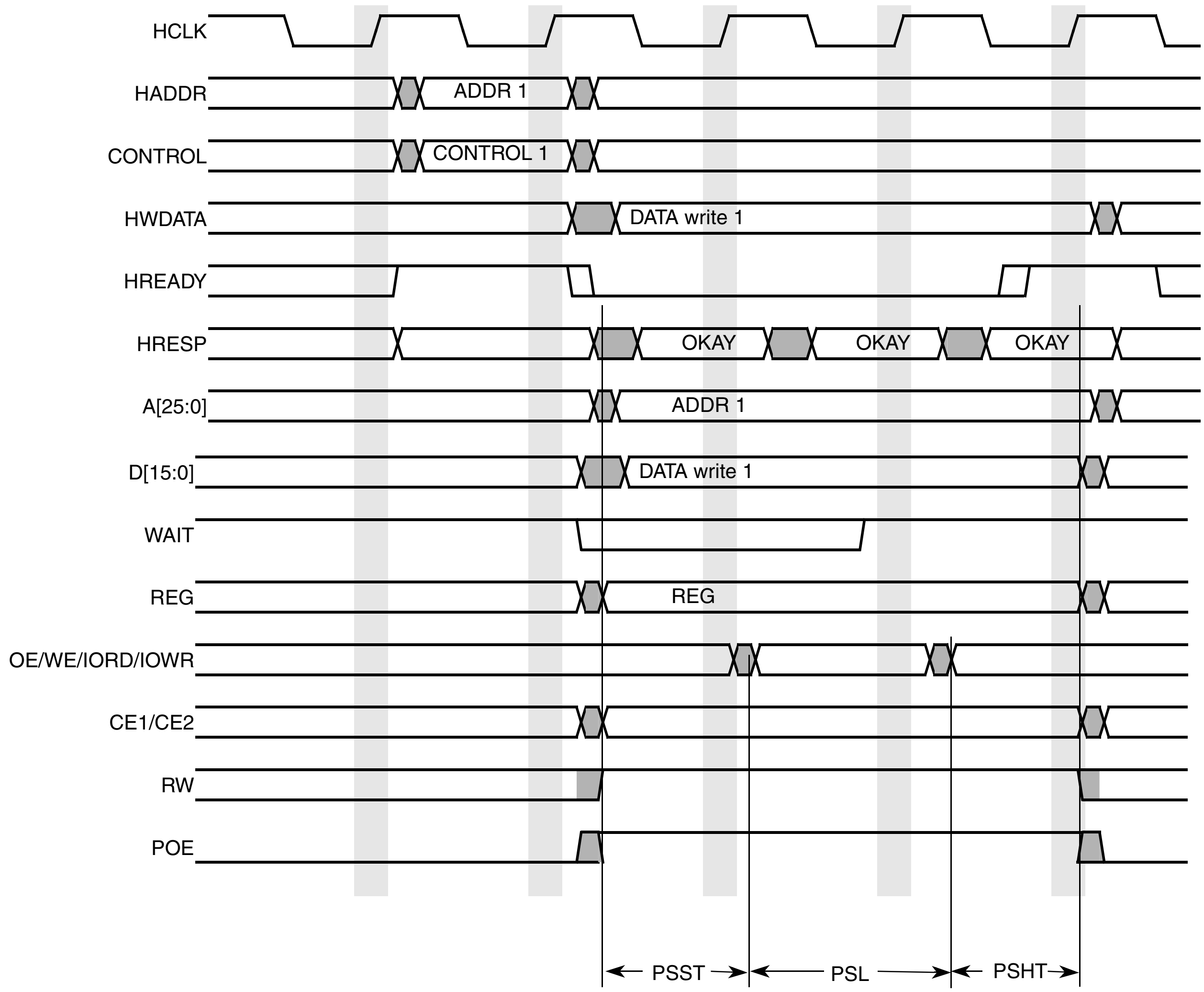

Figure 69. Write Accesses Timing Diagram—PSHT=1, PSST=1

4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 77 depicts the SJC test clock input timing. Figure 78 depicts the SJC boundary scan timing, Figure 79 depicts the SJC test access port, Figure 80 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 59 lists the SJC timing parameters.

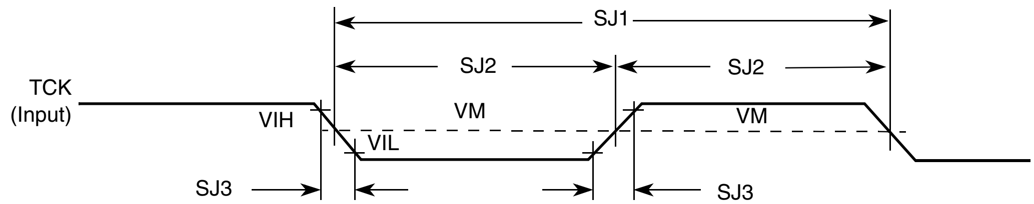

Figure 77. Test Clock Input Timing Diagram

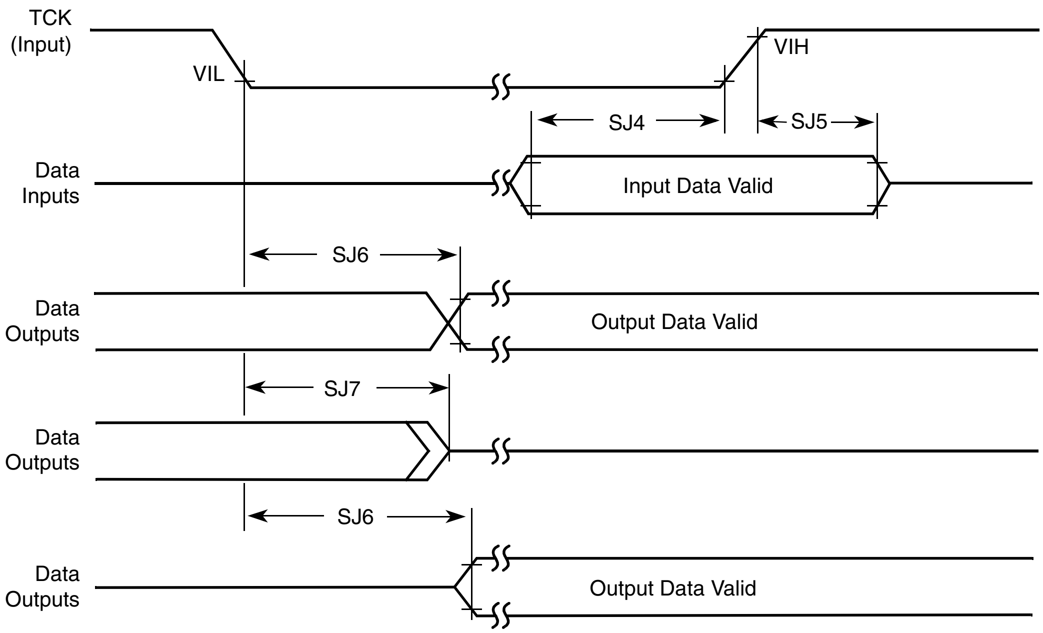

Figure 78. Boundary Scan (JTAG) Timing Diagram

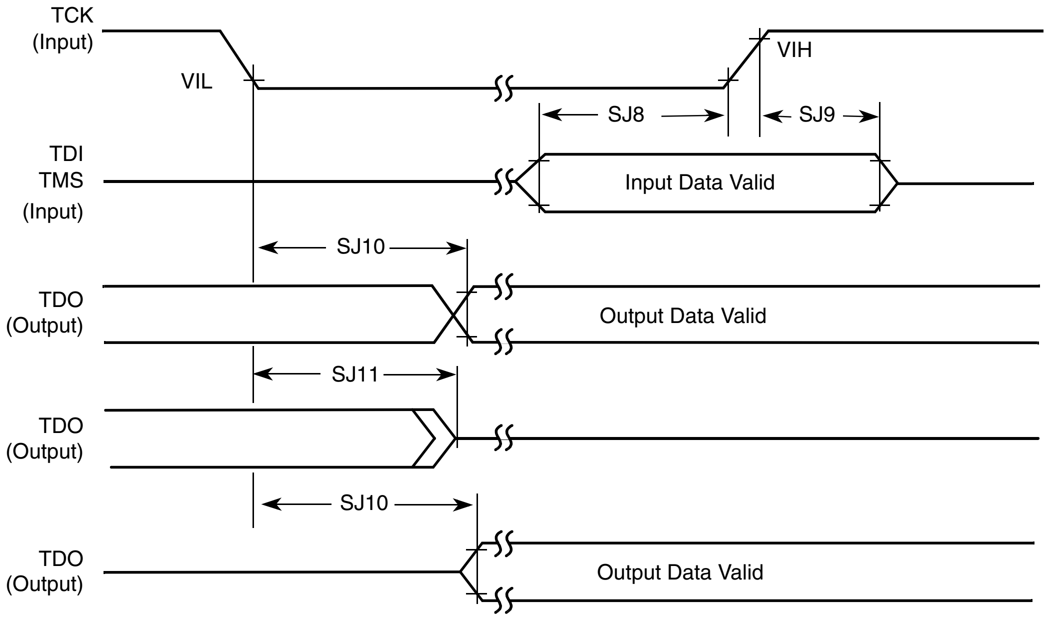

Figure 79. Test Access Port Timing Diagram

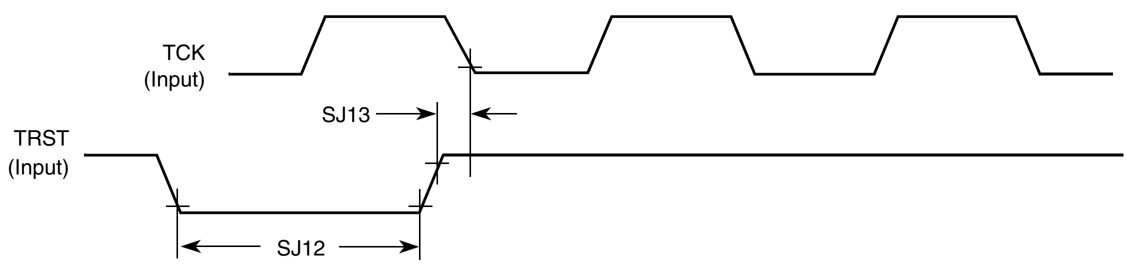

Figure 80. $\overline{\text{TRST}}$ Timing Diagram

Table 59. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min	Max	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

Table 63. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 85 depicts the USB ULPI timing diagram, and Table 64 lists the timing parameters.

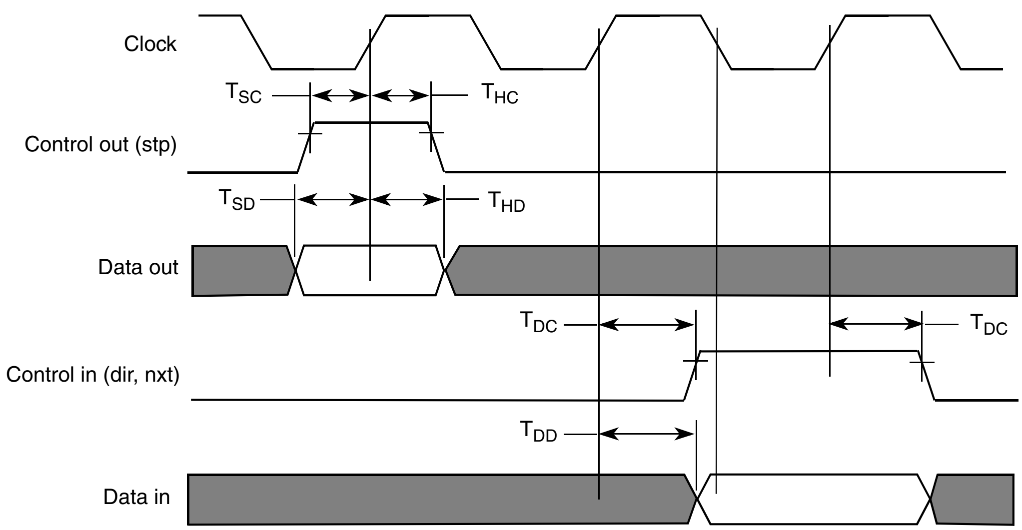

Figure 85. USB ULPI Interface Timing Diagram

Table 64. USB ULPI Interface Timing Specification[1]

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	TSC, TSD	6	—	ns
Hold time (control in, 8-bit data in)	THC, THD	0	—	ns
Output delay (control out, 8-bit data out)	TDC, TDD	—	9	ns

1 Timing parameters are given as viewed by transceiver side.

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
CSPI3_SCLK	E1
CSPI3_SPI_RDY	G6
CTS1	B11
CTS2	G13
D0	AB2
D1	Y3
D10	Y1
D11	U7
D12	W2
D13	V3
D14	W1
D15	U6
D2	AB1
D3	W6
D3_CLS	R20
D3_REV	T26
D3_SPL	U25
D4	AA2
D5	V7
D6	AA1
D7	W3
D8	Y2
D9	V6
DCD_DCE1	B12
DCD_DTE1	B13
$\overline{\text{DE}}$	C18
DQM0	AE19
DQM1	AD19
DQM2	AA20
DQM3	AE18
DRDY0	N26
DSR_DCE1	A11
DSR_DTE1	A12
DTR_DCE1	C11
DTR_DCE2	F12
DTR_DTE1	C12
DVFS0	E25
DVFS1	G24
EB0	W21
EB1	Y24
ECB	AD23
FPSHIFT	N21
GPIO1_0	F18
GPIO1_1	B23
GPIO1_2	C20
LD7	W25

Signal ID	Ball Location
GPIO1_3	F25
GPIO1_4	F19
GPIO1_5 (PWR RDY)	B24
GPIO1_6	A23
GPIO3_0	K21
GPIO3_1	H26
HSYNC	N25
I2C_CLK	J24
I2C_DAT	H25
IOIS16	J3
KEY_COL0	C15
KEY_COL1	B17
KEY_COL2	G15
KEY_COL3	A17
KEY_COL4	C16
KEY_COL5	B18
KEY_COL6	F15
KEY_COL7	A18
KEY_ROW0	F13
KEY_ROW1	B15
KEY_ROW2	C14
KEY_ROW3	A15
KEY_ROW4	G14
KEY_ROW5	B16
KEY_ROW6	F14
KEY_ROW7	A16
L2PG	See VPG1
LBA	AE22
LCS0	P26
LCS1	P21
LD0	T24
LD1	U26
LD10	V24
LD11	Y25
LD12	Y26
LD13	V21
LD14	AA25
LD15	W24
LD16	AA26
LD17	V20
LD2	T21
LD3	V25
LD4	T20
LD5	V26
LD6	U24
SCK6	T2

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
SDCLK	AA21
$\overline{\text{SDCLK}}$	AE20
SDQS0	AD16
SDQS1	AE12
SDQS2	AD11
SDQS3	AD8
SDWE	AF20
SER_RS	T25
SFS3	R6
SFS4	F3
SFS5	A3
SFS6	T3
SIMPD0	G17
SJC_MOD	A20
SRST0	C19
SRX0	B21
SRXD3	R3
SRXD4	C3
SRXD5	B4
SRXD6	R7
STX0	F17
STXD3	R1
STXD4	B3
STXD5	C5
STXD6	T1
SVEN0	A21
TCK	B19
TDI	F16
TDO	A19
TMS	G16

Signal ID	Ball Location
TXD1	F10
TXD2	C13
USB_BYP	A9
USB_OC	C10
USB_PWR	B10
USBH2_CLK	N1
USBH2_DATA0	M1
USBH2_DATA1	M3
USBH2_DIR	N7
USBH2_NXT	N6
USBH2_STP	M2
USBOTG_CLK	G10
USBOTG_DATA0	F9
USBOTG_DATA1	B8
USBOTG_DATA2	G9
USBOTG_DATA3	A7
USBOTG_DATA4	C8
USBOTG_DATA5	B7
USBOTG_DATA6	F8
USBOTG_DATA7	A6
USBOTG_DIR	B9
USBOTG_NXT	A8
USBOTG_STP	C9
VPG0	G25
VPG1	J20
VSTBY	F26
VSYNC0	N24
VSYNC3	R26
WATCHDOG_RST	A24
WRITE	R25