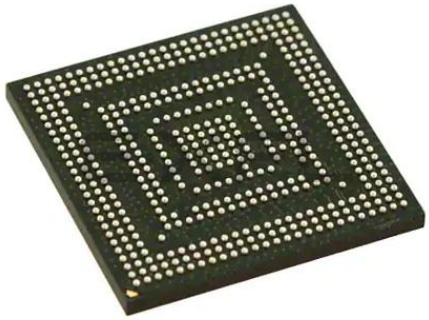

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31lvkn5br2

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
Fusebox	Fusebox	ROM	The Fusebox is a ROM that is factory configured by Freescale.	4.3.12/55 See also Table 11
GPIO	General Purpose I/O Module	Pins	The GPIO provides several groups of 32-bit bidirectional, general purpose I/O. This peripheral provides dedicated general-purpose signals that can be configured as either inputs or outputs.	—
GPT	General Purpose Timer	Timer Peripheral	The GPT is a multipurpose module used to measure intervals or generate periodic output.	—
GPU	Graphics Processing Unit	Multimedia Peripheral	The GPU provides hardware acceleration for 2D and 3D graphics algorithms.	—
I^2C	Inter IC Communication	Connectivity Peripheral	The I^2C provides serial interface for controlling the Sensor Interface and other external devices. Data rates of up to 100 Kbits/s are supported.	4.3.13/56
IIM	IC Identification Module	ID	The IIM provides an interface for reading device identification.	—
IPU	Image Processing Unit	Multimedia Peripheral	The IPU processes video and graphics functions in the MCIMX31 and interfaces to video, still image sensors, and displays.	4.3.14/57, 4.3.15/59
KPP	Keypad Port	Connectivity Peripheral	The KPP is used for keypad matrix scanning or as a general purpose I/O. This peripheral simplifies the software task of scanning a keypad matrix.	—
MPEG-4	MPEG-4 Video Encoder	Multimedia Peripherals	The MPEG-4 encoder accelerates video compression, following the MPEG-4 standard	—
MSHC	Memory Stick Host Controller	Connectivity Peripheral	The MSHC is placed in between the AIPS and the customer memory stick to support data transfer from the MCIMX31 to the customer memory stick.	4.3.16/84
PADIO	Pads I/O	Buffers and Drivers	The PADIO serves as the interface between the internal modules and the device's external connections.	4.3.1/22
PCMCIA	PCM	Connectivity Peripheral	The PCMCIA Host Adapter provides the control logic for PCMCIA socket interfaces.	4.3.17/86
PWM	Pulse-Width Modulator	Timer Peripheral	The PWM has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones.	4.3.18/88
RNGA	Random Number Generator Accelerator	Security	The RNGA module is a digital integrated circuit capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 standards for randomness and non-determinism.	—
RTC	Real Time Clock	Timer Peripheral	The RTC module provides a current stamp of seconds, minutes, hours, and days. Alarm and timer functions are also available for programming. The RTC supports dates from the year 1980 to 2050.	—
RTIC	Run-Time Integrity Checkers	Security	The RTIC ensures the integrity of the peripheral memory contents and assists with boot authentication.	—

Table 6 provides the thermal resistance data for the 14 × 14 mm, 0.5 mm pitch package.

Table 6. Thermal Resistance Data—14 × 14 mm Package

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (natural convection)	Single layer board (1s)	$R_{\theta JA}$	56	°C/W	1, 2, 3
Junction to Ambient (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	30	°C/W	1, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	46	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	26	°C/W	1, 3
Junction to Board	—	$R_{\theta JB}$	17	°C/W	1, 4
Junction to Case	—	$R_{\theta JC}$	10	°C/W	1, 5
Junction to Package Top (natural convection)	—	Ψ_{JT}	2	°C/W	1, 6

NOTES

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 7 provides the thermal resistance data for the 19 × 19 mm, 0.8 mm pitch package.

Table 7. Thermal Resistance Data—19 × 19 mm Package

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (natural convection)	Single layer board (1s)	$R_{\theta JA}$	46	°C/W	1, 2, 3
Junction to Ambient (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	29	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	38	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	25	°C/W	1, 2, 3
Junction to Board	—	$R_{\theta JB}$	19	°C/W	1, 3
Junction to Case (Top)	—	$R_{\theta JCtop}$	10	°C/W	1, 4
Junction to Package Top (natural convection)	—	Ψ_{JT}	2	°C/W	1, 5

NOTES

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Fusebox Supply Current Parameters

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	eFuse Program Current.[1] Current to program one eFuse bit: efuse_pgm = 3.0 V	$I_{program}$	—	35	60	mA
2	eFuse Read Current[2] Current to read an 8-bit eFuse word vdd_fusebox = 1.875 V	I_{read}	—	5	8	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word, and only applies to Silicon Rev. 1.2 and previous.

Table 15. GPIO DC Electrical Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low-level output current, slow slew rate	I_{OL_S}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive	 2 4 8	—	—	mA
Low-level output current, fast slew rate	I_{OL_F}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive	 4 6 8	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	—	NVCC	V
Low-Level DC input voltage	V_{IL}	—	0	—	0.3*QVCC	V
Input Hysteresis	V_{HYS}	Hysteresis enabled	0.25	—	—	V
Schmitt trigger VT+	V_T+	Hysteresis enabled	0.5*QVCC	—	—	V
Schmitt trigger VT–	V_T-	Hysteresis enabled	—	—	0.5*QVCC	V
Pull-up resistor (100 kΩ PU)	R_{PU}	—	—	100	—	kΩ
Pull-down resistor (100 kΩ PD)	R_{PD}	—	—	100	—	
Input current (no PU/PD)	I_{IN}	V_I = NVCC or GND	—	—	±1	µA
Input current (100 kΩ PU)	I_{IN}	V_I = 0 V_I = NVCC	—	—	25 0.1	µA µA
Input current (100 kΩ PD)	I_{IN}	V_I = 0 V_I = NVCC	—	—	0.25 28	µA µA
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

The MCIMX31 I/O parameters appear in Table 16 for DDR (Double Data Rate). See Table 8, "Operating Ranges," on page 13 for temperature and supply voltage ranges.

NOTE

NVCC for Table 16 refers to NVCC2, NVCC21, and NVCC22.

Table 16. DDR (Double Data Rate) I/O DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	I_{OH} = –1 mA	NVCC –0.12	—	—	V
		I_{OH} = specified Drive	0.8*NVCC	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA	—	—	0.08	V
		I_{OL} = specified Drive	—	—	0.2*NVCC	V
High-level output current	I_{OH}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 –3.6 –7.2 –10.8 –14.4	—	—	mA

4.3.5.4 UDMA Out Timing

Figure 18 shows timing when the UDMA out transfer starts, Figure 19 shows timing when the UDMA out host terminates transfer, Figure 20 shows timing when the UDMA out device terminates transfer, and Table 29 lists the timing parameters for UDMA out burst.

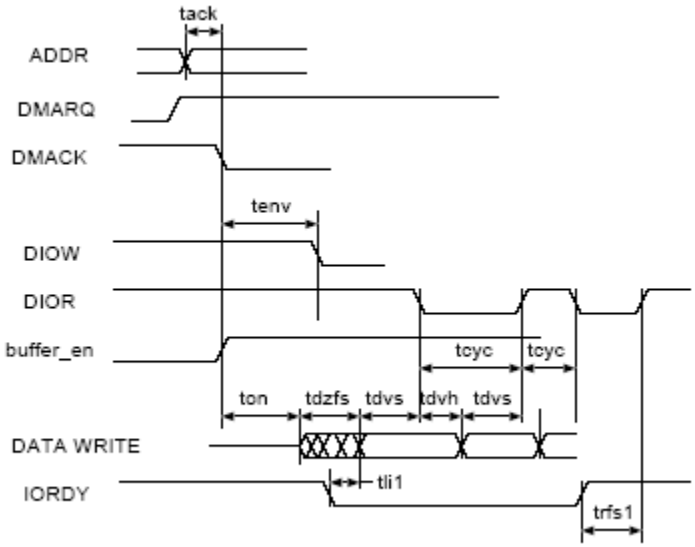

Figure 18. UDMA Out Transfer Starts Timing Diagram

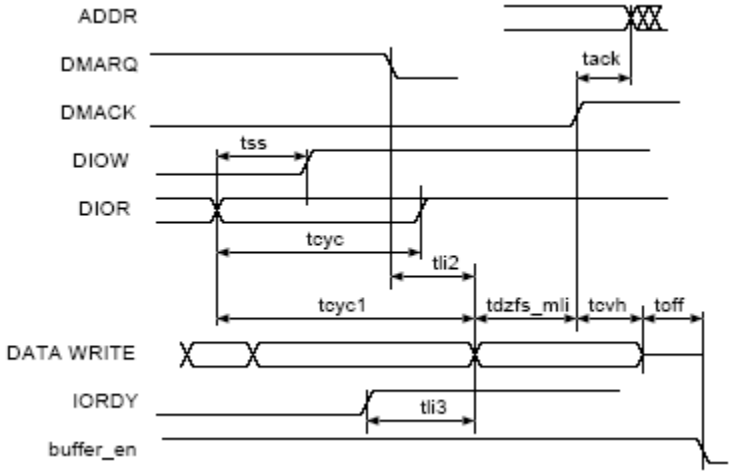

Figure 19. UDMA Out Host Terminates Transfer Timing Diagram

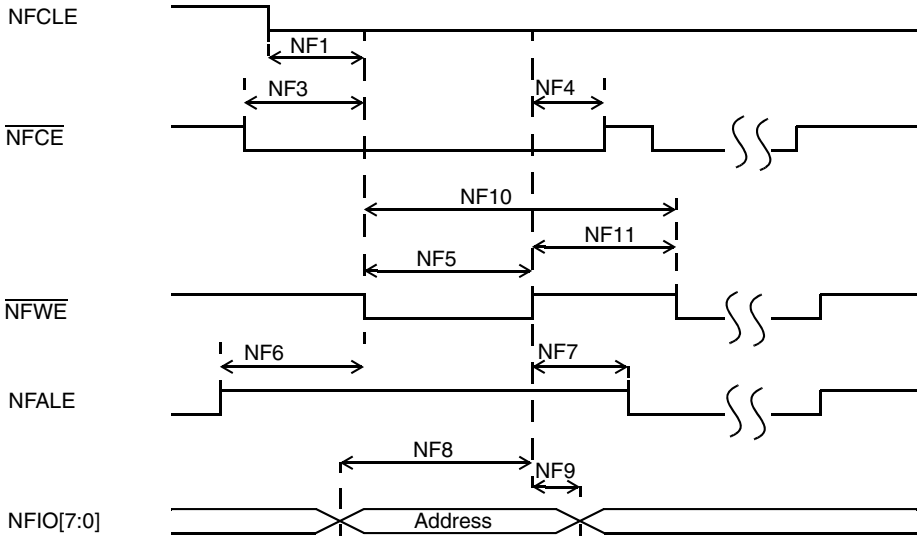

Figure 24. Address Latch Cycle Timing Diagram

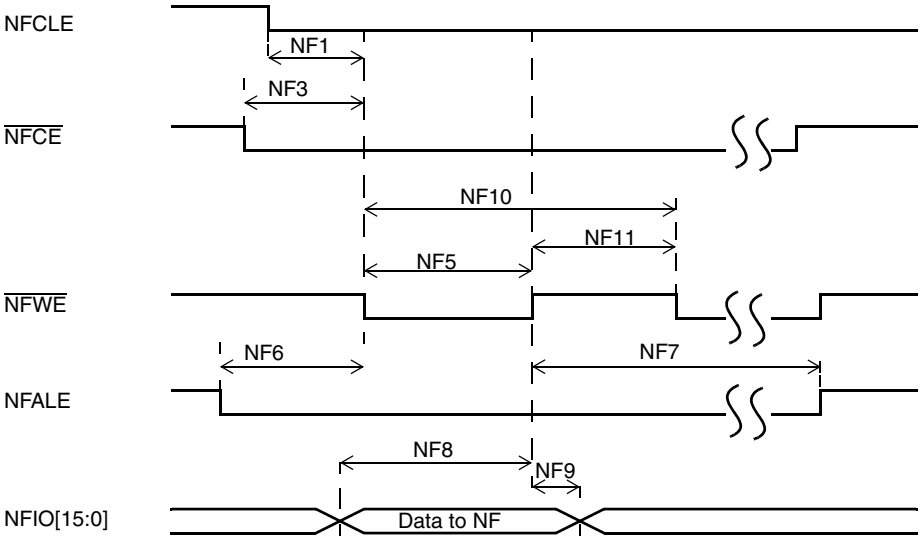

Figure 25. Write Data Latch Cycle Timing Diagram

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.3.9.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 27 depicts the timing of the WEIM module, and Table 33 lists the timing parameters.

Table 34. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD9	Data out hold time[1]	tOH	1.8	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 38 and Table 39.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 34 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

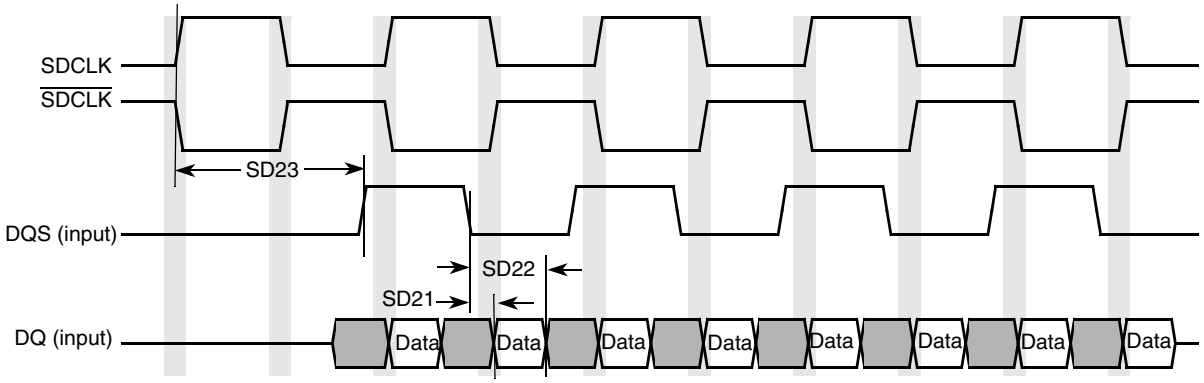

Figure 39. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 39. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 39 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.10 ETM Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a TPA that supports TRACECLK frequencies up to 133 MHz.

Figure 40 depicts the TRACECLK timings of ETM, and Table 40 lists the timing parameters.

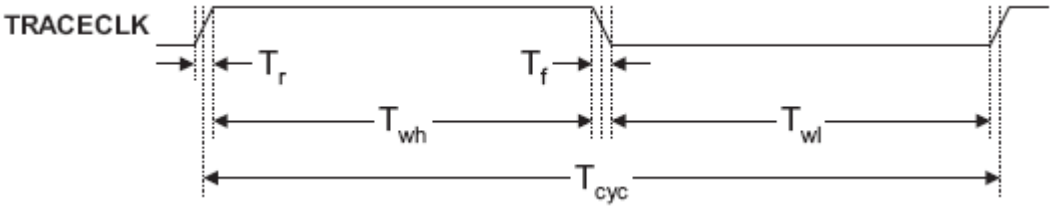

Figure 40. ETM TRACECLK Timing Diagram

4.3.14 IPU—Sensor Interfaces

4.3.14.1 Supported Camera Sensors

Table 44 lists the known supported camera sensors at the time of publication.

Table 44. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI–SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors not validated at time of publication.

4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

Table 46. Supported Display Components[1]

Type	Vendor	Model
TFT displays (memory-less)	Sharp (HR-TFT Super Mobile LCD family)	LQ035Q7 DB02, LM019LC1Sxx
	Samsung (QCIF and QVGA TFT modules for mobile phones)	LTS180S1-HF1, LTS180S3-HF1, LTS350Q1-PE1, LTS350Q1-PD1, LTS220Q1-HE1[2]
	Toshiba (LTM series)	LTM022P806[2], LTM04C380K[2], LTM018A02A[2], LTM020P332[2], LTM021P337[2], LTM019P334[2], LTM022A783[2], LTM022A05ZZ[2]
	NEC	NL6448BC20-08E, NL8060BC31-27
Display controllers	Epson	S1D15xxx series, S1D19xxx series, S1D13713, S1D13715
	Solomon Systech	SSD1301 (OLED), SSD1828 (LDCD)
	Hitachi	HD66766, HD66772
	ATI	W2300
Smart display modules	Epson	L1F10043 T[2], L1F10044 T[2], L1F10045 T[2], L2D22002[2], L2D20014[2], L2F50032[2], L2D25001 T[2]
	Hitachi	120 160 65K/4096 C-STN (#3284 LTD-1398-2) based on HD 66766 controller
	Densitron Europe LTD	All displays with MPU 80/68K series interface and serial peripheral interface
	Sharp	LM019LC1Sxx
	Sony	ACX506AKM
Digital video encoders (for TV)	Analog Devices	ADV7174/7179
	Crystal (Cirrus Logic)	CS49xx series
	Focus	FS453/4

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only display component suppliers.

2 These display components not validated at time of publication.

4.3.15.2 Synchronous Interfaces

4.3.15.2.1 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 46 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.

4.3.15.4.2 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics."

4.3.15.5 Asynchronous Interfaces

4.3.15.5.1 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock. The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) of by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals changes only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k) and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK. In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode. In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 52, Figure 53, Figure 54, and Figure 55. These timing images correspond to active-low DISPB_D#_CS, DISPB_D#_WR and DISPB_D#_RD signals.

Additionally, the IPU allows a programmable pause between two burst. The pause is defined in the HSP_CLK cycles. It allows to avoid timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

4.3.16 Memory Stick Host Controller (MSHC)

Figure 66, Figure 67, and Figure 68 depict the MSHC timings, and Table 52 and Table 53 list the timing parameters.

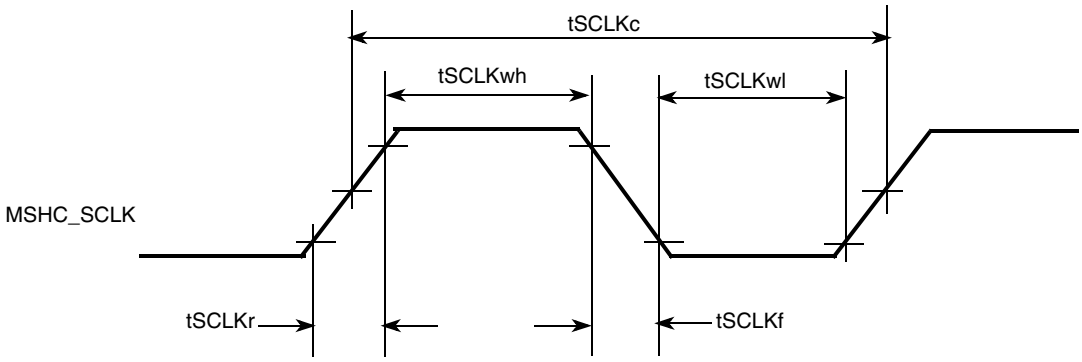

Figure 66. MSHC_CLK Timing Diagram

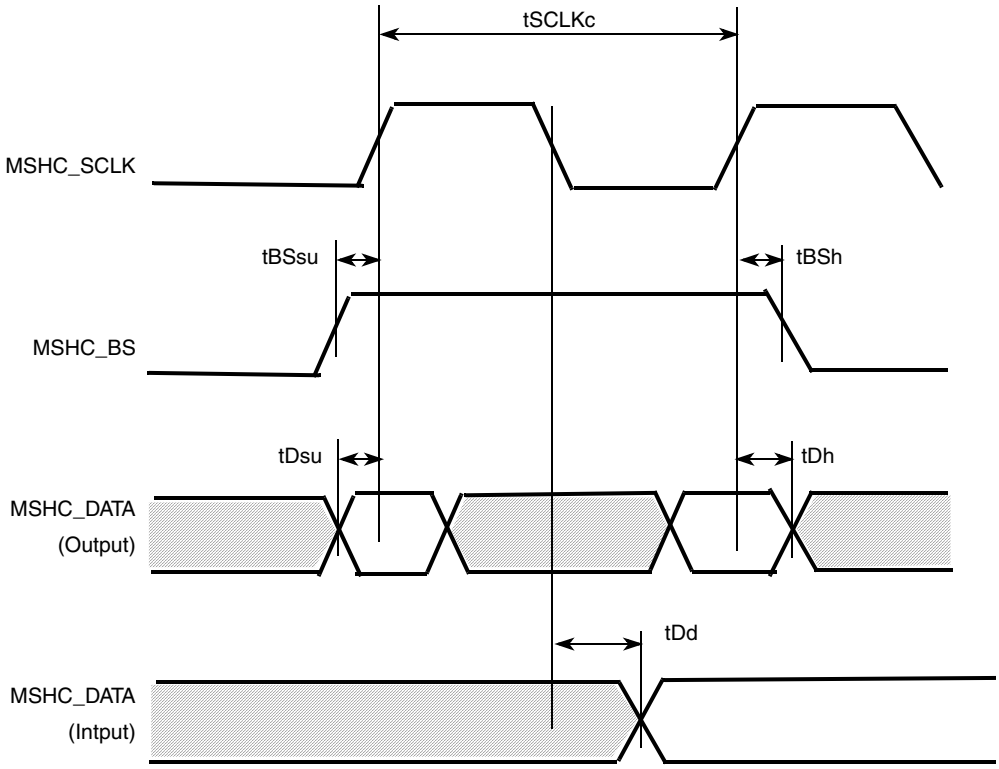

Figure 67. Transfer Operation Timing Diagram (Serial)

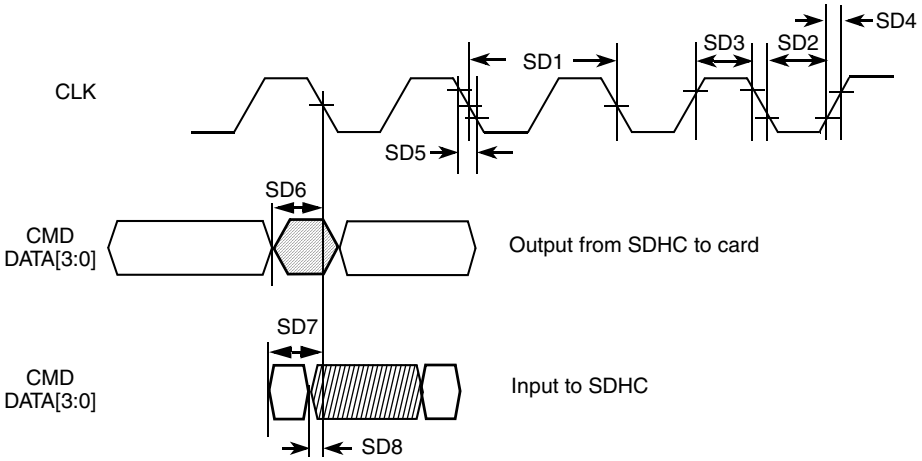

Figure 72. SDHC Timing Diagram

Table 56. SDHC Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed)	f_{PP}[2]	0	25	MHz
	Clock Frequency (MMC Full Speed)	f_{PP}[3]	0	20	MHz
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz
SD2	Clock Low Time	t_{WL}	10	—	ns
SD3	Clock High Time	t_{WH}	10	—	ns
SD4	Clock Rise Time	t_{TLH}	—	10	ns
SD5	Clock Fall Time	t_{THL}	—	10	ns
SDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	SDHC output delay	t_{ODL}	–6.5	3	ns
SDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	SDHC input setup	t_{IS}	—	18.5	ns
SD8	SDHC input hold	t_{IH}	—	–11.5	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 V–3.3 V.
2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 MHz–25 MHz.
3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 MHz–20 MHz.
4 In card identification mode, card clock must be 100 kHz–400 kHz, voltage ranges from 2.7 V–3.3 V.

4.3.20 SIM Electrical Specifications

Each SIM card interface consist of a total of 12 pins (for 2 separate ports of 6 pins each. Mostly one port with 5 pins is used).

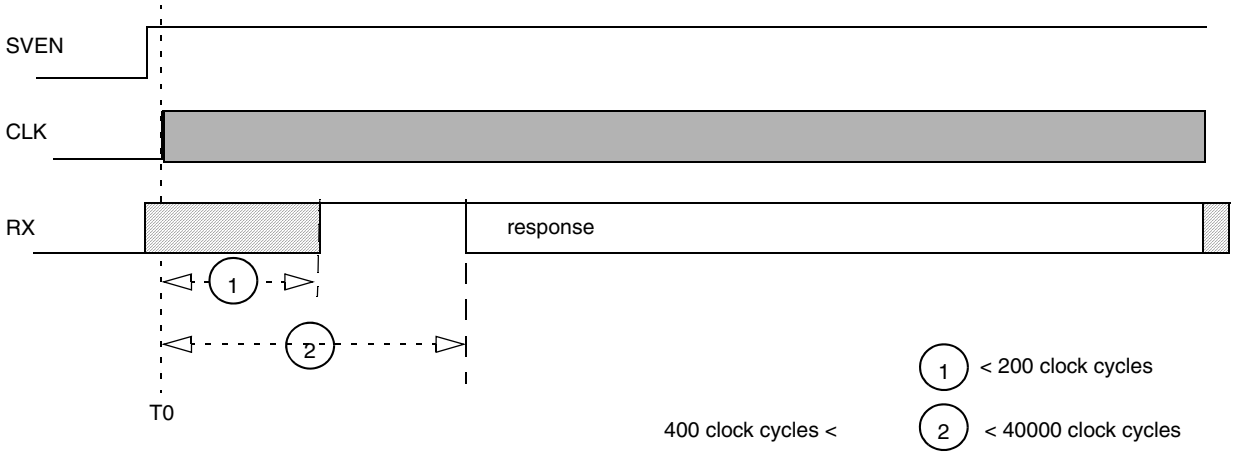

Figure 74. Internal-Reset Card Reset Sequence

4.3.20.2.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 75):

1. After powerup, the clock signal is enabled on CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
4. RST is set High (time T1)
5. RST must remain High for at least 40000 clock cycles after T1 and a response must be received on RX between 400 and 40000 clock cycles after T1.

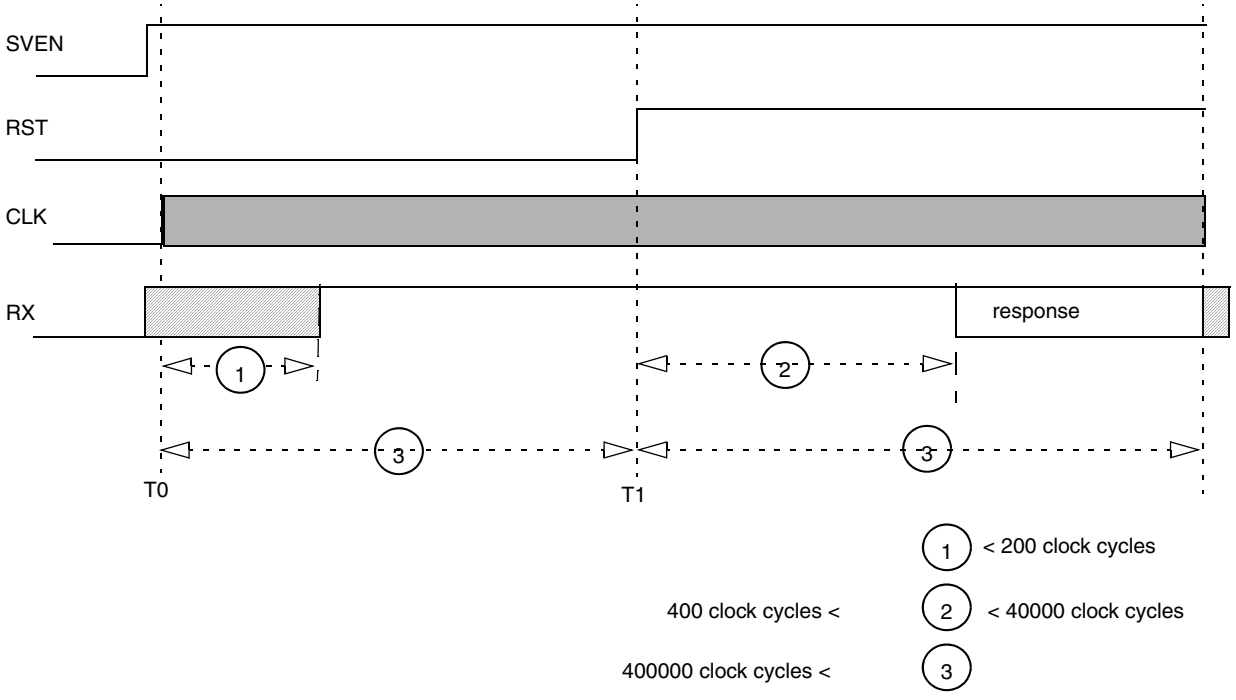

Figure 75. Active-Low-Reset Card Reset Sequence

Table 60. SSI Transmitter with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6	ns
SS15	(Tx/Rx) Internal FS fall time	—	6	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0	—	ns
SS52	Loading	—	25	pF

5.2.2 MAPBGA Signal Assignment–19 × 19 mm 0.8 mm

See Table 71 for the 19 × 19 mm, 0.8 mm pitch signal assignments/ball map.

5.2.3 Connection Tables–19 x 19 mm 0.8 mm

Table 67 shows the device connection list for power and ground, alpha-sorted followed by Table 68, which shows the no-connects. Table 69 shows the device connection list for signals.

5.2.3.1 Ground and Power ID Locations—19 x 19 mm 0.8 mm

Table 67. 19 x 19 BGA Ground/Power ID by Ball Grid Location

GND/PWR ID	Ball Location
FGND	U16
FUSE_VDD	T15
FVCC	T16
GND	A1, A2, A3, A21, A22, A23, B1, B2, B22, B23, C1, C2, C22, C23, D22, D23, J12, J13, K10, K11, K12, K13, K14, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14, R12, Y1, Y23, AA1, AA2, AA22, AA23, AB1, AB2, AB21, AB22, AB23, AC1, AC2, AC21, AC22, AC23
IOQVDD	T8
MGND	U14
MVCC	U15
NVCC1	G15, G16, H16, J17
NVCC2	N16, P16, R15, R16, T14
NVCC3	K7, K8, L7, L8
NVCC4	H14, J15, K15
NVCC5	G9, G10, H8, H9
NVCC6	G11, G12, G13, H12
NVCC7	H15, J16, K16, L16, M16
NVCC8	H10, H11, J11
NVCC9	G14
NVCC10	P8, R7, R8, R9, T9
NVCC21	T11, T12, T13, U11
NVCC22	T10, U7, U8, U9, U10, V6, V7, V8, V9, V10
QVCC	H13, J14, L15, M15, N9, N15, P9, P15, R10, R11, R13, R14
QVCC1	J8, J9, J10, K9
QVCC4	L9, M7, M8, N8
SGND	U13
SVCC	U12
UVCC	P18
UGND	P17

Table 73. Product Differentiation (continued)

Item	Location	MCIMX31/MCIMX31L	MCIMX31C/MCIMX31LC
GPIO maximum input current (100 kΩ PU)	Table 15, "GPIO DC Electrical Parameters," on page 22	V_I = 0, I_{IN} = 25 μA V_I = NVCC, I_{IN} = 0.1 μA	N/A N/A
Core operating speed	Table 8, "Operating Ranges," on page 13	532 MHz	400 MHz
Package	Table 70, "Ball Map—14 x 14 0.5 mm Pitch," on page 117 and Table 71, "Ball Map—19 x 19 0.8 mm Pitch," on page 118	MAPBGA Packages 457 14 x 14 mm, 0.5 mm Pitch 473 19 x 19 mm, 0.8 mm Pitch	MAPBGA Package 473 19 x 19 mm, 0.8 mm Pitch
Pin Assignment	Table 66, "14 x 14 BGA Signal ID by Ball Grid Location," on page 107 and Table 69, "19 x 19 BGA Signal ID by Ball Grid Location," on page 113	MAPBGA Packages 457 14 x 14 mm, 0.5 mm Pitch 473 19 x 19 mm, 0.8 mm Pitch	MAPBGA Package 473 19 x 19 mm, 0.8 mm Pitch

7 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

MCIMX31 Product Brief (order number MCIMX31PB)

MCIMX31 Reference Manual (order number MCIMX31RM)

MCIMX31 Chip Errata (order number MCIMX31CE)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. ARM Ltd. documentation is available from http://www.arm.com.

8 Revision History

Table 74 summarizes revisions to this document since the release of Rev. 3.4.

Table 74. Revision History

Rev.	Location	Revision
4	Figure 87, Table 73	Updated.
4.1	Table 1, "Ordering Information," on page 3	Added note about JTAG compliance.
4.1	Section 1.2.1/3	Updated with new operating frequencies
4.1	Table 8, "Operating Ranges," on page 13	Added new operating frequencies

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