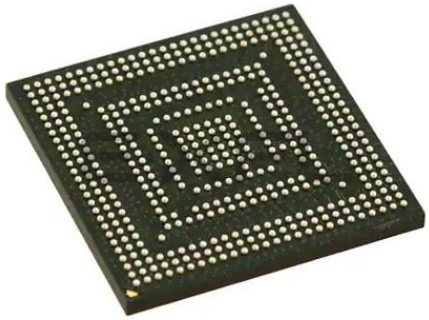

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx31lvkn5c

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31.

Table 1. Ordering Information

Part Number	Silicon Revision[1, 2, 3,4]	Device Mask	Operating Temperature Range (°C)	Package[5]
MCIMX31VKN5	1.15	2L38W and 3L38W	0 to 70	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LVKN5	1.15	2L38W and 3L38W	0 to 70	
MCIMX31VKN5B	1.2	M45G	0 to 70	
MCIMX31LVKN5B	1.2	M45G	0 to 70	
MCIMX31VKN5C	2.0	M91E	0 to 70	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LVKN5C	2.0	M91E	0 to 70	
MCIMX31CVKN5C	2.0	M91E	–40 to 85	
MCIMX31LCVKN5C	2.0	M91E	–40 to 85	
MCIMX31VMN5C	2.0	M91E	0 to 70	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LVMN5C	2.0	M91E	0 to 70	

1 Information on reading the silicon revision register can be found in the IC Identification (IIM) chapter of the Reference Manual, see Section 7, "Product Documentation."

2 Errata and fix information of the various mask sets can be found in the standard MCIMX31 Chip Errata, see Section 7, "Product Documentation."

3 Changes in output buffer characteristics can be found in the I/O Setting Exceptions and Special Pad Descriptions table in the Reference Manual, see Section 7, "Product Documentation."

4 JTAG functionality is not tested nor guaranteed at -40°C.

5 Case 1581 and 1931 are RoHS compliant, lead-free, MSL = 3, and solders at 260°C.

1.2.1 Feature Differences Between Mask Sets

The following is a summary of differences between silicon Revision 2.0, mask set M91E, and previous revisions of silicon. A complete list of these differences is given in Table 72.

- Extended operating temperature range is available: –40°C to 85°C
- Supply current information changes, as shown in Table 13 and Table 14
- FUSE_VDD supply voltage is floated or grounded during read operation
- No restriction on PLL versus core supply voltage
- Operating frequency as shown in Table 8.

4.1.1 Supply Current Specifications

Table 12 shows the core current consumption for 0°C to 70°C for Silicon Revision 1.2 and previous for the MCIMX31.

Table 12. Current Consumption for 0°C to 70°C[1, 2] for Silicon Revision 1.2 and Previous

Mode	Conditions	QVCC (Peripheral)		QVCC1 (ARM)		QVCC4 (L2)		FVCC + MVCC + SVCC + UVCC (PLL)		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
State Retention	• QVCC and QVCC1 = 0.95 V • L2 caches are power gated (QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.80	—	0.50	—	—	—	0.04	—	mA
Wait	• QVCC,QVCC1, and QVCC4 = 1.22 V • ARM is in wait for interrupt mode • MAX is active • L2 cache is stopped but powered • MCU PLL is on (532 MHz), VCC = 1.4 V • USB PLL and SPLL are off, VCC = 1.4 V • FPM is on • CKIH input is on • CAMP is on • 32 kHz input is on • All clocks are gated off • All modules are off (by programming CGR[2:0] registers) • RNGA oscillator is off • No external resistive loads	6.00	—	3.00	—	0.04	—	3.50	—	mA

1 Typical column: TA = 25°C

2 Maximum column: TA = 70°C

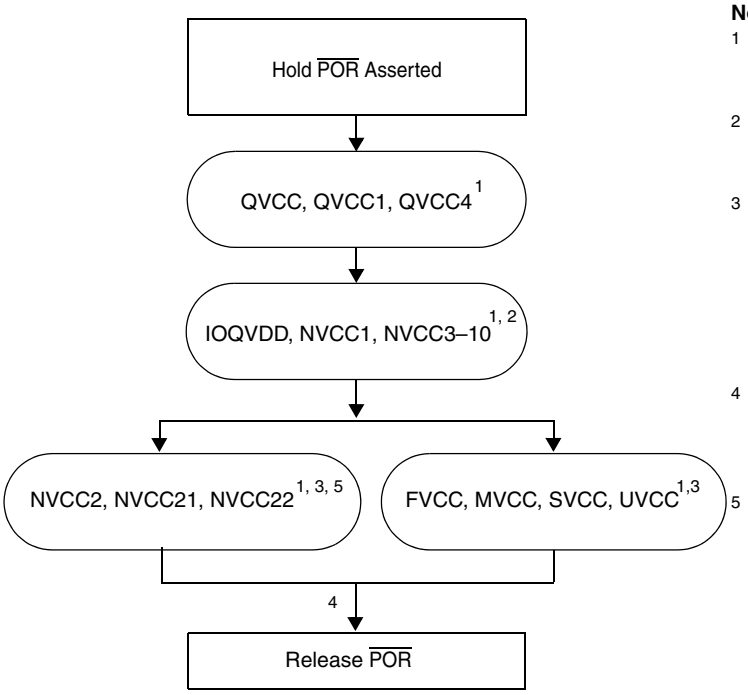
Table 13 shows the core current consumption for –40°C to 85°C for Silicon Revision 2.0 for the MCIMX31.

Table 13. Current Consumption for –40°C to 85°C[1, 2] for Silicon Revision 2.0

Mode	Conditions	QVCC (Peripheral)		QVCC1 (ARM)		QVCC4 (L2)		FVCC + MVCC + SVCC + UVCC (PLL)		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Deep Sleep	• QVCC = 0.95 V • ARM and L2 caches are power gated (QVCC1 = QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.16	5.50	—	—	—	—	0.02	0.10	mA
State Retention	• QVCC and QVCC1 = 0.95 V • L2 caches are power gated (QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.16	5.50	0.07	2.20	—	—	0.02	0.10	mA
Wait	• QVCC,QVCC1, and QVCC4 = 1.22 V • ARM is in wait for interrupt mode • MAX is active • L2 cache is stopped but powered • MCU PLL is on (532 MHz), VCC = 1.4 V • USB PLL and SPLL are off, VCC = 1.4 V • FPM is on • CKIH input is on • CAMP is on • 32 kHz input is on • All clocks are gated off • All modules are off (by programming CGR[2:0] registers) • RNGA oscillator is off • No external resistive loads	6.00	15.00	2.20	25.00	0.03	0.29	3.60	4.40	mA

1 Typical column: TA = 25°C

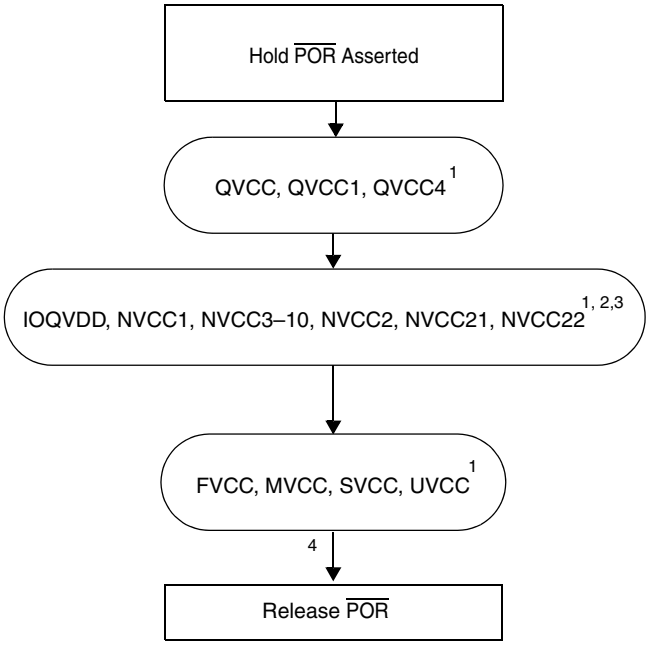
2 Maximum column: TA = 85°C



Notes:

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. The parallel paths in the flow indicate that supply group NVCC2, NVCC21, and NVCC22, and supply group FVCC, MVCC, SVCC, and UVCC ramp-ups are independent. Note that this power-up sequence is backward compatible to Silicon Revs. 1.15 and 1.2, because NVCC2x ramp-up proceeding PLL supplies is allowed.
4. Unlike the power-up sequence for Silicon Revision 1.2, FUSE_VDD should not be driven on power-up for Silicon Revision 2.0. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.
5. Raising IOQVDD before NVCC21 produces a slight increase in current drain on IOQVDD of approximately 3–5 mA. The current increase will not damage the IC. Refer to Errata ID TLSbo91750 for details.

Figure 3. Option 1 Power-Up Sequence (Silicon Revision 2.0)



Notes:

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. Raising NVCC2, NVCC21, and NVCC22 at the same time as IOQVDD does not produce the slight increase in current drain on IOQVDD (as described in Figure 3, Note 5).
4. Unlike the power-up sequence for Silicon Revision 1.2, FUSE_VDD should not be driven on power-up for Silicon Revision 2.0. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.

Figure 4. Option 2 Power-Up Sequence (Silicon Revision 2.0)

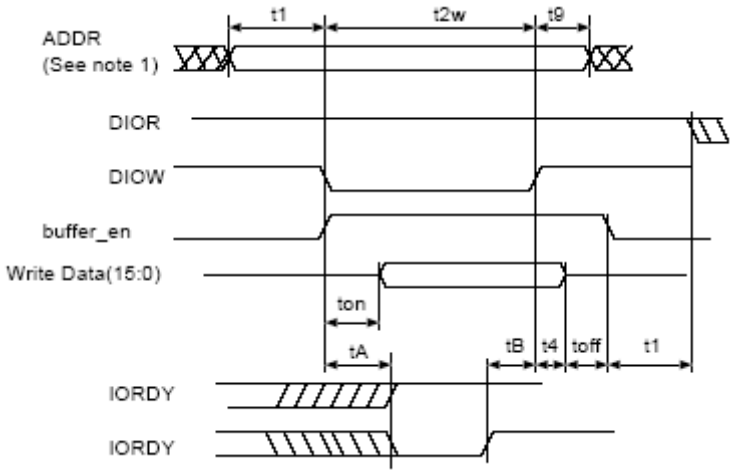


Figure 12. Multiword DMA (MDMA) Timing

Table 26. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 12	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w * T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 * T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 13 shows timing for MDMA read, Figure 14 shows timing for MDMA write, and Table 27 lists the timing parameters for MDMA read and write.

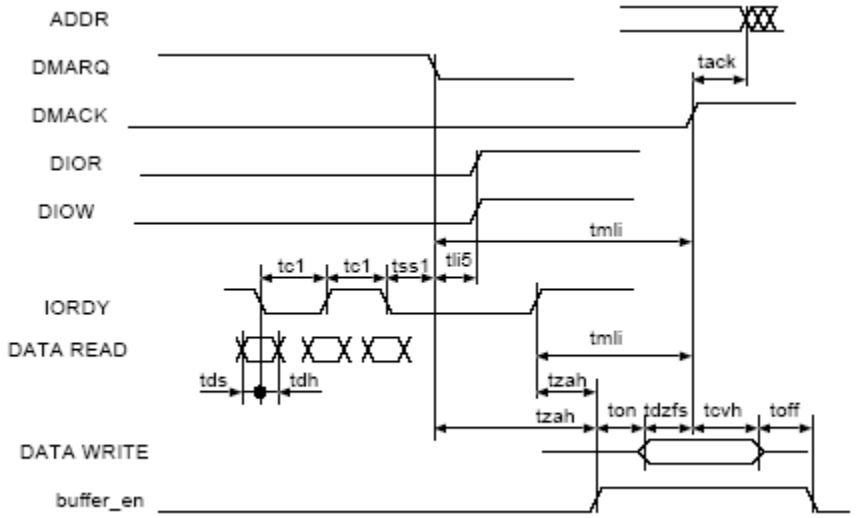


Figure 17. UDMA In Device Terminates Transfer Timing Diagram

Table 28. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 15, Figure 16, Figure 17	Description	Controlling Variable
tack	tack	tack (min) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env * T) – (tskew1 + tskew2) tenv (max) = (time_env * T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp * T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp * T) – (tco + tsu + 3T + 2 *tbuf + 2*tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) * T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) * T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs * T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff big enough to avoid bus contention

Table 33. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{OE}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{EB}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{EB}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{LBA}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{LBA}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{ECB}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{ECB}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{DTACK}$ setup time[1]	0	—	ns
WE20	$\overline{DTACK}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing

2 BCLK parameters are being measured from the 50% VDD.

3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 28, Figure 29, Figure 30, Figure 31, Figure 32, and Figure 33 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

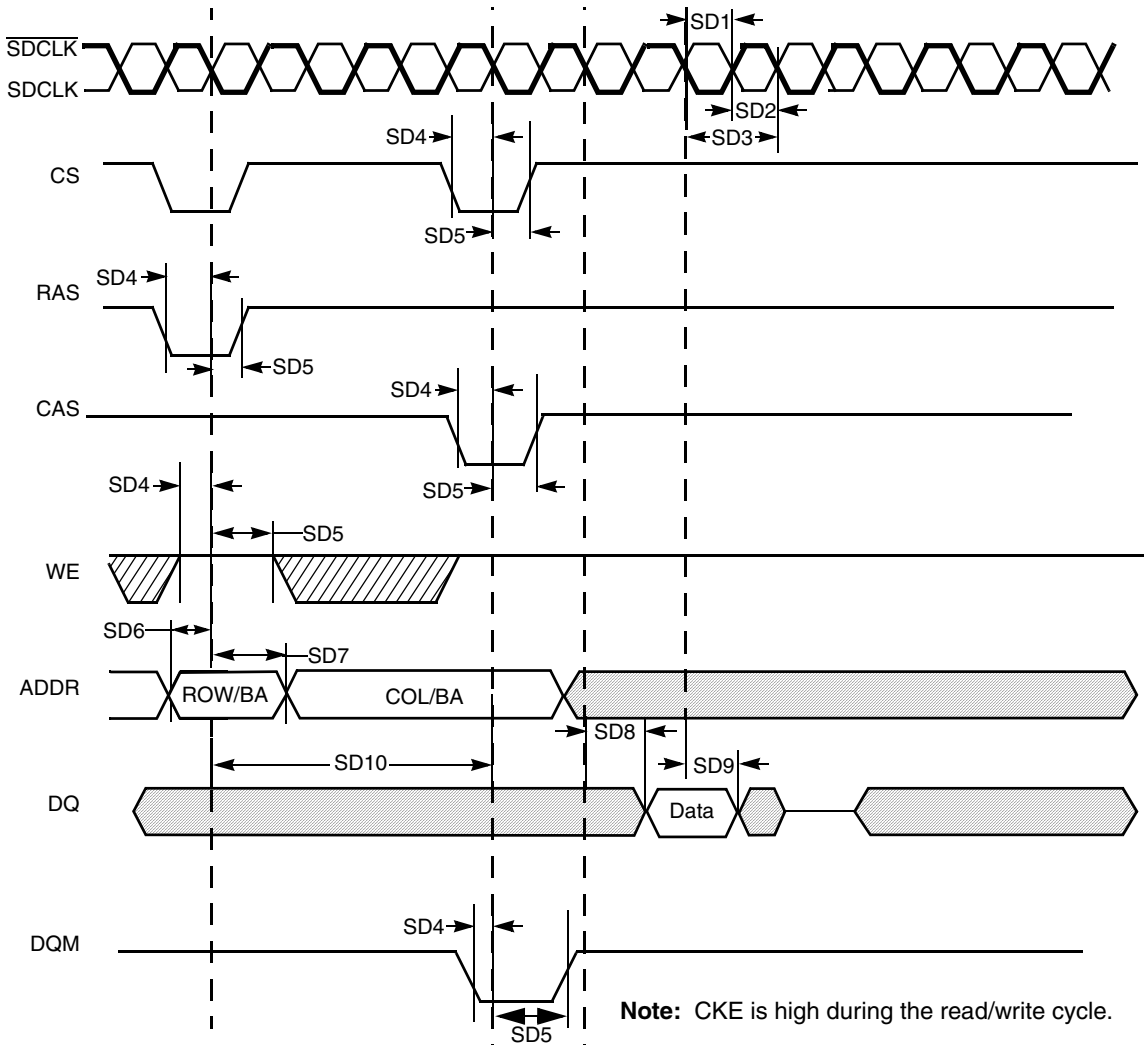


Figure 34. SDRAM Read Cycle Timing Diagram

Table 34. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM}}$ clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns

Table 36. SDRAM Refresh Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

[1] SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 36 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

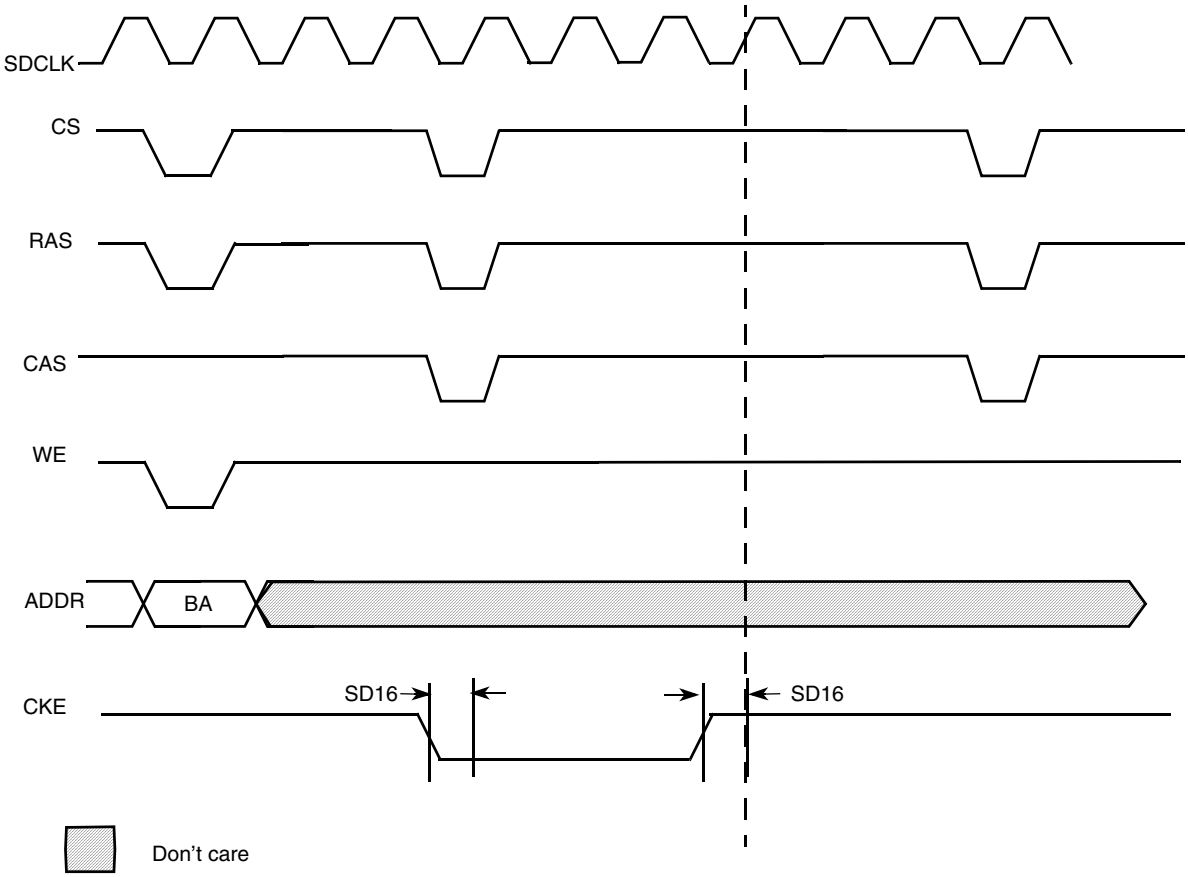


Figure 37. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 37. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

4.3.13 I²C Electrical Specifications

This section describes the electrical information of the I²C Module.

4.3.13.1 I²C Module Timing

Figure 42 depicts the timing of I²C module. Table 43 lists the I²C module timing parameters where the I/O supply is 2.7 V. 1

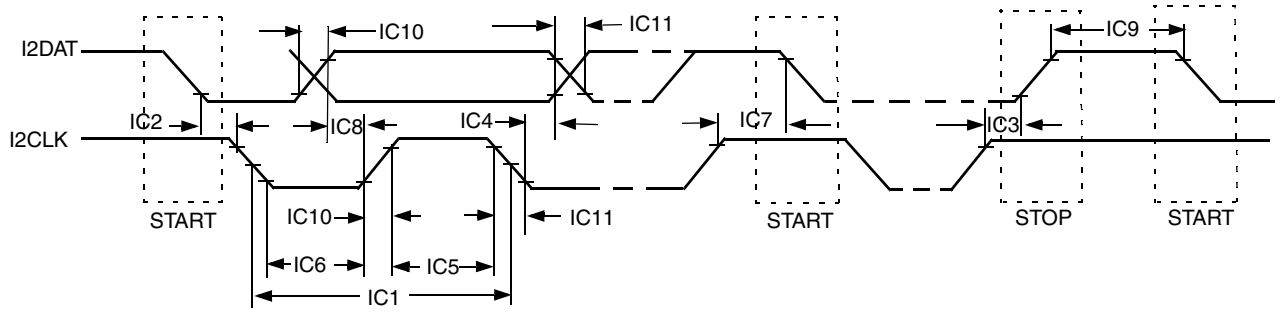


Figure 42. I²C Bus Timing Diagram

Table 43. I²C Module Timing Parameters—I²C Pin I/O Supply=2.7 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	20+0.1C_b[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	20+0.1C_b[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

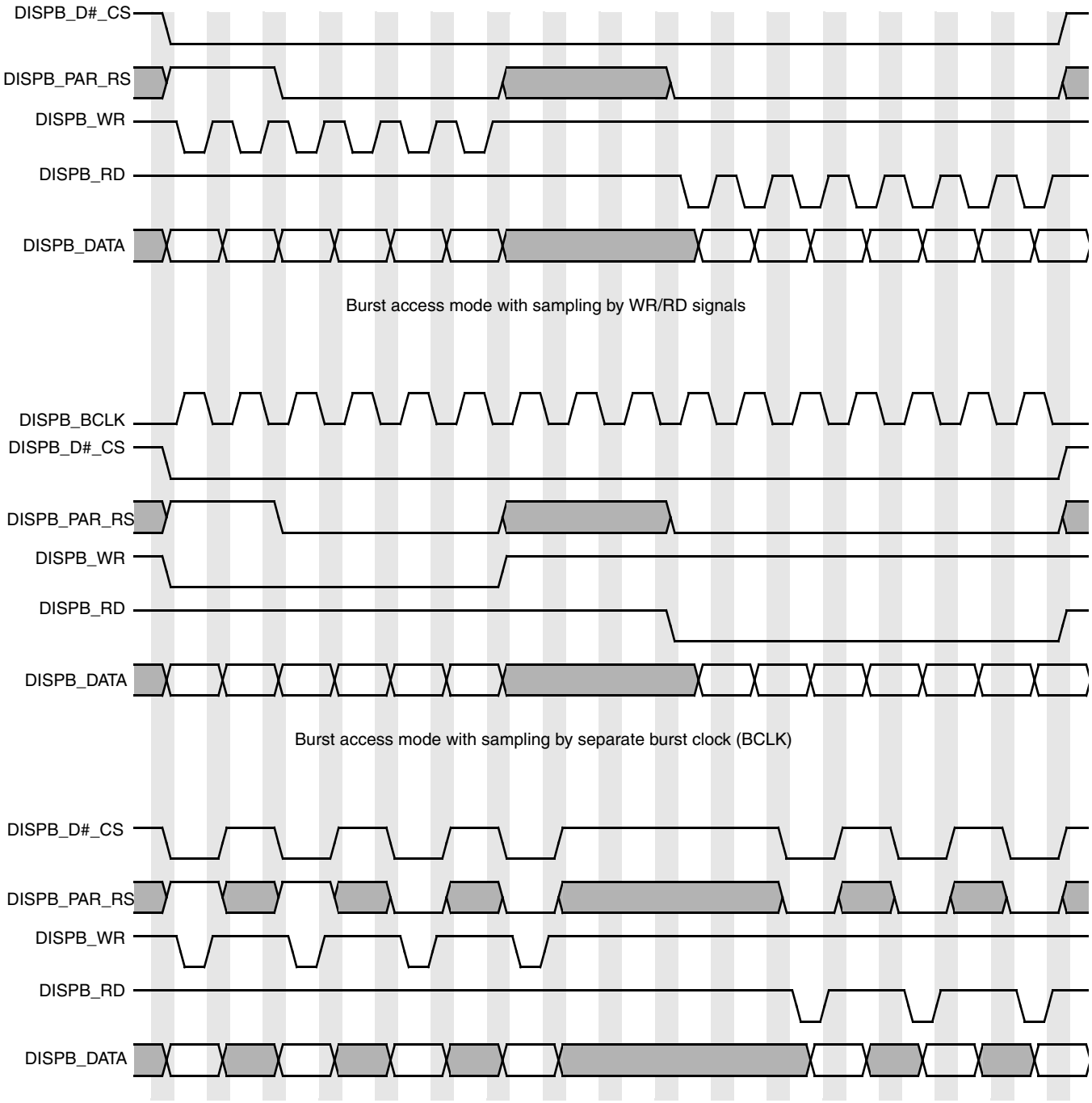


Figure 53. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

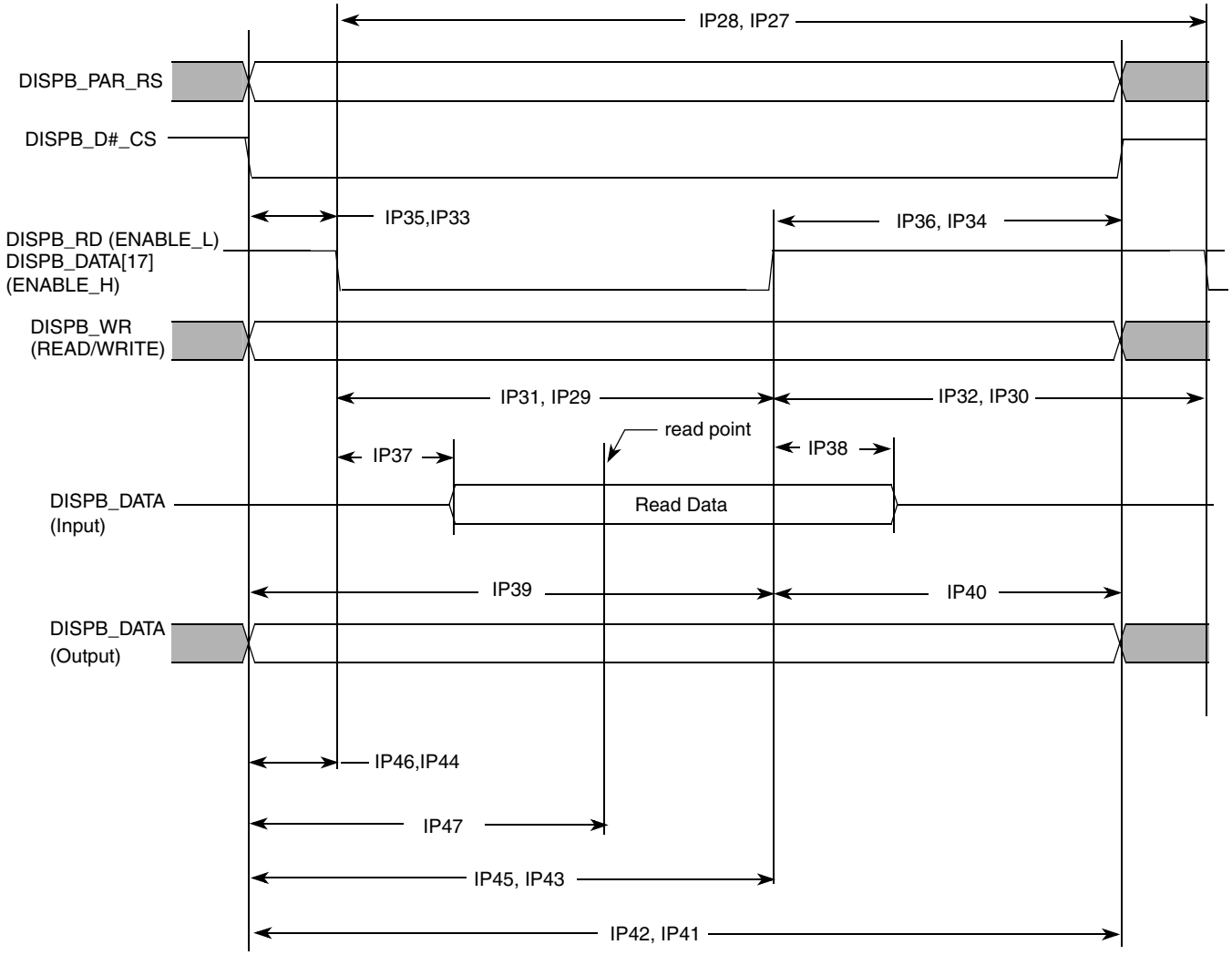


Figure 60. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Table 50. Asynchronous Parallel Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP29	Read low pulse width	Trl	Tdicdr–Tdicur–1.5	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.5	ns
IP30	Read high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.5	Tdicpr–Tdicdr+ Tdicur	Tdicpr–Tdicdr+Tdicur+1.5	ns
IP31	Write low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP32	Write high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP34	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns
IP35	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

4.3.16 Memory Stick Host Controller (MSHC)

Figure 66, Figure 67, and Figure 68 depict the MSHC timings, and Table 52 and Table 53 list the timing parameters.

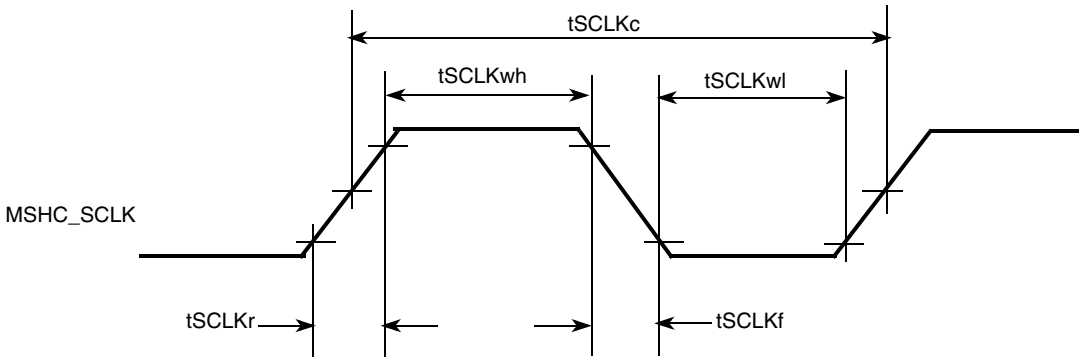


Figure 66. MSHC_CLK Timing Diagram

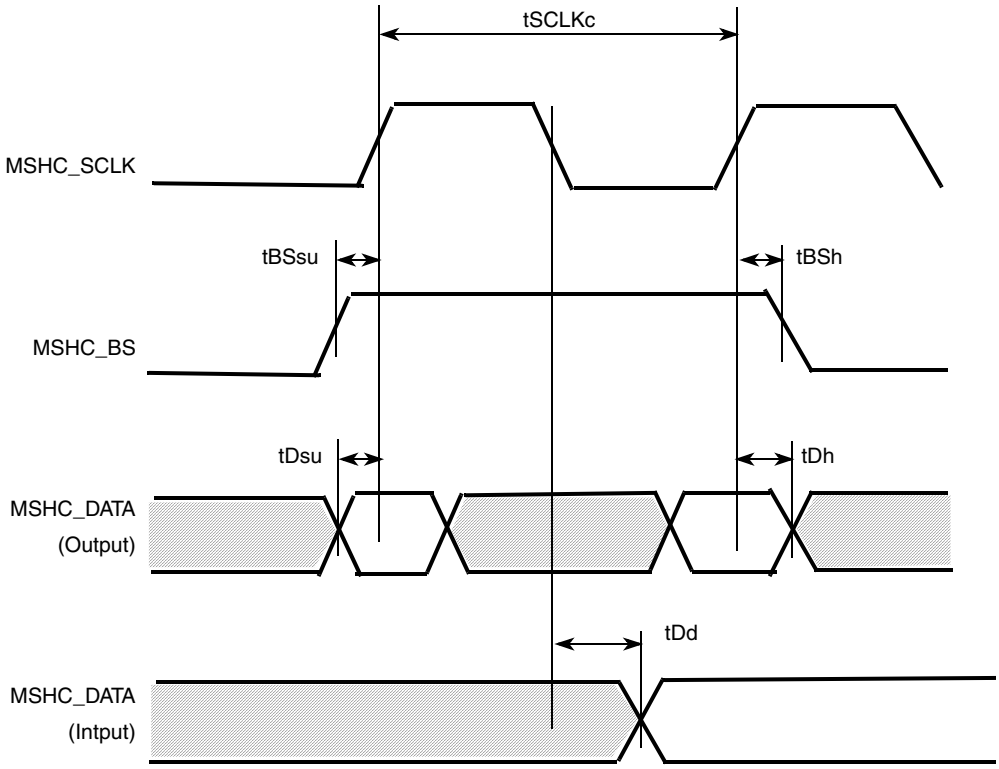


Figure 67. Transfer Operation Timing Diagram (Serial)

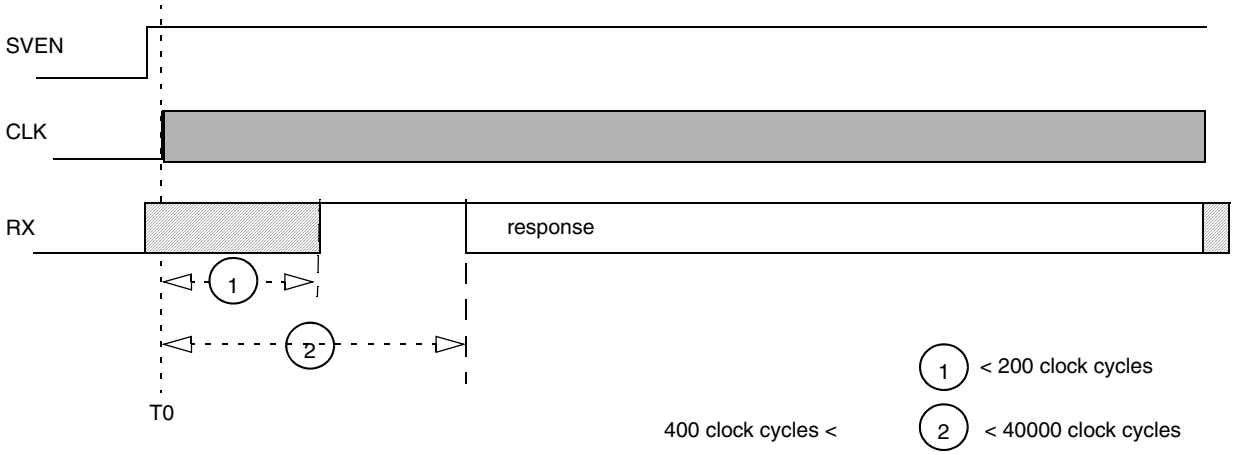


Figure 74. Internal-Reset Card Reset Sequence

4.3.20.2.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 75):

1. After powerup, the clock signal is enabled on CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
4. RST is set High (time T1)
5. RST must remain High for at least 40000 clock cycles after T1 and a response must be received on RX between 400 and 40000 clock cycles after T1.

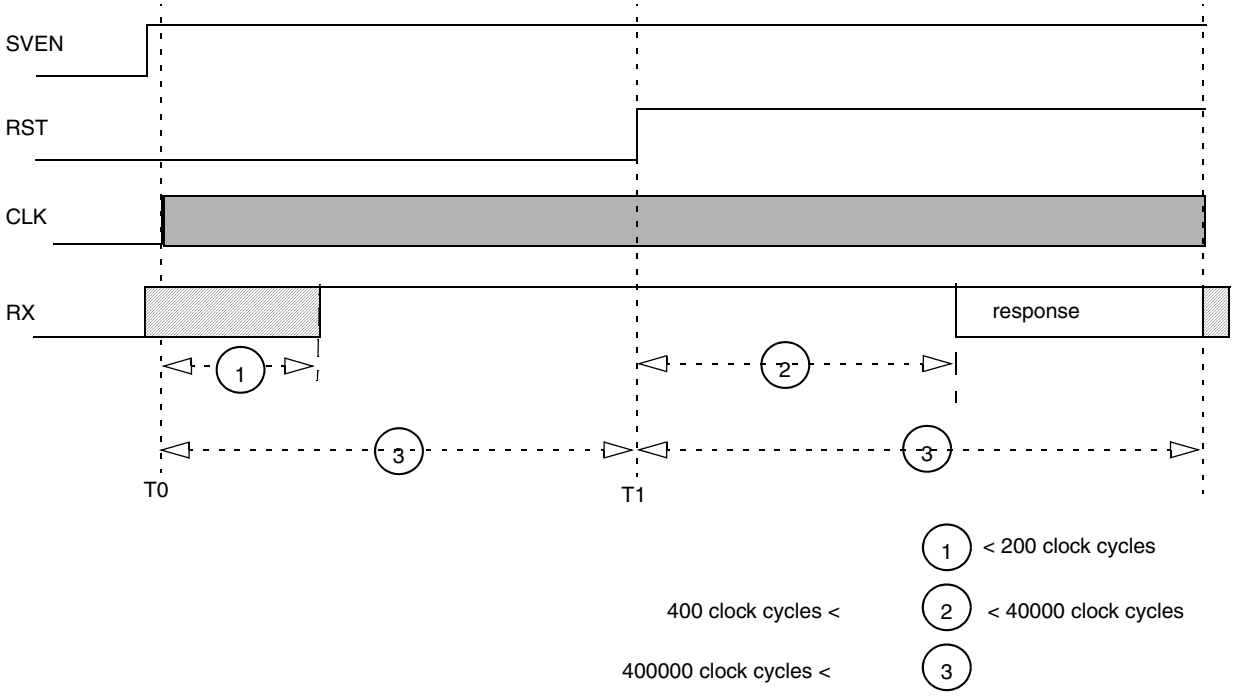


Figure 75. Active-Low-Reset Card Reset Sequence

Table 59. SJC Timing Parameters (continued)

ID	Parameter	All Frequencies		Unit
		Min	Max	
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 On cases where SDMA TAP is put in the chain, the max TCK frequency is limited by max ratio of 1:8 of SDMA core frequency to TCK limitation. This implies max frequency of 8.25 MHz (or 121.2 ns) for 66 MHz IPG clock.

2 V_M - mid point voltage

4.3.22 SSI Electrical Specifications

This section describes the electrical information of SSI. Note the following pertaining to timing information:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on AUDMUX signals when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing will be same as that of Tx Data (for example, during AC97 mode of operation).

4.3.22.1 SSI Transmitter Timing with Internal Clock

Figure 81 depicts the SSI transmitter timing with internal clock, and Table 60 lists the timing parameters.

4.3.22.2 SSI Receiver Timing with Internal Clock

Figure 82 depicts the SSI receiver timing with internal clock, and Table 61 lists the timing parameters.

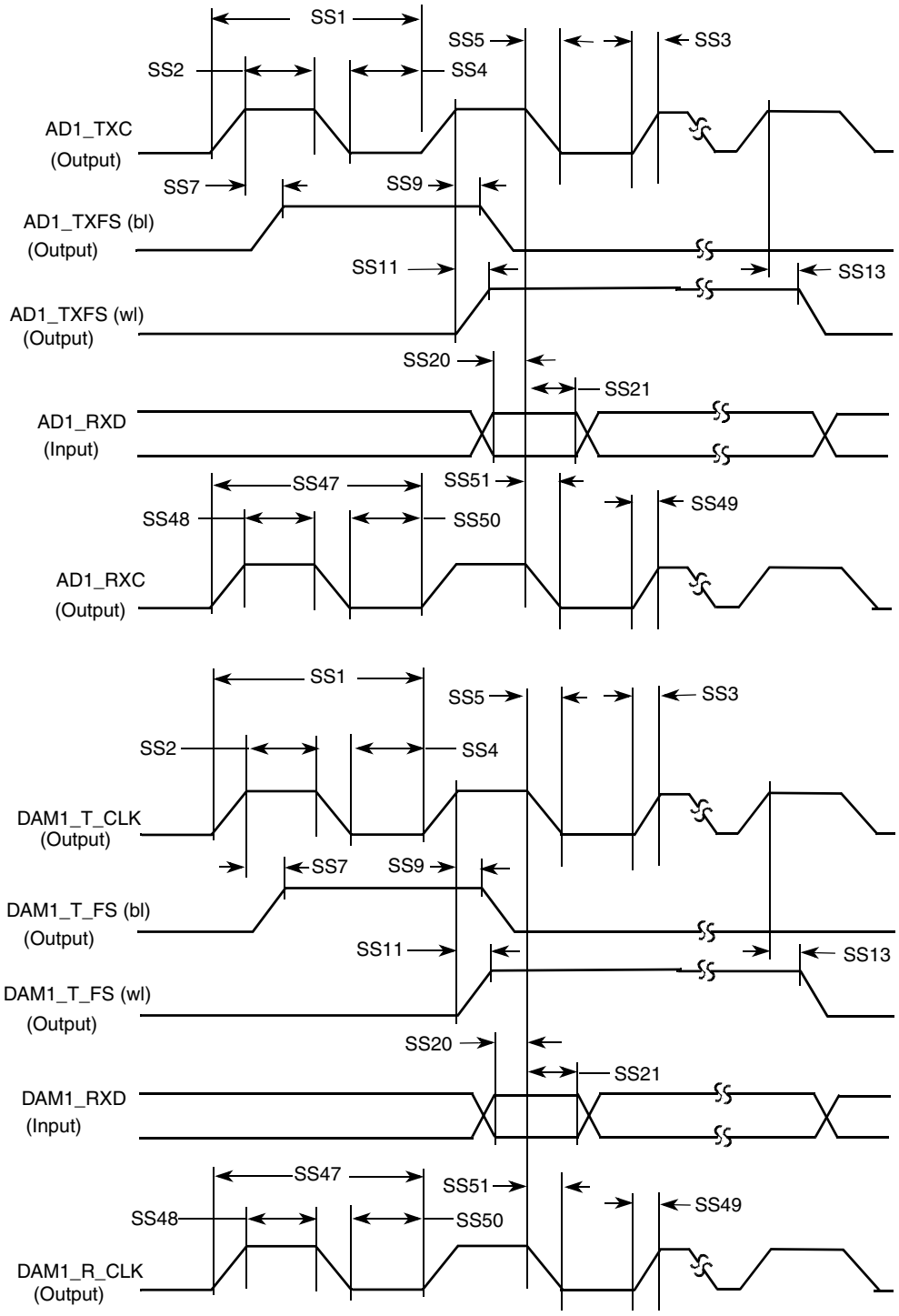


Figure 82. SSI Receiver with Internal Clock Timing Diagram

5.2.2 MAPBGA Signal Assignment–19 × 19 mm 0.8 mm

See Table 71 for the 19 × 19 mm, 0.8 mm pitch signal assignments/ball map.

5.2.3 Connection Tables–19 x 19 mm 0.8 mm

Table 67 shows the device connection list for power and ground, alpha-sorted followed by Table 68, which shows the no-connects. Table 69 shows the device connection list for signals.

5.2.3.1 Ground and Power ID Locations—19 x 19 mm 0.8 mm

Table 67. 19 x 19 BGA Ground/Power ID by Ball Grid Location

GND/PWR ID	Ball Location
FGND	U16
FUSE_VDD	T15
FVCC	T16
GND	A1, A2, A3, A21, A22, A23, B1, B2, B22, B23, C1, C2, C22, C23, D22, D23, J12, J13, K10, K11, K12, K13, K14, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14, R12, Y1, Y23, AA1, AA2, AA22, AA23, AB1, AB2, AB21, AB22, AB23, AC1, AC2, AC21, AC22, AC23
IOQVDD	T8
MGND	U14
MVCC	U15
NVCC1	G15, G16, H16, J17
NVCC2	N16, P16, R15, R16, T14
NVCC3	K7, K8, L7, L8
NVCC4	H14, J15, K15
NVCC5	G9, G10, H8, H9
NVCC6	G11, G12, G13, H12
NVCC7	H15, J16, K16, L16, M16
NVCC8	H10, H11, J11
NVCC9	G14
NVCC10	P8, R7, R8, R9, T9
NVCC21	T11, T12, T13, U11
NVCC22	T10, U7, U8, U9, U10, V6, V7, V8, V9, V10
QVCC	H13, J14, L15, M15, N9, N15, P9, P15, R10, R11, R13, R14
QVCC1	J8, J9, J10, K9
QVCC4	L9, M7, M8, N8
SGND	U13
SVCC	U12
UVCC	P18
UGND	P17

Table 68. 19 x 19 BGA No Connects[1]

Signal	Ball Location
NC	N7
NC	P7
NC	U21

1 These contacts are not used and must be floated by the user.

5.2.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location
A0	Y6
A1	AC5
A10	V15
A11	AB3
A12	AA3
A13	Y3
A14	Y15
A15	Y14
A16	V14
A17	Y13
A18	V13
A19	Y12
A2	AB5
A20	V12
A21	Y11
A22	V11
A23	Y10
A24	Y9
A25	Y8
A3	AA5
A4	Y5
A5	AC4
A6	AB4
A7	AA4
A8	Y4
A9	AC3
ATA_CS0	E1
ATA_CS1	G4
ATA_DIOR	E3
ATA_DIOW	H6
ATA_DMACK	E2
$\overline{\text{ATA\_RESET}}$	F3
BATT_LINE	F6
BCLK	W20
BOOT_MODE0	F17
BOOT_MODE1	C21

Signal ID	Ball Location
CKIL	E21
CLKO	C20
CLKSS	H17
COMPARE	A20
CONTRAST	N21
CS0	U17
CS1	Y22
CS2	Y18
CS3	Y19
CS4	Y20
CS5	AA21
CSI_D10	K21
CSI_D11	K22
CSI_D12	K23
CSI_D13	L20
CSI_D14	L18
CSI_D15	L21
CSI_D4	J20
CSI_D5	J21
CSI_D6	L17
CSI_D7	J22
CSI_D8	J23
CSI_D9	K20
CSI_HSYNC	H22
CSI_MCLK	H20
CSI_PIXCLK	H23
CSI_VSYNC	H21
CSPI1_MISO	N2
CSPI1_MOSI	N1
CSPI1_SCLK	M4
CSPI1_SPI_RDY	M1
CSPI1_SS0	M2
CSPI1_SS1	N6
CSPI1_SS2	M3
CSPI2_MISO	B4
CSPI2_MOSI	D5

5.3 Ball Maps

Table 70. Ball Map—14 x 14 0.5 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	GND	SFS5	CSPI2_MISO	CSPI2_SS2	USBOTG_DATA7	USBOTG_DATA3	USBOTG_NXT	USB_BYP	RXD1	DSR_DCE1	DSR_DTE1	RXD2	CE_CONTROL	KEY_ROW3	KEY_ROW7	KEY_COL3	KEY_COL7	TDO	SJC_MOD	SVEN0	CAPTURE	GPIO1_6	WATCHDOG_RST	GND	GND	A
B	GND	GND	STXD4	SRXD5	CSPI2_SS0	CSPI2_SPI_RDY	USBOTG_DATA5	USBOTG_DATA1	USBOTG_DIR	USB_PWR	CTS1	DCD_DCE1	DCD_DTE1	RTS2	KEY_ROW1	KEY_ROW5	KEY_COL1	KEY_COL5	TCK	TRSTB	SRX0	SCLK0	GPIO1_1	GPIO1_5	GND	GND	B
C	GND	GND	SRXD4	SCK4	STXD5	CSPI2_SS1	CSPI2_SCLK	USBOTG_DATA4	USBOTG_STP	USB_OC	DTR_DCE1	DTR_DTE1	TXD2	KEY_ROW2	KEY_COL0	KEY_COL4	RTCK	$\overline{DE}$	SRST0	GPIO1_2	BOOT_MODE1	BOOT_MODE3	CLKO	GND	GND	GND	C
D	GND	CSPI3_MOSI	SCK5																					BOOT_MODE2	GND	BOOT_MODE4	D
E	CSPI3_SCLK	ATA_DIOR	CSPI2_MOSI		NVCC5																	GND		GND	DVFS0	POWER_FAIL	E
F	ATA_DMACK	ATA_CS1	SFS4			NVCC5	BATT_LINE	USBOTG_DATA6	USBOTG_DATA0	TXD1	RI_DCE1	DTR_DCE2	KEY_ROW0	KEY_ROW6	KEY_COL6	TDI	STX0	GPIO1_0	GPIO1_4	BOOT_MODE0	GND			CKIH	GPIO1_3	VSTBY	F
G	PWMO	$\overline{PC\_RW}$	CSPI3_MISO			CSPI3_SPI_RDY	NVCC5		USBOTG_DATA2	USBOTG_CLK	RTS1	RI_DTE1	CTS2	KEY_ROW4	KEY_COL2	TMS	SIMPD0	COMPARE	NVCC1		NVCC1			DVFS1	VPG0	CLKSS	G
H	PC_RST	PC_BVD1	$\overline{ATA\_RESET}$			ATA_DIOW															CKIL			$\overline{POR}$	I2C_DAT	GPIO3_1	H
J	PC_VS1	PC_READY	IOIS16			ATA_CS0	PC_POE			QVCC1	QVCC1	NVCC8	NVCC8	QVCC	NVCC6	NVCC6	NVCC9			VPG1	$\overline{RESET\_IN}$			I2C_CLK	CSI_VSYNC	CSI_PIXCLK	J
K	$\overline{PC\_CD2}$	SD1_DATA3	PC_PWRON			PC_BVD2	PC_VS2		QVCC1						NVCC6			NVCC1		CSI_HSYNC	GPIO3_0			CSI_MCLK	CSI_D5	CSI_D7	K
L	SD1_DATA1	SD1_CMD	SD1_DATA2			$\overline{PC\_WAIT}$	$\overline{PC\_CD1}$		NVCC3		QVCC1	GND	QVCC	QVCC	QVCC	QVCC		NVCC4	NVCC4	CSI_D8	CSI_D4			CSI_D6	CSI_D9	CSI_D11	L
M	USBH2_DATA0	USBH2_STP	USBH2_DATA1			SD1_DATA0	SD1_CLK		NVCC3		GND	GND	GND	GND	GND	GND		QVCC		CSI_D14	CSI_D12			CSI_D10	CSI_D13	CSI_D15	M
N	USBH2_CLK	CSPI1_SCLK	CSPI1_SPI_RDY			USBH2_NXT	USBH2_DIR		QVCC4		NVCC3	GND	GND	GND	GND	GND		NVCC7		SD_D_I	FPSHIFT			VSYNC0	HSYNC	DRDY0	N
P	CSPI1_SS1	CSPI1_MOSI	CSPI1_SS0			CSPI1_SS2	CSPI1_MISO		NVCC10		NVCC10	GND	GND	GND	GND	GND		NVCC7		READ	LCS1			SD_D_CLK	SD_D_IO	LCS0	P
R	STXD3	SCK3	SRXD3			SFS3	SRXD6		QVCC4		NVCC10	GND	GND	GND	GND	GND		NVCC7		D3_CLS	PAR_RS			CONTRAST	WRITE	VSYNC3	R
T	STXD6	SCK6	SFS6			$\overline{NFCE}$	$\overline{NFWE}$		QVCC4		NVCC10	GND	GND	SGND	MGND	UGND		NVCC7		LD4	LD2			LD0	SER_RS	D3_REV	T
U	NFRB	$\overline{NFWP}$	NFCLE			D15	D11		QVCC4									QVCC		TTM_PAD	LD8			LD6	D3_SPL	LD1	U
V	NFALE	$\overline{NFRE}$	D13			D9	D5			QVCC	QVCC	QVCC	QVCC	SVCC	MVCC	UVCC	GND			LD17	LD13			LD10	LD3	LD5	V
W	D14	D12	D7			D3	NVCC22														EB0			LD15	LD7	LD9	W
Y	D10	D8	D1			IOQVDD	NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	NVCC21	NVCC21	NVCC21	NVCC2	NVCC2	NVCC2	NVCC2	M_GRANT			EB1	LD11	LD12	Y
AA	D6	D4	A4			NVCC22	SD31	SD28	SD27	SD23	SD21	SD18	SD16	SD13	SD9	SD7	SD5	SD3	SD2	DQM2	SDCLK			FVCC	LD14	LD16	AA
AB	D2	D0	A6		A2																	RW		FGND	OE	BCLK	AB
AC	MA10	GND	A11																					FUSE_VDD	M_REQUEST	GND	AC
AD	GND	GND	A12	A13	A8	A0	SDBA0	SDQS3	SD29	SD25	SDQS2	SD17	SD15	SD12	SD8	SDQS0	SD4	SD0	DQM1	CAS	SDCKE0	CS3	ECB	GND	GND	GND	AD
AE	GND	GND	A7	A3	SDBA1	SD30	SD26	SD24	SD22	SD20	SD19	SDQS1	SD14	SD11	SD10	SD6	SD1	DQM3	DQM0	$\overline{SDCLK}$	CS2	LBA	CS0	GND	GND	GND	AE
AF	GND	GND	A9	A5	A1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A10	RAS	SDWE	SDCKE1	CS5	CS1	CS4	GND	GND	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	