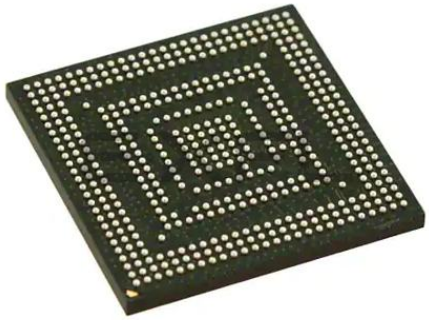

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31lvkn5cr2

3 Signal Descriptions

Signal descriptions are in the reference manual. Special signal considerations are listed following this paragraph. The BGA ball assignment is in Section 5, "Package Information and Pinout."

Special Signal Considerations:

- **Tamper detect (GPIO1_6)**

  Tamper detect logic is used to issue a security violation. This logic is activated if the tamper detect input is asserted.

  The tamper detect logic is disabled after reset. After enabling the logic, it is impossible to disable it until the next reset. The GPR[16] bit functions as the tamper detect enable bit.

  GPIO1_6 functions similarly to other I/O with GPIO capabilities regardless of the status of the tamper detect enable bit. (For example, the GPIO1_6 can function as an input with GPIO capabilities, such as sampling through PSR or generating interrupts.)

- **Power ready (GPIO1_5)**

  The power ready input, GPIO1_5, should be connected to an external power management IC power ready output signal. If not used, GPIO1_5 must either be (a) externally pulled-up to NVCC1 or (b) a no connect, internally pulled-up by enabling the on-chip pull-up resistor. GPIO1_5 is a dedicated input and cannot be used as a general-purpose input/output.

- **SJC_MOD**

  SJC_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.

- **CE_CONTROL**

  CE_CONTROL is a reserved input and must be externally tied to GND through a 1 kΩ resistor.

- **TTM_PAD**

  TTM_PAD is for Freescale factory use only. Control bits indicate pull-up/down disabled. However, TTM_PAD is actually connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.

- **M_REQUEST and M_GRANT**

  These two signals are not utilized internally. The user should make no connection to these signals.

- **Clock Source Select (CLKSS)**

  The CLKSS is the input that selects the default reference clock source providing input to the DPLL. To select CKIH, tie CLKSS to NVCC1. To select CKIL, tie CLKSS to ground. After initialization, the reference clock source can be changed (initial setting is overwritten) by programming the PRCS bits in the CCMR.

4.3.5.2 PIO Mode Timing

Figure 11 shows timing for PIO read, and Table 25 lists the timing parameters for PIO read.

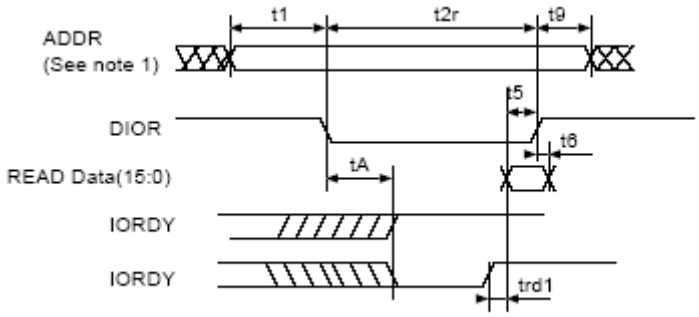


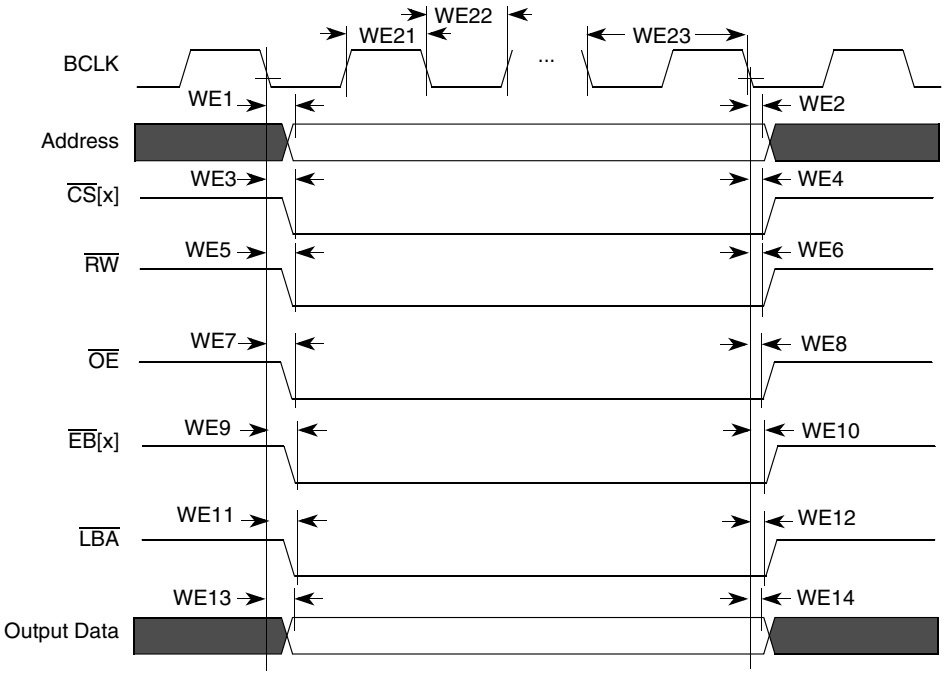
Figure 11. PIO Read Timing Diagram

Table 25. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 11	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9

Figure 12 shows timing for PIO write, and Table 26 lists the timing parameters for PIO write.

WEIM Outputs Timing



WEIM Inputs Timing

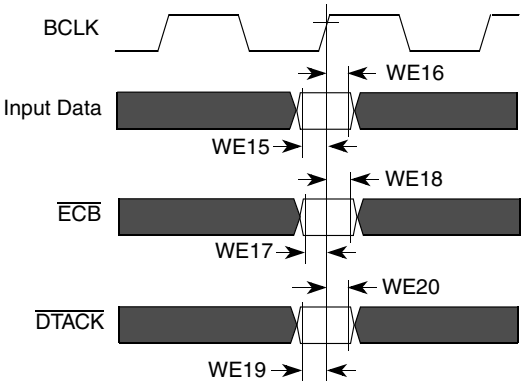


Figure 27. WEIM Bus Timing Diagram

Table 33. WEIM Bus Timing Parameters

ID	Parameter	Min	Max	Unit
WE1	Clock fall to Address Valid	–0.5	2.5	ns
WE2	Clock rise/fall to Address Invalid	–0.5	5	ns
WE3	Clock rise/fall to $\overline{CS}$[x] Valid	–3	3	ns
WE4	Clock rise/fall to $\overline{CS}$[x] Invalid	–3	3	ns
WE5	Clock rise/fall to $\overline{RW}$ Valid	–3	3	ns
WE6	Clock rise/fall to $\overline{RW}$ Invalid	–3	3	ns
WE7	Clock rise/fall to $\overline{OE}$ Valid	–3	3	ns

Table 33. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{OE}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{EB}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{EB}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{LBA}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{LBA}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{ECB}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{ECB}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{DTACK}$ setup time[1]	0	—	ns
WE20	$\overline{DTACK}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing

2 BCLK parameters are being measured from the 50% VDD.

3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 28, Figure 29, Figure 30, Figure 31, Figure 32, and Figure 33 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

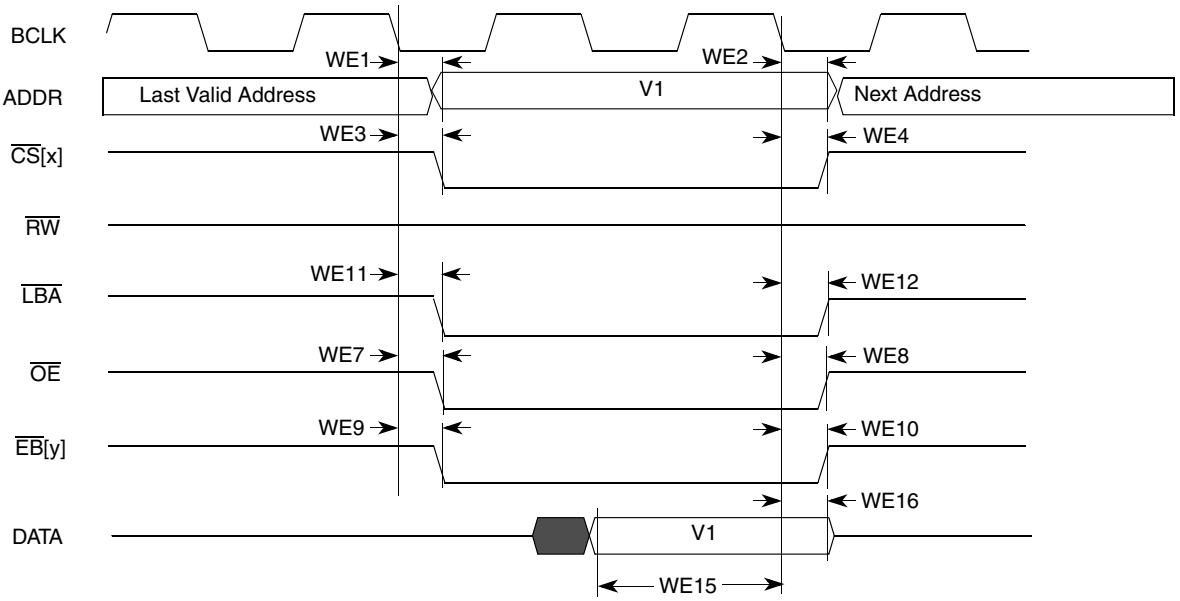


Figure 28. Asynchronous Memory Timing Diagram for Read Access—WSC=1

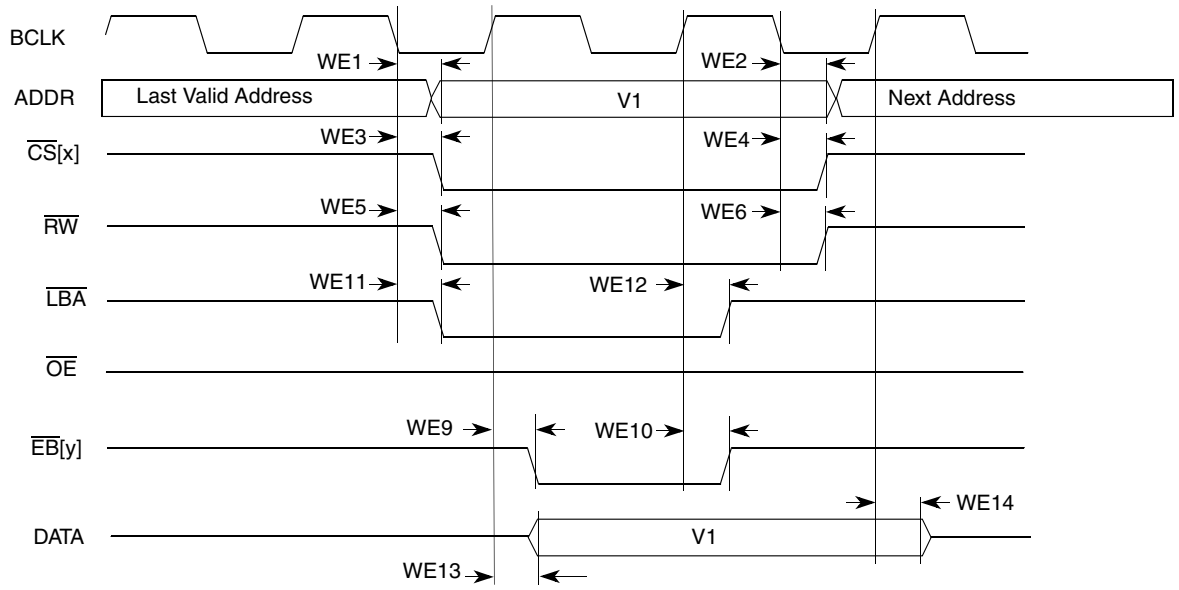


Figure 29. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

Table 35. SDR SDRAM Write Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD13	Data setup time	tDS	2.0	—	ns
SD14	Data hold time	tDH	1.3	—	ns

[1] SD11 and SD12 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

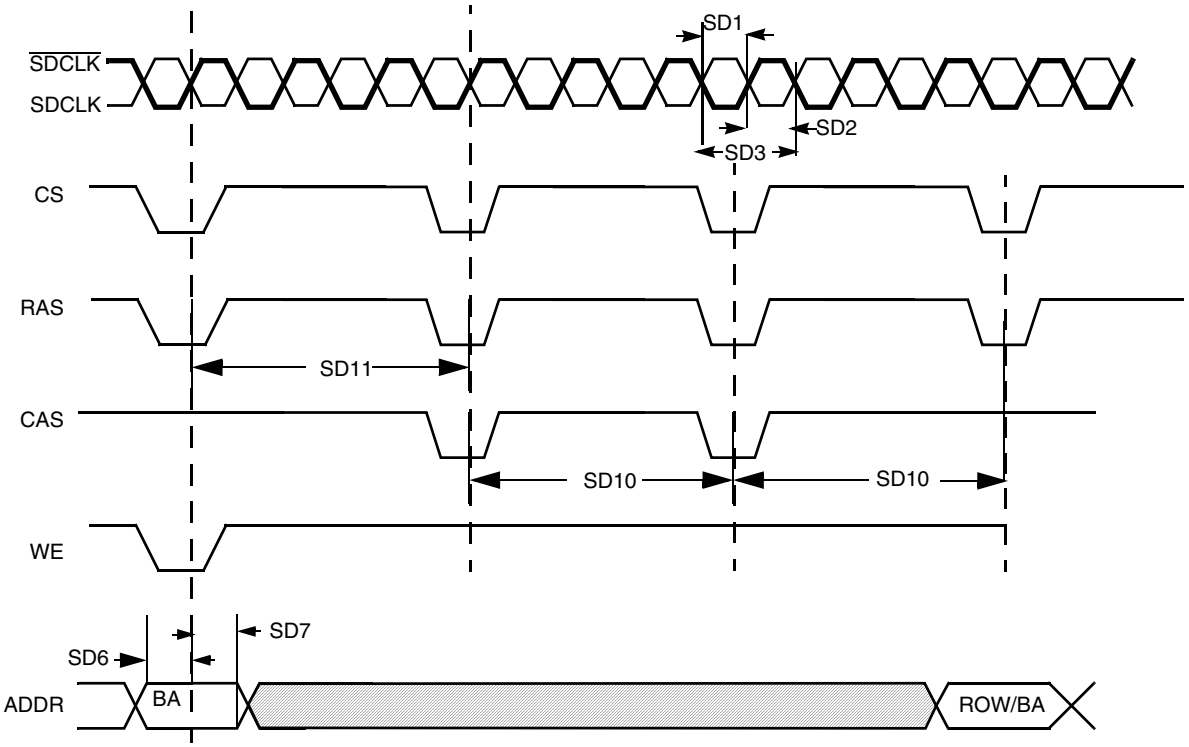


Figure 36. SDRAM Refresh Timing Diagram

Table 36. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns

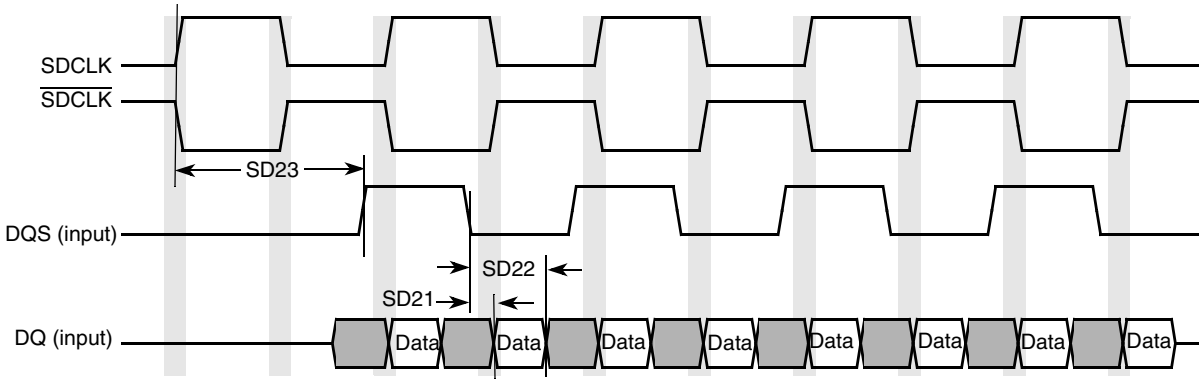


Figure 39. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 39. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 39 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.10 ETM Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a TPA that supports TRACECLK frequencies up to 133 MHz.

Figure 40 depicts the TRACECLK timings of ETM, and Table 40 lists the timing parameters.

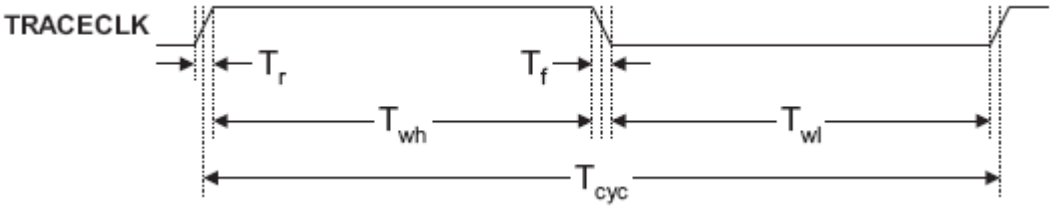


Figure 40. ETM TRACECLK Timing Diagram

4.3.13 I²C Electrical Specifications

This section describes the electrical information of the I²C Module.

4.3.13.1 I²C Module Timing

Figure 42 depicts the timing of I²C module. Table 43 lists the I²C module timing parameters where the I/O supply is 2.7 V. 1

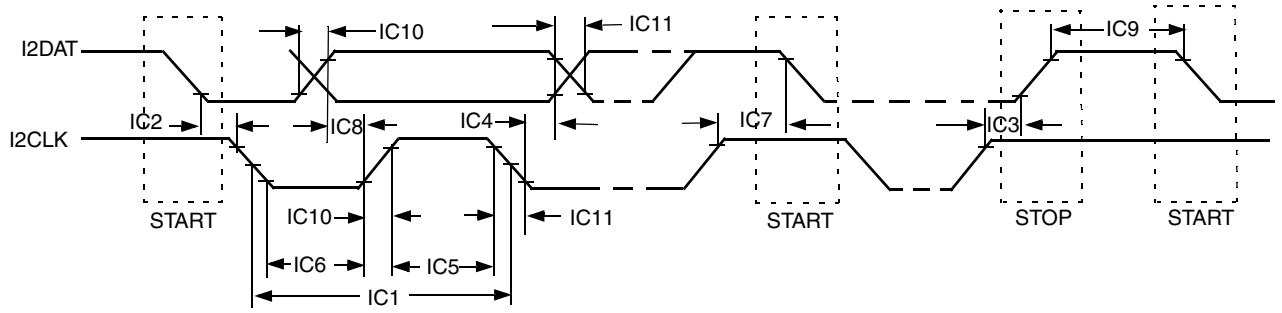


Figure 42. I²C Bus Timing Diagram

Table 43. I²C Module Timing Parameters—I²C Pin I/O Supply=2.7 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	20+0.1C_b[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	20+0.1C_b[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

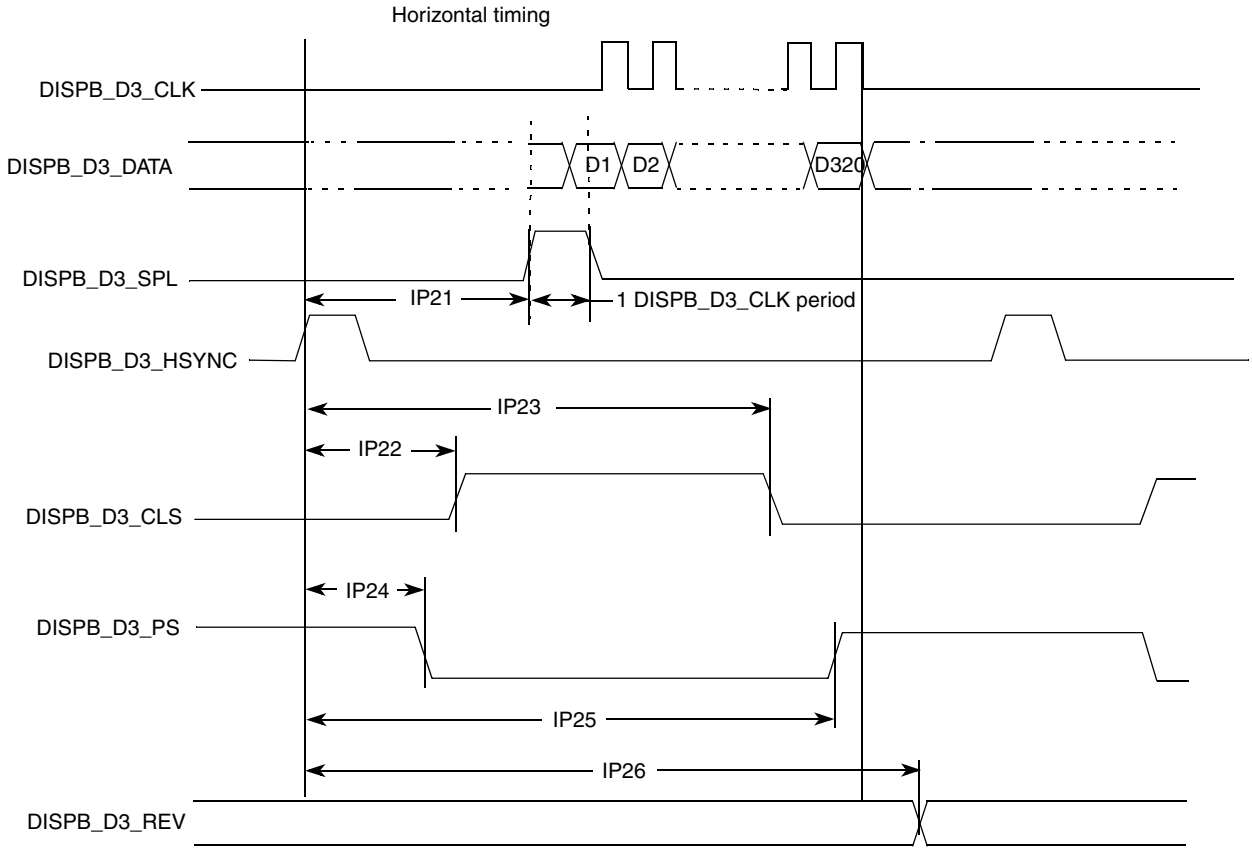
3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

4.3.15.3 Interface to Sharp HR-TFT Panels

Figure 50 depicts the Sharp HR-TFT panel interface timing, and Table 49 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics." The timing images correspond to straight polarity of the Sharp signals.



Example is drawn with FW+1=320 pixel/line, FH+1=240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 50. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

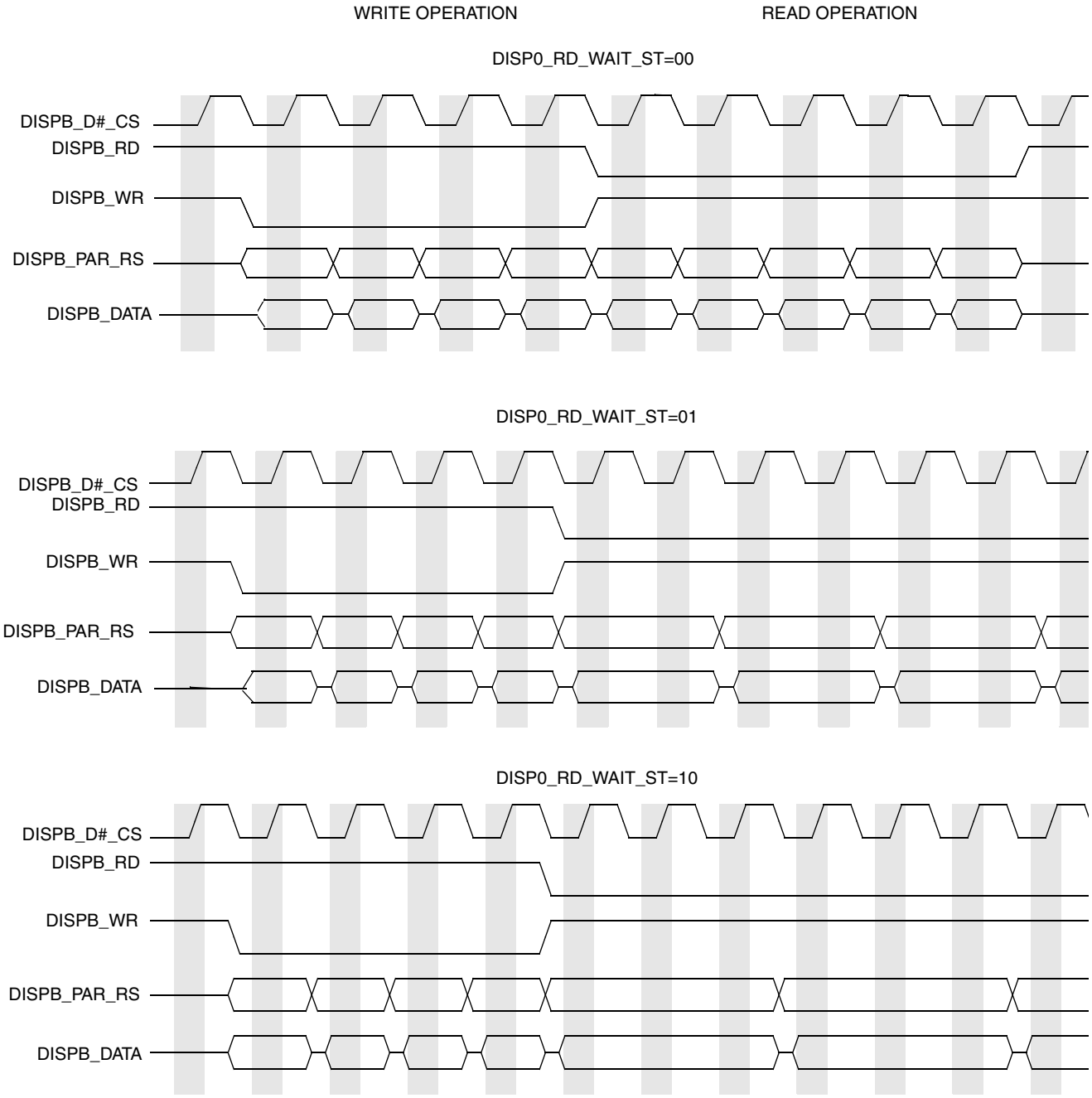


Figure 56. Parallel Interface Timing Diagram—Read Wait States

4.3.15.5.2 Parallel Interfaces, Electrical Characteristics

Figure 57, Figure 59, Figure 58, and Figure 60 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 50 lists the timing parameters at display access level. All timing images are based on active low control signals (signals polarity is controlled via the DI_DISP_SIG_POL Register).

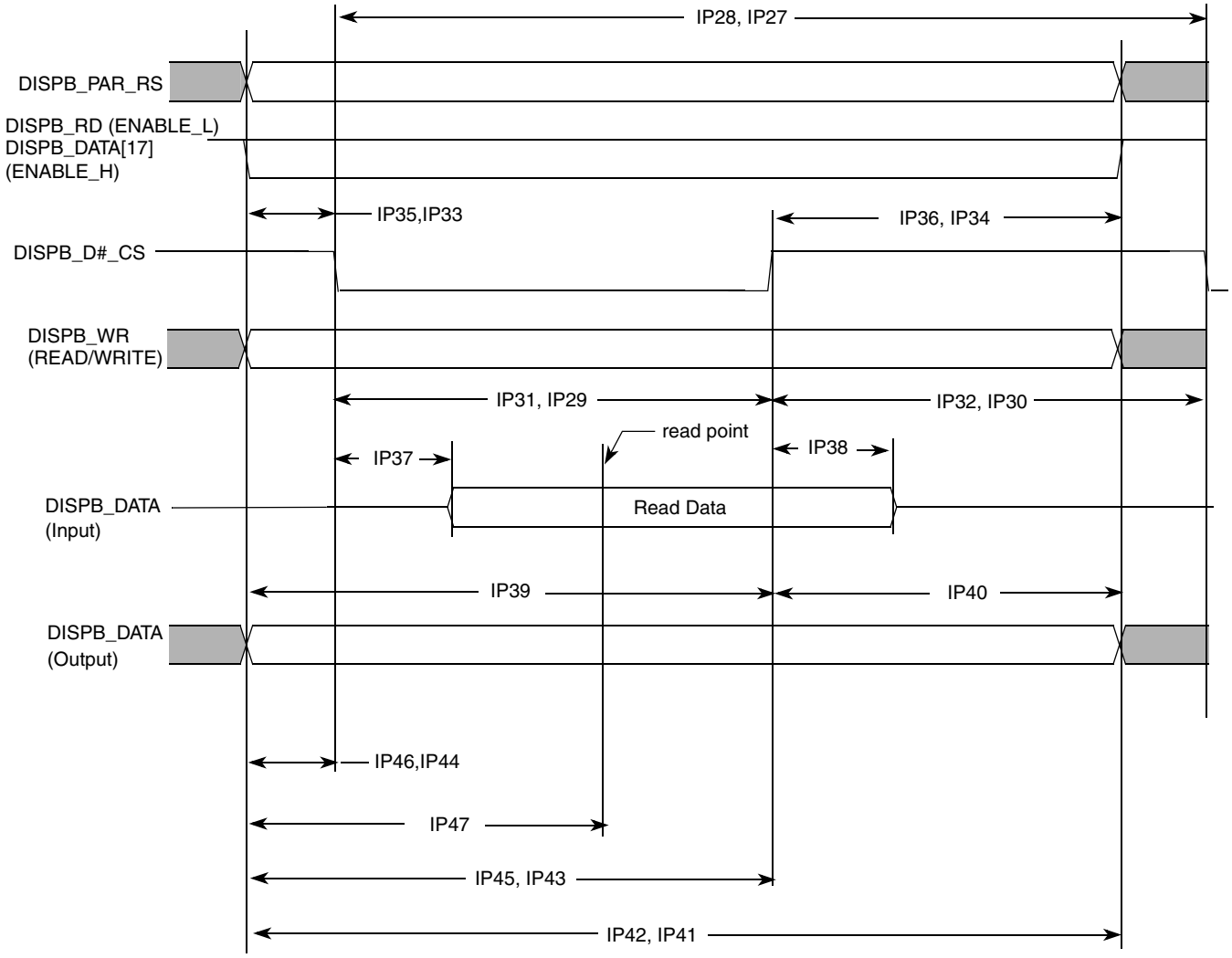


Figure 59. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

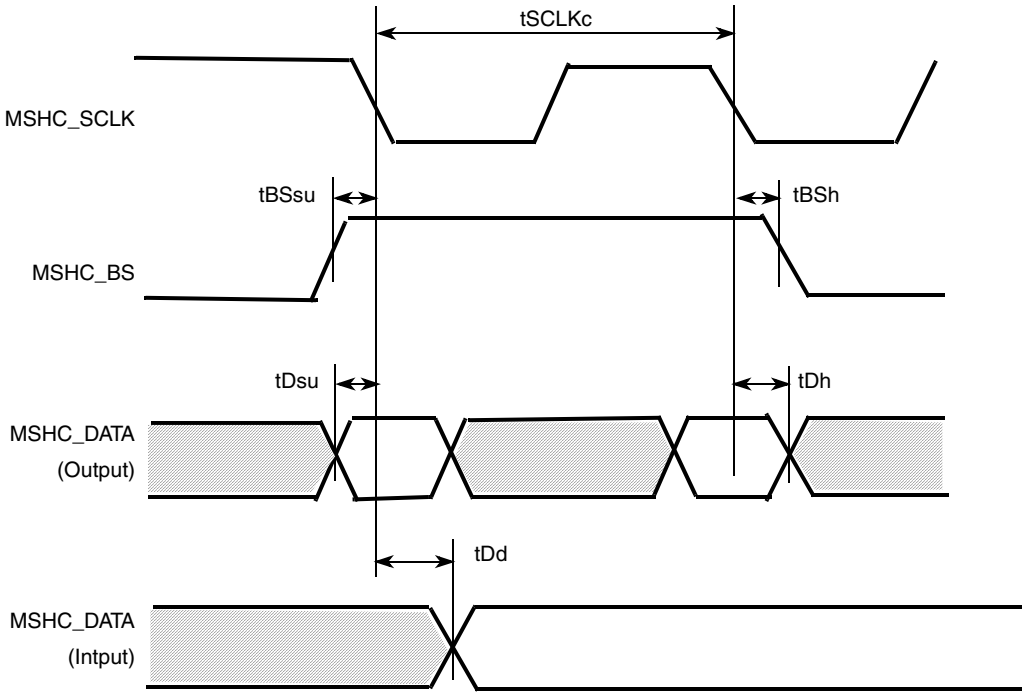


Figure 68. Transfer Operation Timing Diagram (Parallel)

NOTE

The Memory Stick Host Controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications* document. Tables in this section details the specifications requirements for parallel and serial modes, and not the MCIMX31 timing.

Table 52. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 8, "Operating Ranges," on page 13.

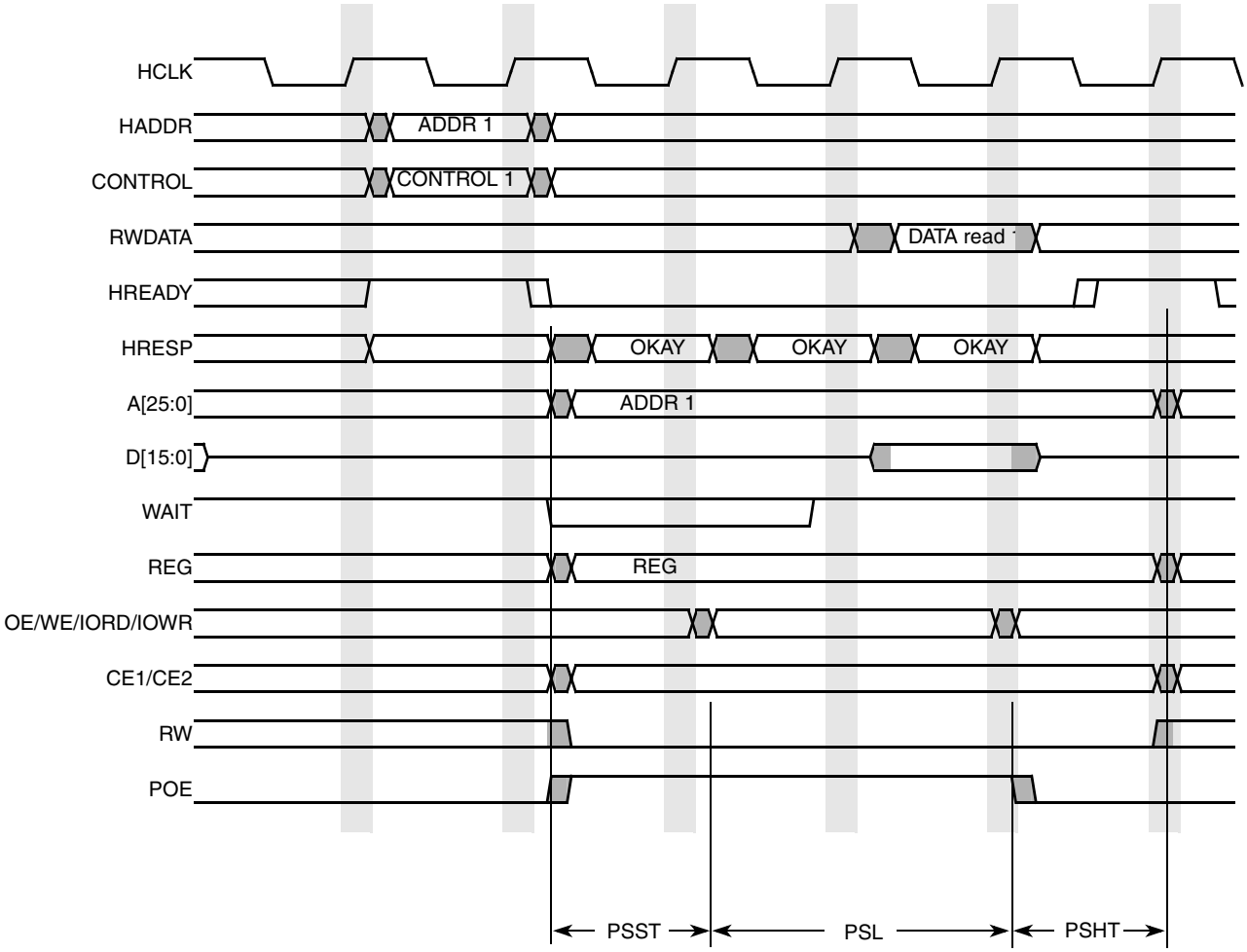


Figure 70. Read Accesses Timing Diagram—PSHT=1, PSST=1

Table 54. PCMCIA Write and Read Timing Parameters

Symbol	Parameter	Min	Max	Unit
PSHT	PCMCIA strobe hold time	0	63	clock
PSST	PCMCIA strobe set up time	1	63	clock
PSL	PCMCIA strobe length	1	128	clock

4.3.18 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

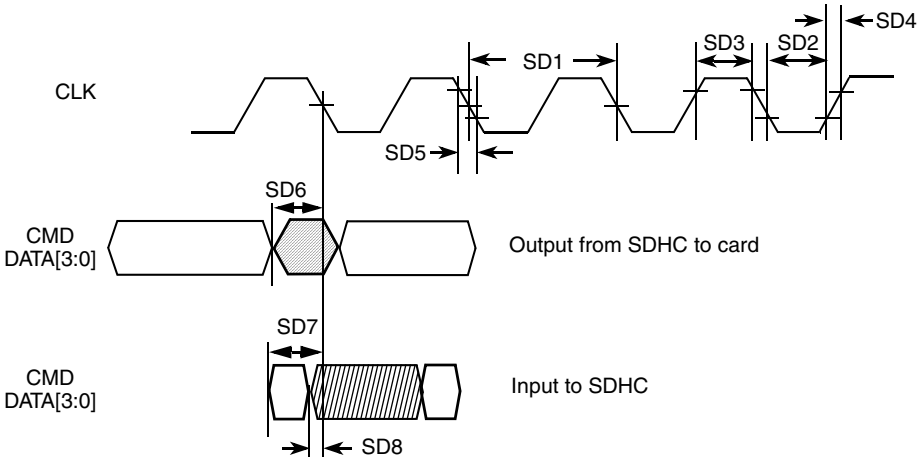


Figure 72. SDHC Timing Diagram

Table 56. SDHC Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed)	f_{PP}[2]	0	25	MHz
	Clock Frequency (MMC Full Speed)	f_{PP}[3]	0	20	MHz
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz
SD2	Clock Low Time	t_{WL}	10	—	ns
SD3	Clock High Time	t_{WH}	10	—	ns
SD4	Clock Rise Time	t_{TLH}	—	10	ns
SD5	Clock Fall Time	t_{THL}	—	10	ns
SDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	SDHC output delay	t_{ODL}	–6.5	3	ns
SDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	SDHC input setup	t_{IS}	—	18.5	ns
SD8	SDHC input hold	t_{IH}	—	–11.5	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 V–3.3 V.
2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 MHz–25 MHz.
3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 MHz–20 MHz.
4 In card identification mode, card clock must be 100 kHz–400 kHz, voltage ranges from 2.7 V–3.3 V.

4.3.20 SIM Electrical Specifications

Each SIM card interface consist of a total of 12 pins (for 2 separate ports of 6 pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the aim card will be used by the SIM card to recover the clock from the data much like a standard UART. All six (or 5 in case bi-directional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other.

There are no required timing relationships between the signals in normal mode, but there are some in two specific cases: reset and power down sequences.

4.3.20.1 General Timing Requirements

Figure 73 shows the timing of the SIM module, and Figure 57 lists the timing parameters.

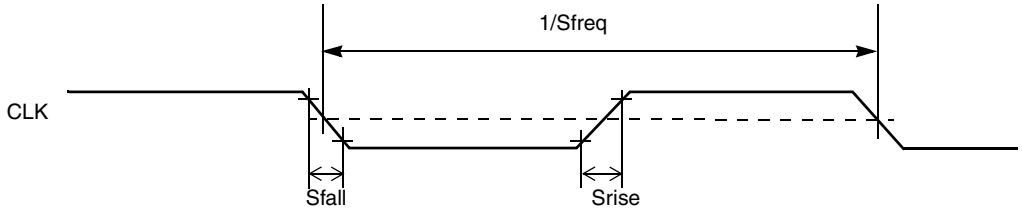


Figure 73. SIM Clock Timing Diagram

Table 57. SIM Timing Specification—High Drive Strength

Num	Description	Symbol	Min	Max	Unit
1	SIM Clock Frequency (CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM CLK Rise Time [2]	S_{rise}	—	20	ns
3	SIM CLK Fall Time [3]	S_{fall}	—	20	ns
4	SIM Input Transition Time (RX, SIMPD)	S_{trans}	—	25	ns

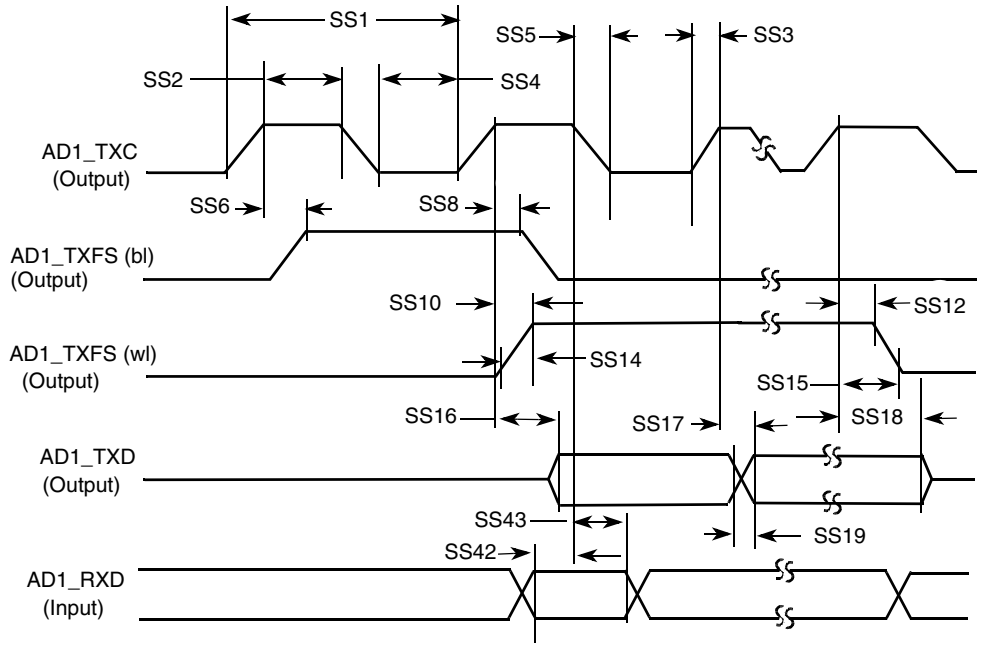
1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

4.3.20.2 Reset Sequence

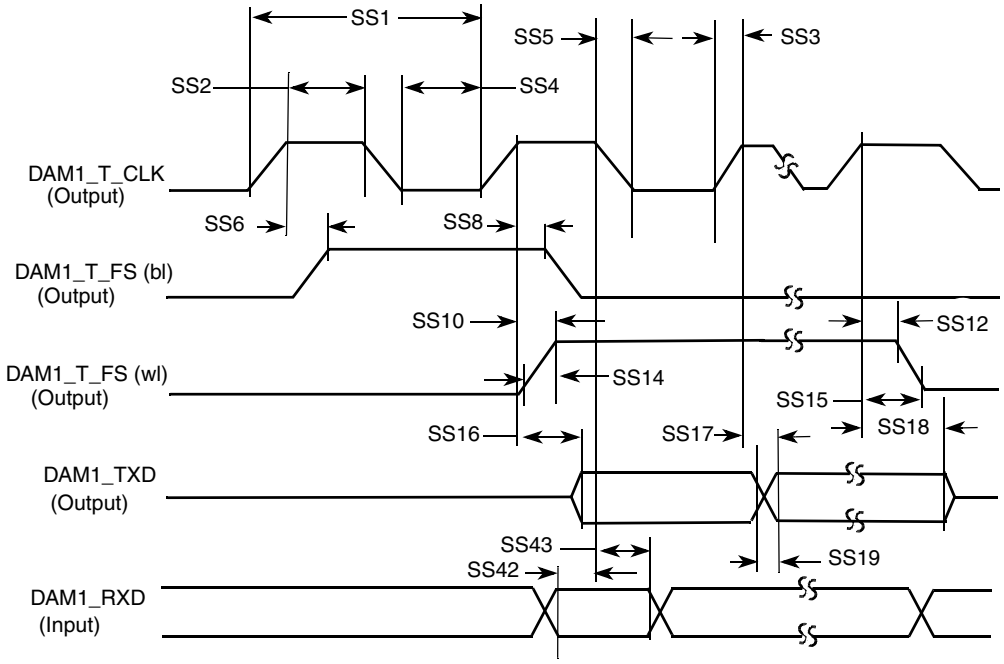
4.3.20.2.1 Cards with Internal Reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 74):

- After powerup, the clock signal is enabled on SGCLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 81. SSI Transmitter with Internal Clock Timing Diagram

4.3.22.2 SSI Receiver Timing with Internal Clock

Figure 82 depicts the SSI receiver timing with internal clock, and Table 61 lists the timing parameters.

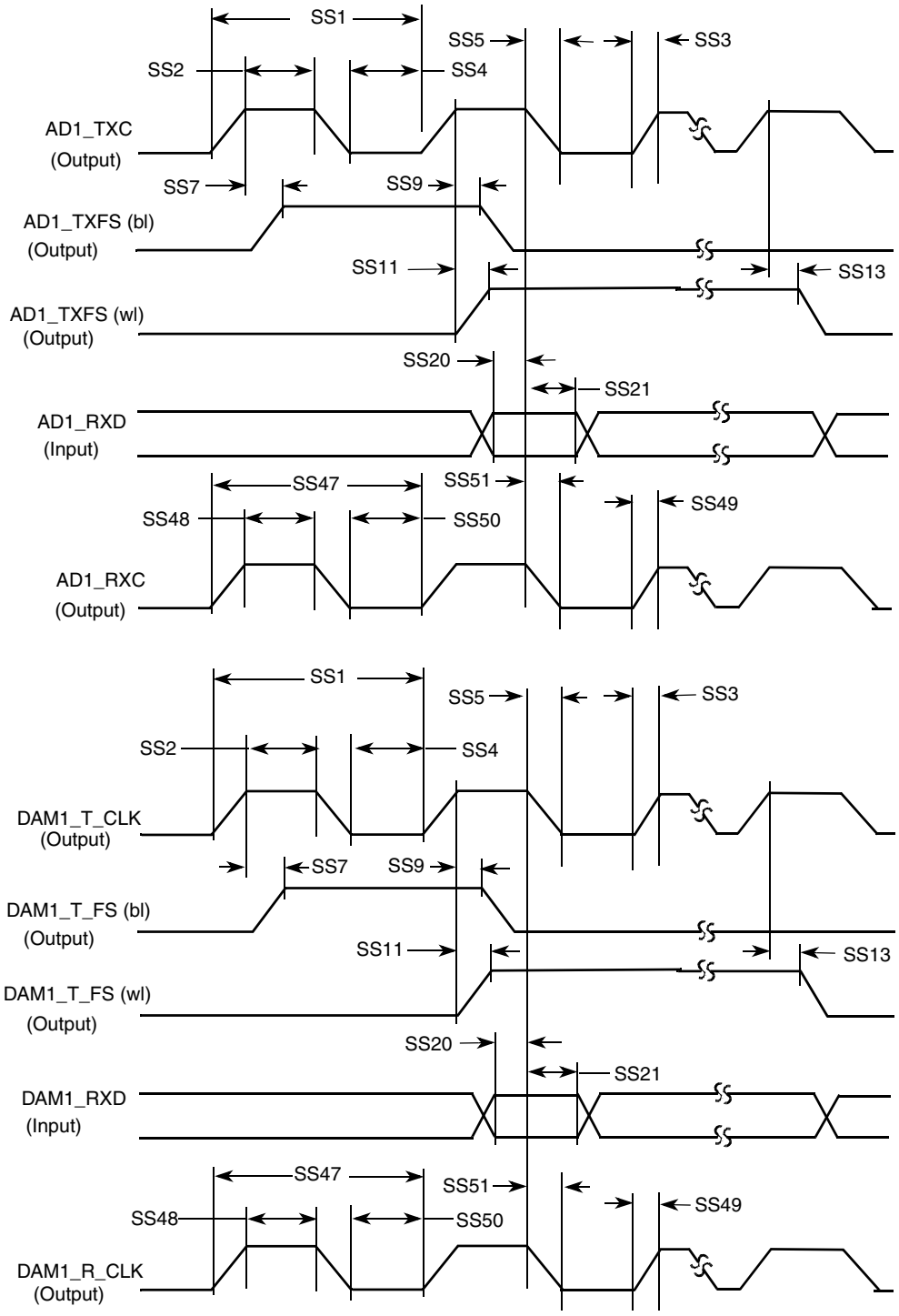
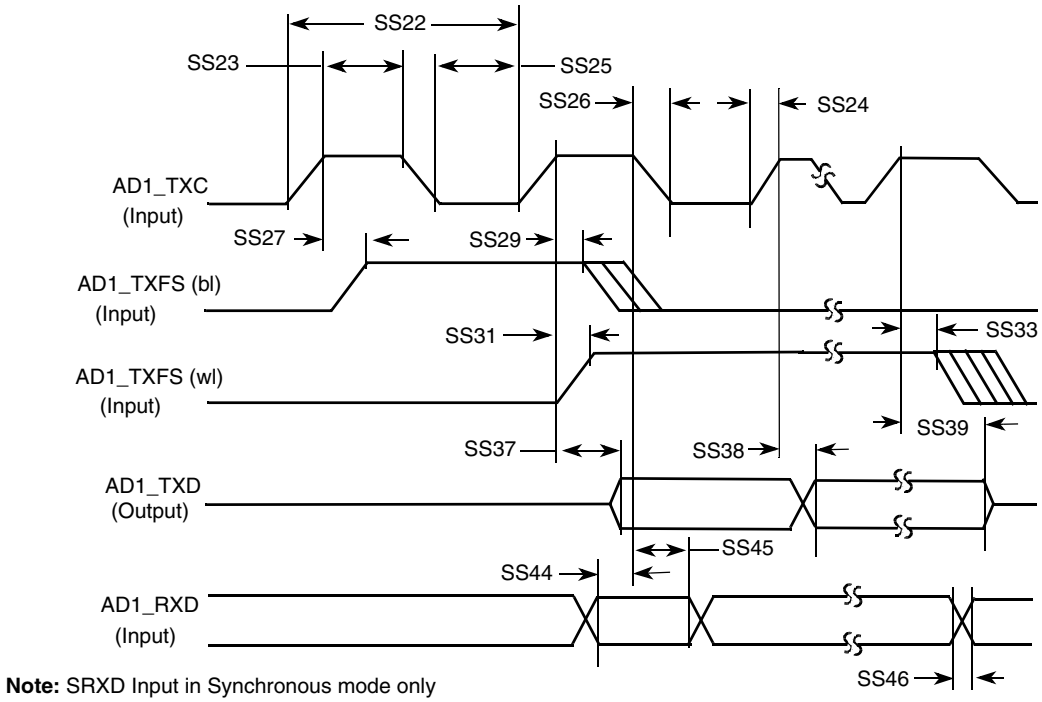


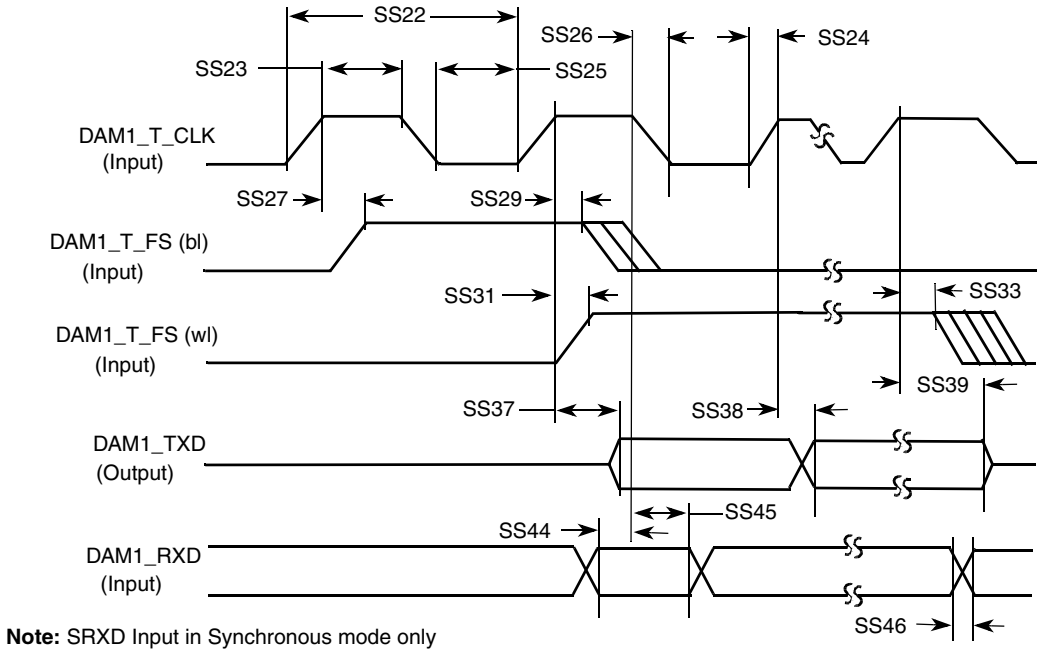
Figure 82. SSI Receiver with Internal Clock Timing Diagram

4.3.22.3 SSI Transmitter Timing with External Clock

Figure 83 depicts the SSI transmitter timing with external clock, and Table 62 lists the timing parameters.



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 83. SSI Transmitter with External Clock Timing Diagram

Table 63. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 85 depicts the USB ULPI timing diagram, and Table 64 lists the timing parameters.

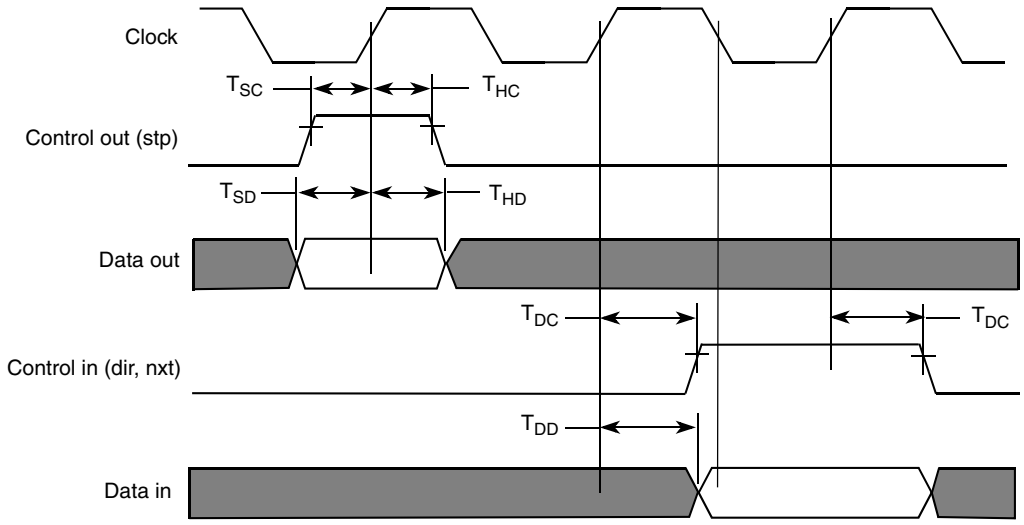


Figure 85. USB ULPI Interface Timing Diagram

Table 64. USB ULPI Interface Timing Specification[1]

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	T_{SC}, T_{SD}	6	—	ns
Hold time (control in, 8-bit data in)	T_{HC}, T_{HD}	0	—	ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	—	9	ns

1 Timing parameters are given as viewed by transceiver side.

Table 73. Product Differentiation (continued)

Item	Location	MCIMX31/MCIMX31L	MCIMX31C/MCIMX31LC
GPIO maximum input current (100 kΩ PU)	Table 15, "GPIO DC Electrical Parameters," on page 22	V_I = 0, I_{IN} = 25 μA V_I = NVCC, I_{IN} = 0.1 μA	N/A N/A
Core operating speed	Table 8, "Operating Ranges," on page 13	532 MHz	400 MHz
Package	Table 70, "Ball Map—14 x 14 0.5 mm Pitch," on page 117 and Table 71, "Ball Map—19 x 19 0.8 mm Pitch," on page 118	MAPBGA Packages 457 14 x 14 mm, 0.5 mm Pitch 473 19 x 19 mm, 0.8 mm Pitch	MAPBGA Package 473 19 x 19 mm, 0.8 mm Pitch
Pin Assignment	Table 66, "14 x 14 BGA Signal ID by Ball Grid Location," on page 107 and Table 69, "19 x 19 BGA Signal ID by Ball Grid Location," on page 113	MAPBGA Packages 457 14 x 14 mm, 0.5 mm Pitch 473 19 x 19 mm, 0.8 mm Pitch	MAPBGA Package 473 19 x 19 mm, 0.8 mm Pitch

7 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

MCIMX31 Product Brief (order number MCIMX31PB)

MCIMX31 Reference Manual (order number MCIMX31RM)

MCIMX31 Chip Errata (order number MCIMX31CE)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. ARM Ltd. documentation is available from http://www.arm.com.

8 Revision History

Table 74 summarizes revisions to this document since the release of Rev. 3.4.

Table 74. Revision History

Rev.	Location	Revision
4	Figure 87, Table 73	Updated.
4.1	Table 1, "Ordering Information," on page 3	Added note about JTAG compliance.
4.1	Section 1.2.1/3	Updated with new operating frequencies
4.1	Table 8, "Operating Ranges," on page 13	Added new operating frequencies