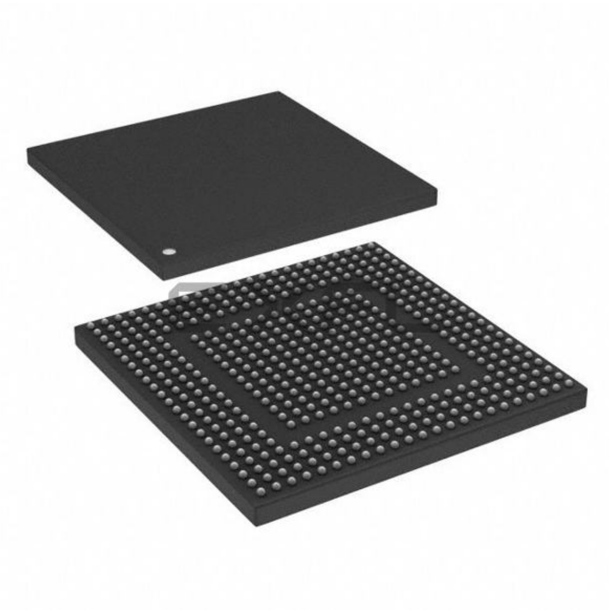

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-LFBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31lvmn5cr2

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
SCC	Security Controller Module	Security	The SCC is a hardware component composed of two blocks—the Secure RAM module, and the Security Monitor. The Secure RAM provides a way of securely storing sensitive information.	—
SDHC	Secured Digital Host Controller	Connectivity Peripheral	The SDHC controls the MMC (MultiMediaCard), SD (Secure Digital) memory, and I/O cards by sending commands to cards and performing data accesses to and from the cards.	4.3.19/89
SDMA	Smart Direct Memory Access	System Control Peripheral	The SDMA controller maximizes the system's performance by relieving the ARM core of the task of bulk data transfer from memory to memory or between memory and on-chip peripherals.	—
SIM	Subscriber Identification Module	Connectivity Peripheral	The SIM interfaces to an external Subscriber Identification Card. It is an asynchronous serial interface adapted for Smart Card communication for e-commerce applications.	4.3.20/90
SJC	Secure JTAG Controller	Debug	The SJC provides debug and test control with maximum security and provides a flexible architecture for future derivatives or future multi-cores architecture.	4.3.21/94
SSI	Synchronous Serial Interface	Multimedia Peripheral	The SSI is a full-duplex, serial port that allows the device to communicate with a variety of serial devices, such as standard codecs, Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.	4.3.22/96
UART	Universal Asynchronous Receiver/Transmitter	Connectivity Peripheral	The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.	—
USB	Universal Serial Bus— 2 Host Controllers and 1 OTG (On-The-Go)	Connectivity Peripherals	• USB Host 1 is designed to support transceiverless connection to the on-board peripherals in Low Speed and Full Speed mode, and connection to the ULPI (UTMI+ Low-Pin Count) and Legacy Full Speed transceivers. • USB Host 2 is designed to support transceiverless connection to the Cellular Modem Baseband Processor. • The USB-OTG controller offers HS/FS/LS capabilities in Host mode and HS/FS in device mode. In Host mode, the controller supports direct connection of a FS/LS device (without external hub). In device (bypass) mode, the OTG port functions as gateway between the Host 1 Port and the OTG transceiver.	4.3.23/104
WDOG	Watchdog Timer Module	Timer Peripheral	The WDOG module protects against system failures by providing a method for the system to recover from unexpected events or programming errors.	—

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31 (worst-case scenario)

4.2.1 Powering Up

The Power On Reset ($\overline{\text{POR}}$) pin must be kept asserted (low) throughout the power up sequence. Power up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{\text{POR}}$. Figure 2 shows the power-up sequence for silicon Revisions 1.2 and previous. Figure 3 and Figure 4 show the power-up sequence for silicon Revision 2.0.

NOTE

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

4.3.4 1-Wire Electrical Specifications

Figure 7 depicts the RPP timing, and Table 21 lists the RPP timing parameters.

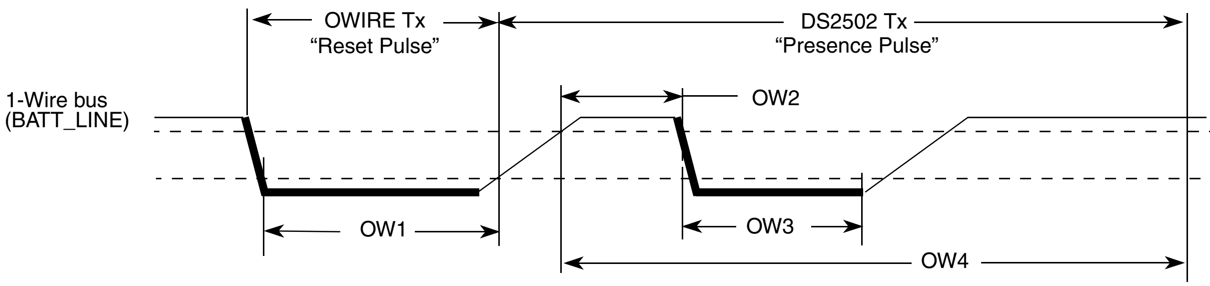

Figure 7. Reset and Presence Pulses (RPP) Timing Diagram

Table 21. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 8 depicts Write 0 Sequence timing, and Table 22 lists the timing parameters.

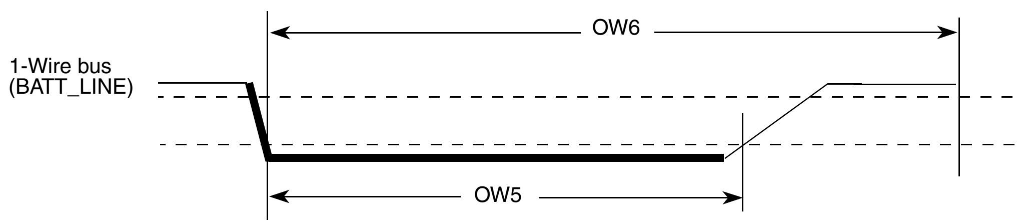

Figure 8. Write 0 Sequence Timing Diagram

Table 22. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Units
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

Figure 9 depicts Write 1 Sequence timing, Figure 10 depicts the Read Sequence timing, and Table 23 lists the timing parameters.

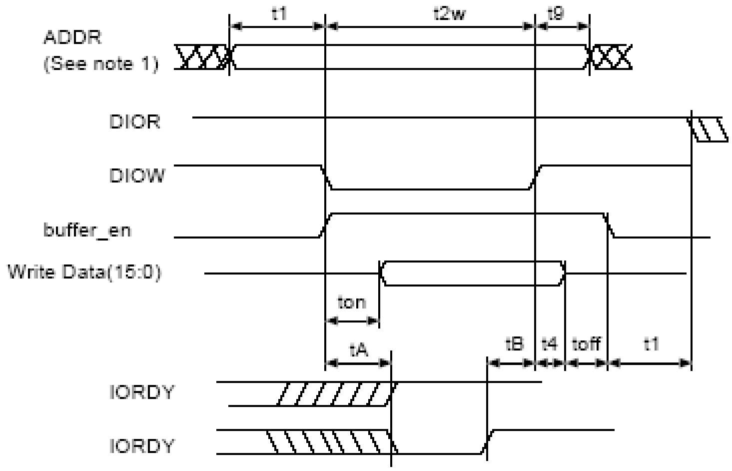

Figure 12. Multiword DMA (MDMA) Timing

Table 26. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 12	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w * T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 * T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 13 shows timing for MDMA read, Figure 14 shows timing for MDMA write, and Table 27 lists the timing parameters for MDMA read and write.

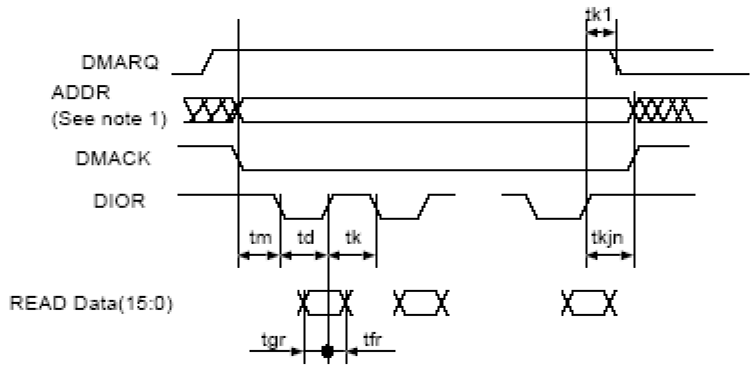

Figure 13. MDMA Read Timing Diagram

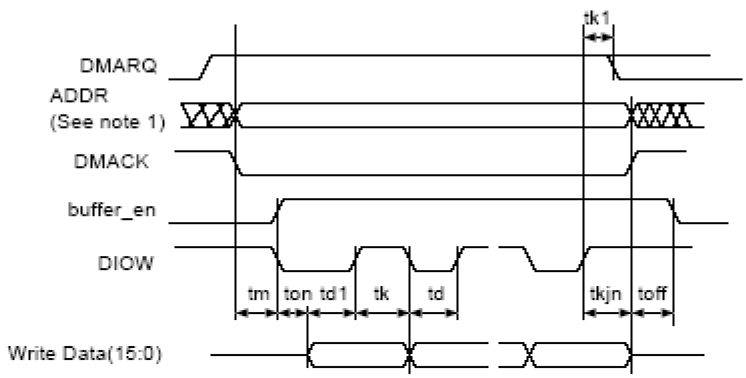

Figure 14. MDMA Write Timing Diagram

Table 27. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 13, Figure 14	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

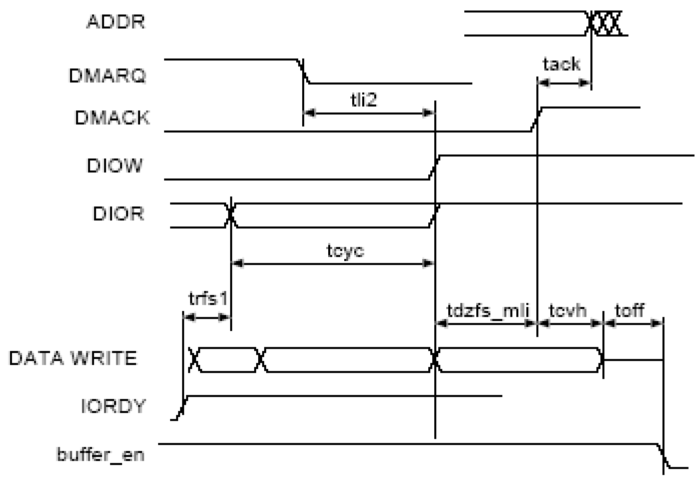

Figure 20. UDMA Out Device Terminates Transfer Timing Diagram

Table 29. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 18, Figure 19, Figure 20	Value	Controlling Variable
tack	tack	tack (min) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env * T) – (tskew1 + tskew2) tenv (max) = (time_env * T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs * T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh * T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc * T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc * 2 * T	time_cyc
trfs1	trfs	trfs = 1.6 * T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs * T – (tskew1)	time_dzfs
tss	tss	tss = time_ss * T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) * T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

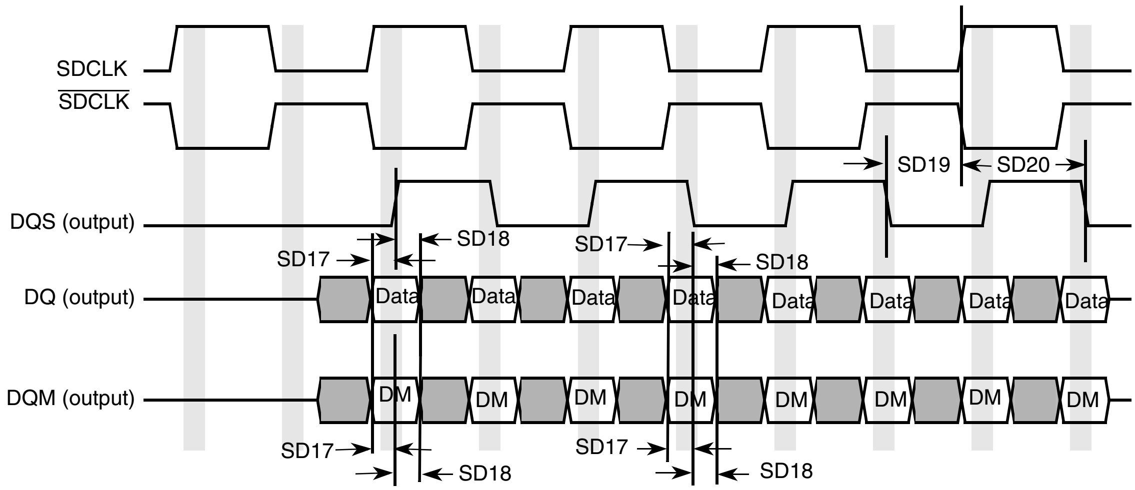

Figure 38. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 38. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min	Max	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 38 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

The timing described in Figure 44 is that of a Motorola sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.3.14.3 Electrical Characteristics

Figure 45 depicts the sensor interface timing, and Table 45 lists the timing parameters.

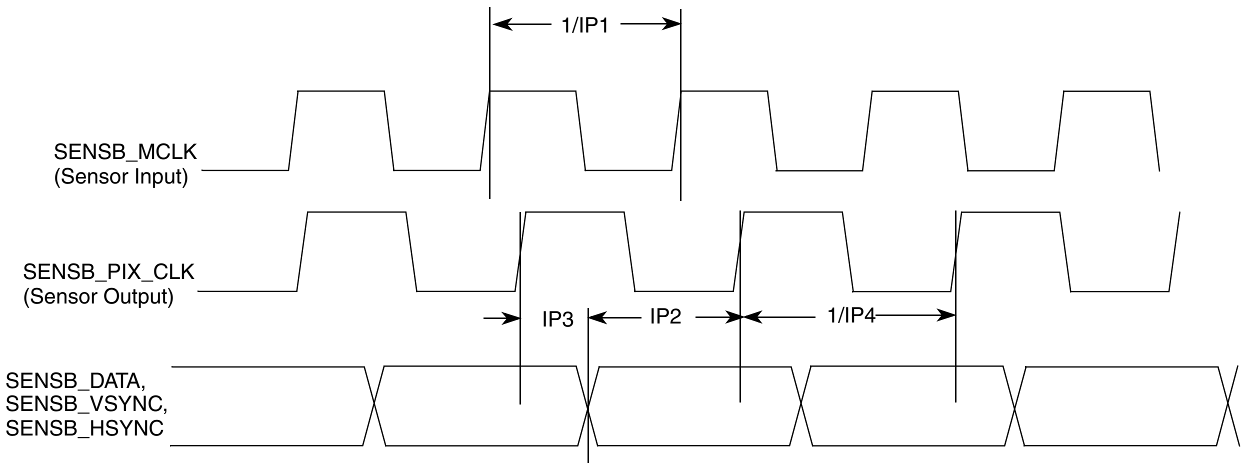

Figure 45. Sensor Interface Timing Diagram

Table 45. Sensor Interface Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

[1] The timing specifications for Figure 45 are referenced to the rising edge of SENS_PIX_CLK when the SENS_PIX_CLK_POL bit in the CSI_SENS_CONF register is cleared. When the SENS_PIX_CLK_POL is set, the clock is inverted and all timing specifications will remain the same but are referenced to the falling edge of the clock.

4.3.15 IPU—Display Interfaces

4.3.15.1 Supported Display Components

Table 46 lists the known supported display components at the time of publication.

[2] Display interface clock down time

$$\mathrm{Tdicd} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP3\_IF\_CLK\_DOWN\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[3] Display interface clock up time

$$\mathrm{Tdicu} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP3\_IF\_CLK\_UP\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

4.3.15.3 Interface to Sharp HR-TFT Panels

Figure 50 depicts the Sharp HR-TFT panel interface timing, and Table 49 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics." The timing images correspond to straight polarity of the Sharp signals.

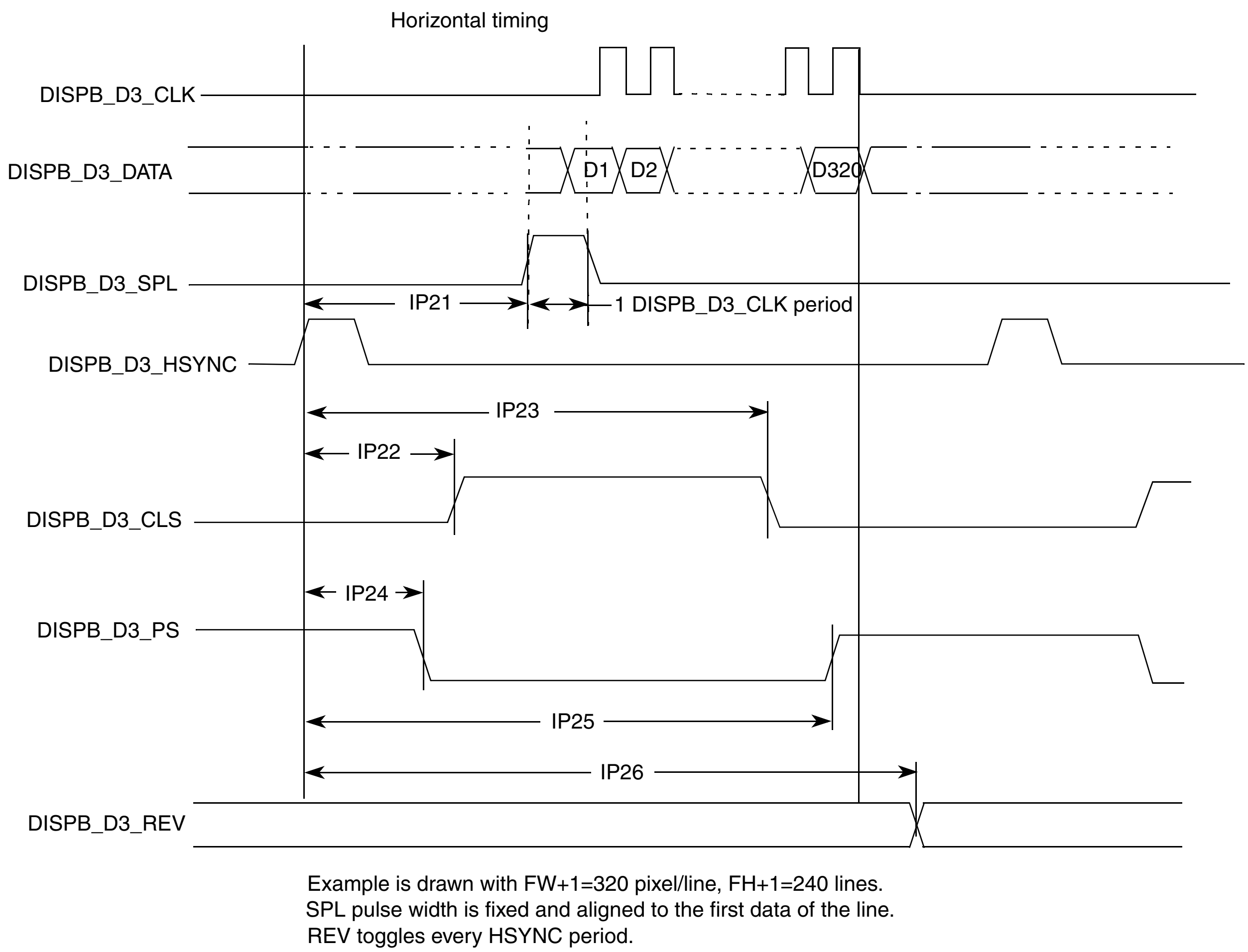

Figure 50. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

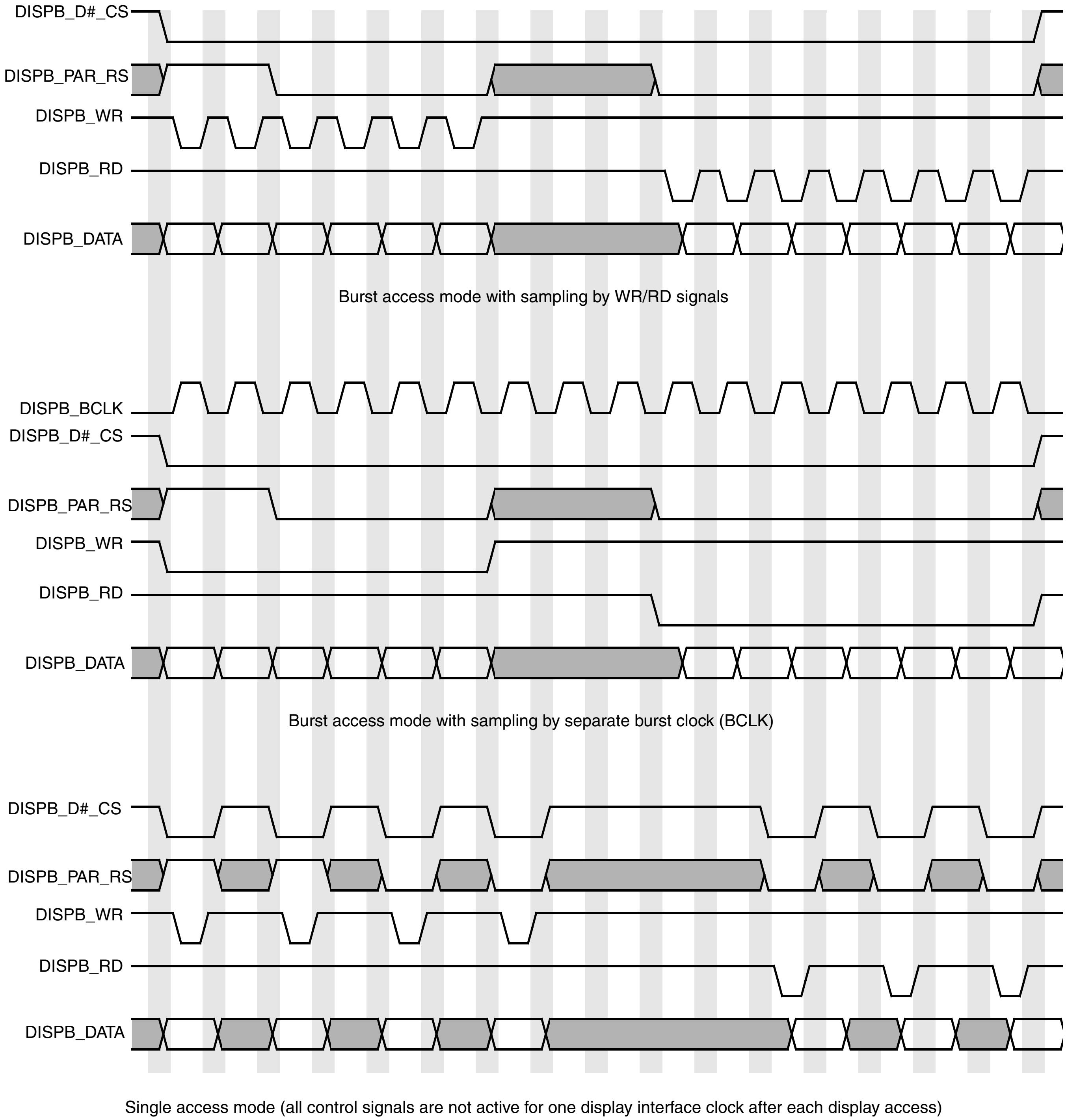

Figure 53. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

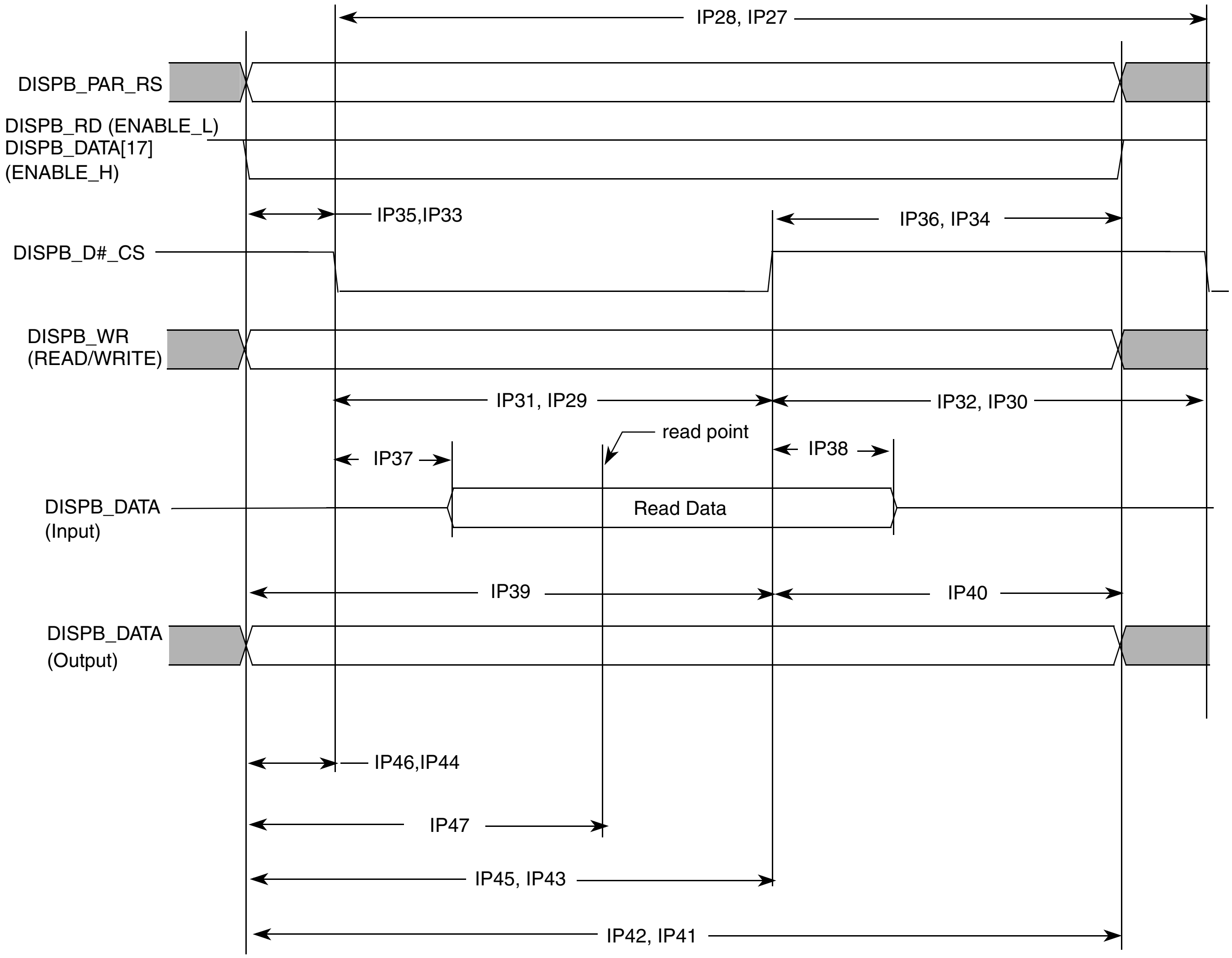

Figure 59. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

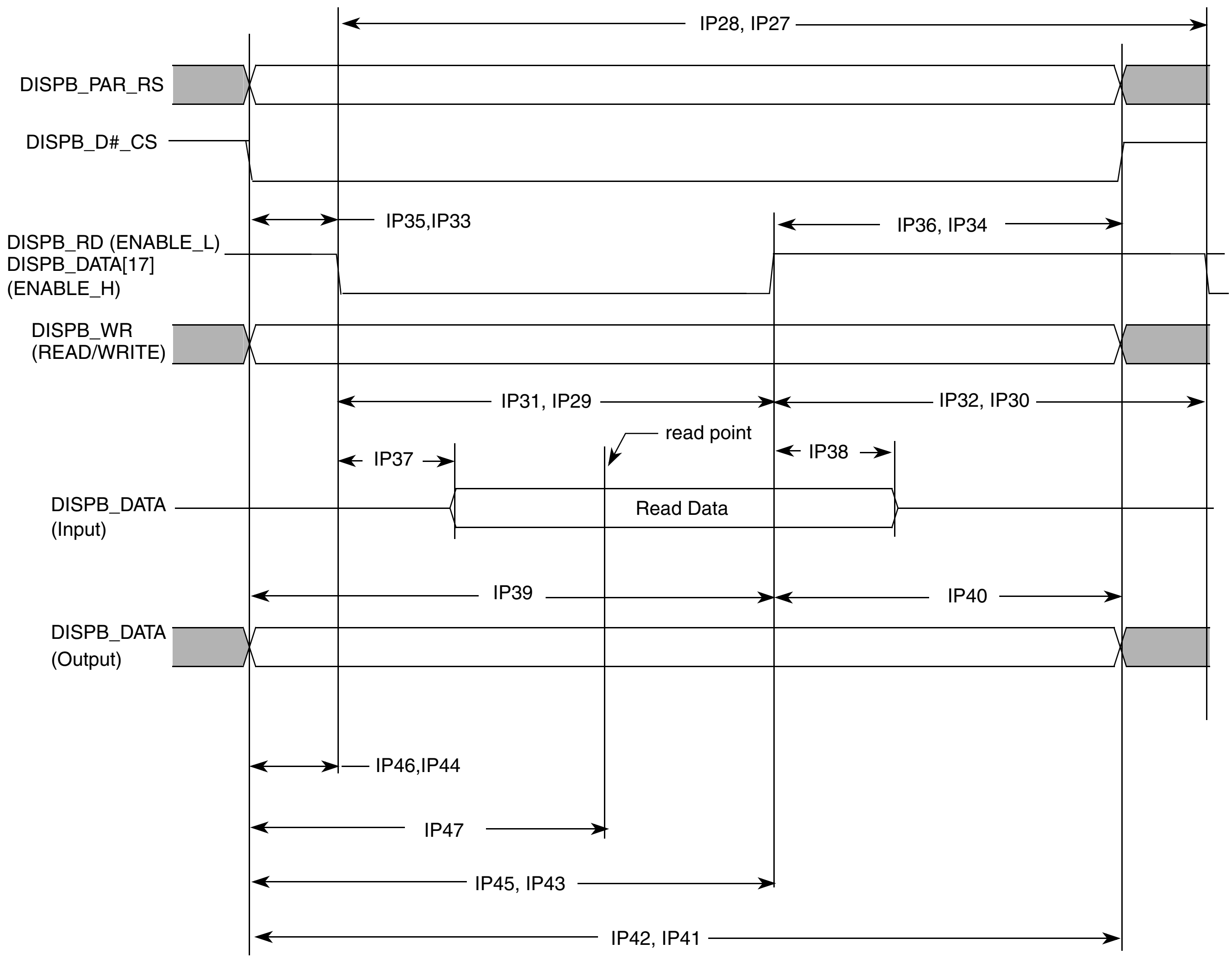

Figure 60. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Table 50. Asynchronous Parallel Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP29	Read low pulse width	Trl	Tdicdr–Tdicur–1.5	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.5	ns
IP30	Read high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.5	Tdicpr–Tdicdr+ Tdicur	Tdicpr–Tdicdr+Tdicur+1.5	ns
IP31	Write low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP32	Write high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP34	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns
IP35	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

4.3.15.5.3 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 61 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux should provide joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP1_CONF and DI_SER_DISP2_CONF Registers.

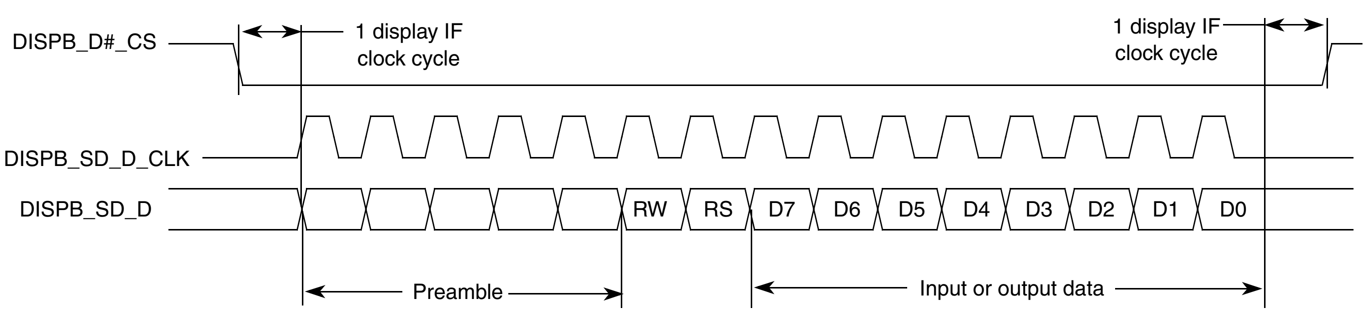

Figure 61. 3-Wire Serial Interface Timing Diagram

Figure 62 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

Figure 64 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

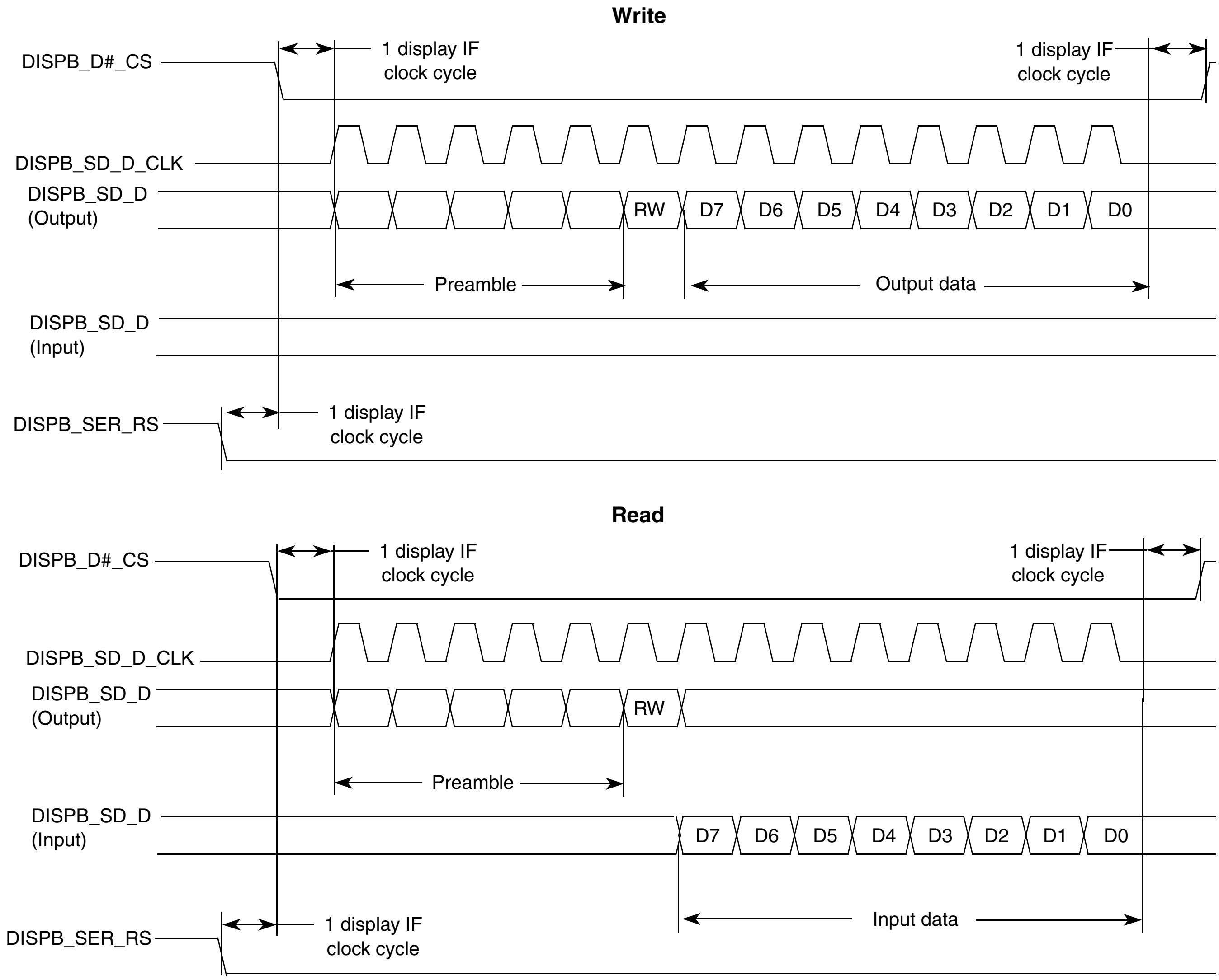

Figure 64. 5-Wire Serial Interface (Type 2) Timing Diagram

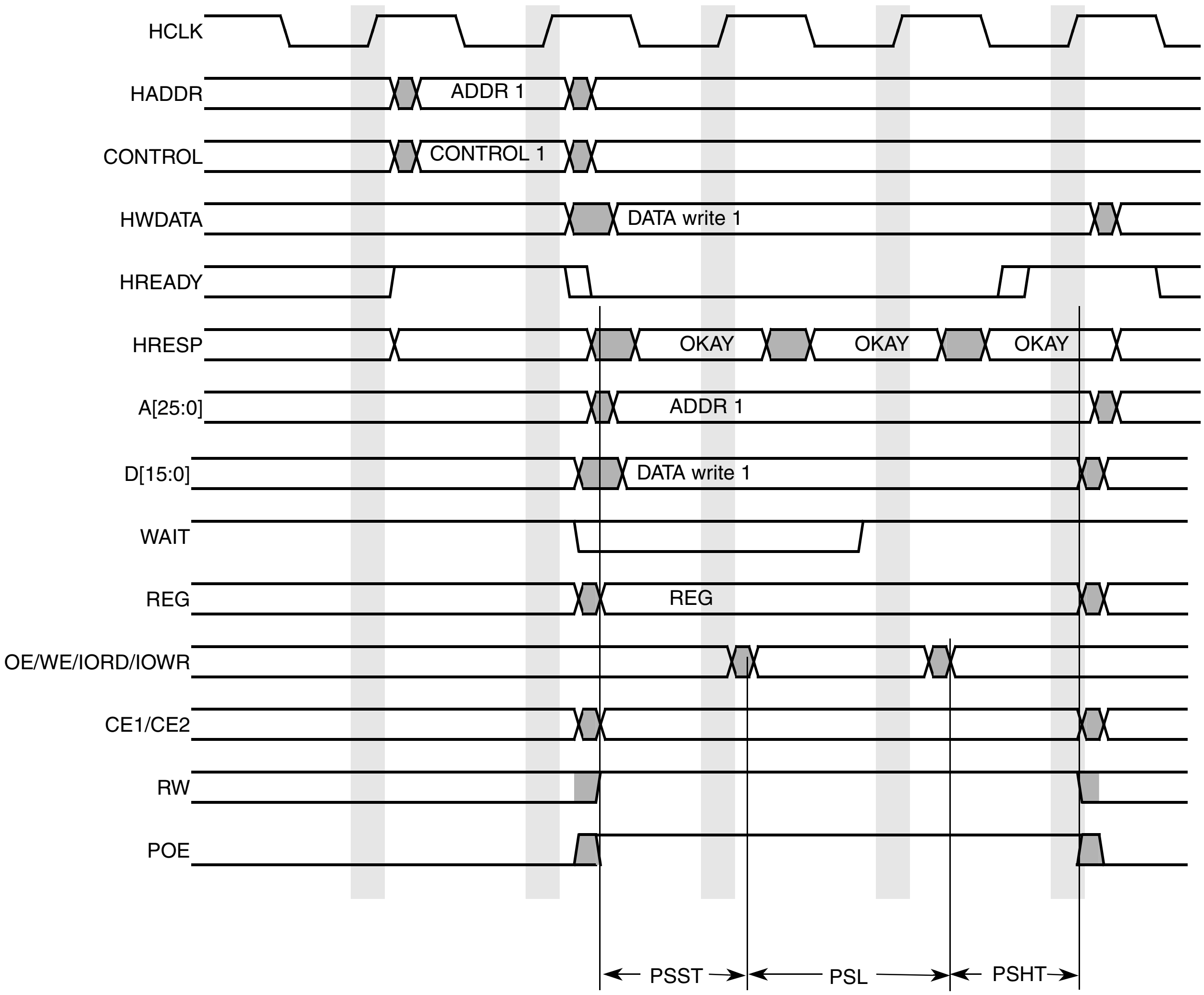

Figure 69. Write Accesses Timing Diagram—PSHT=1, PSST=1

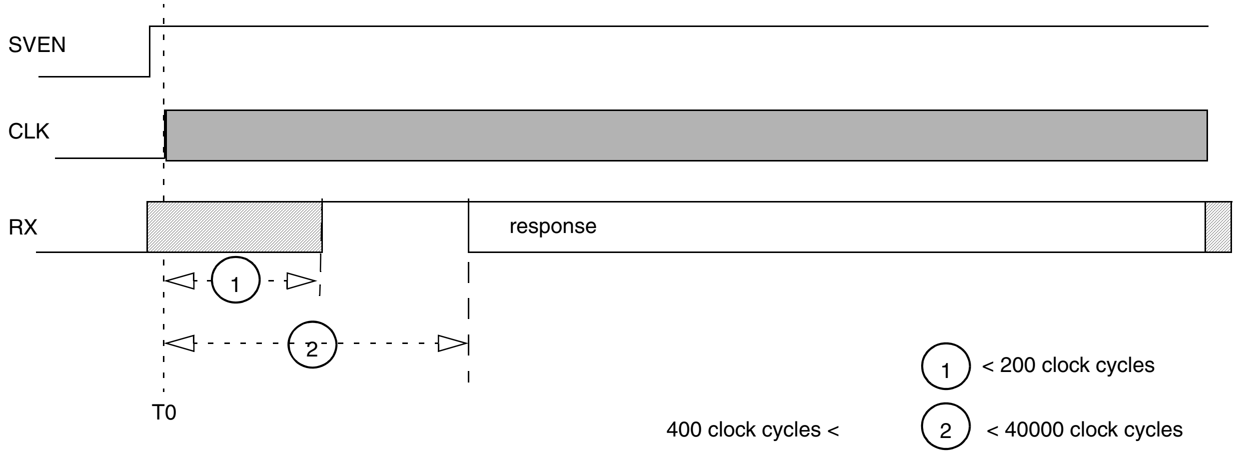

Figure 74. Internal-Reset Card Reset Sequence

4.3.20.2.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 75):

1. After powerup, the clock signal is enabled on CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
4. RST is set High (time T1)
5. RST must remain High for at least 40000 clock cycles after T1 and a response must be received on RX between 400 and 40000 clock cycles after T1.

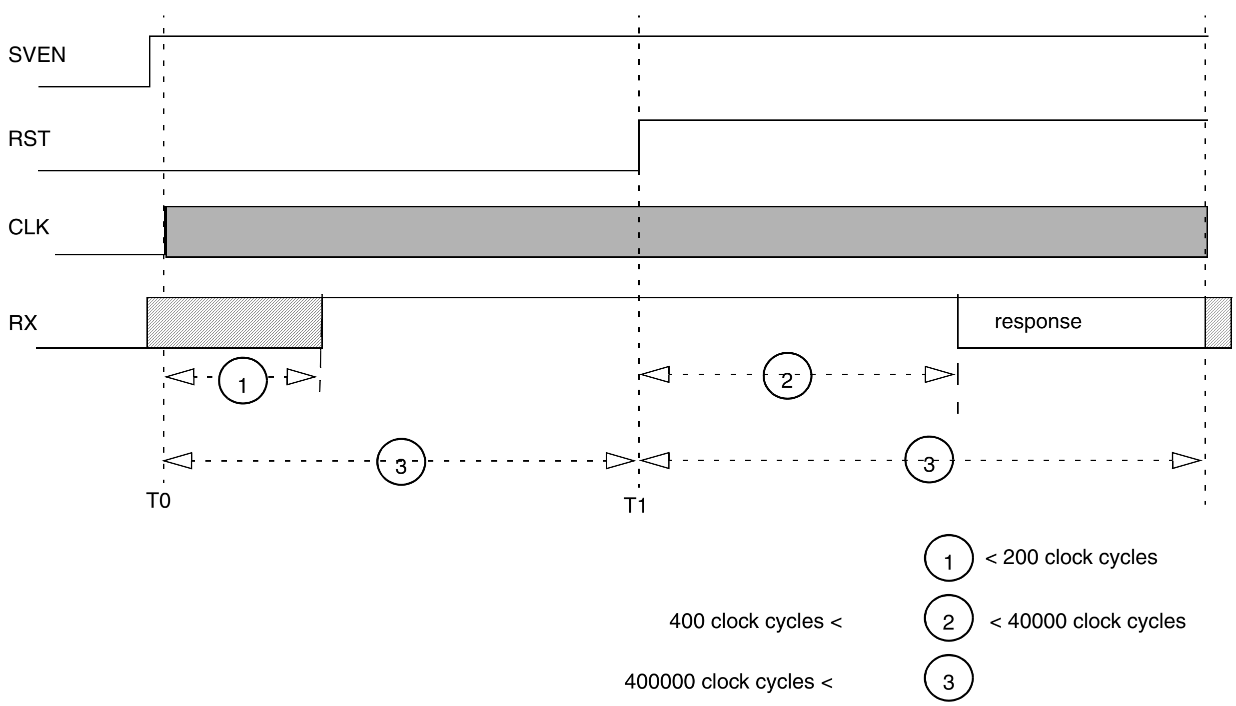

Figure 75. Active-Low-Reset Card Reset Sequence

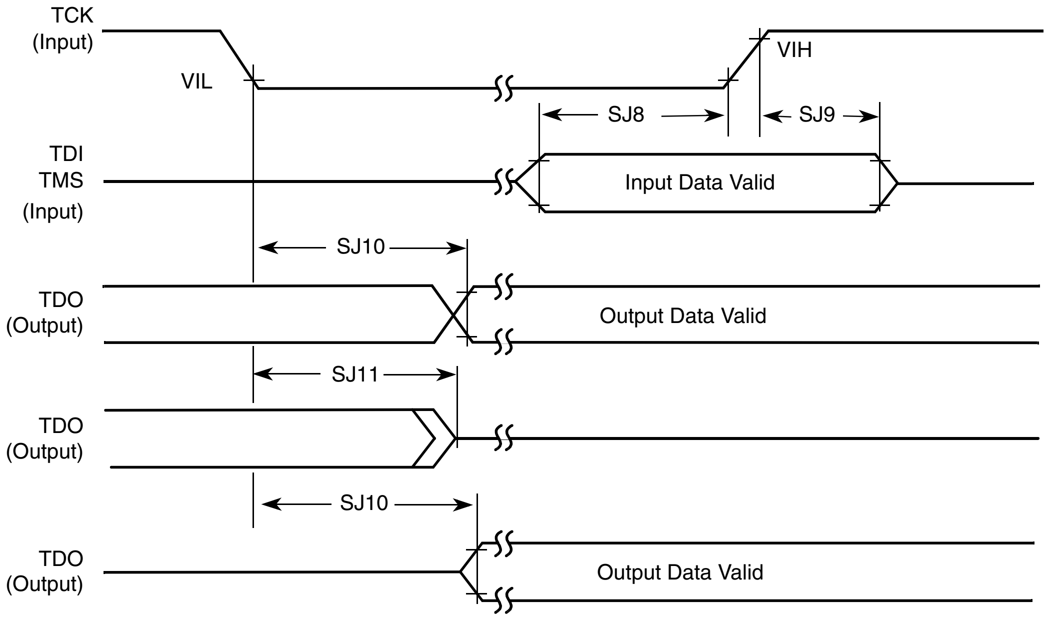

Figure 79. Test Access Port Timing Diagram

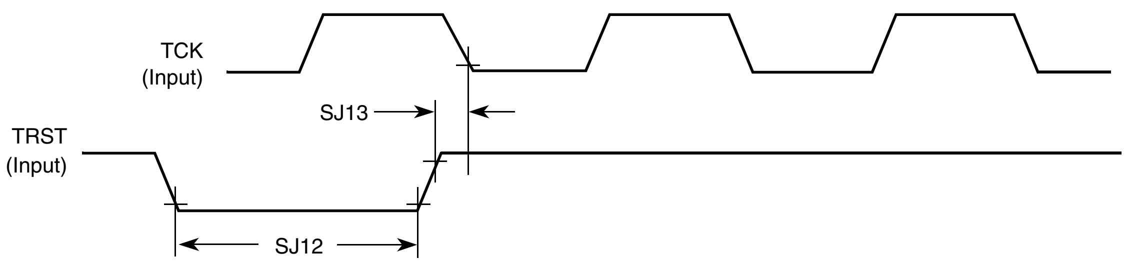

Figure 80. $\overline{\text{TRST}}$ Timing Diagram

Table 59. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min	Max	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

5.2 MAPBGA Production Package—473 19 x 19 mm, 0.8 mm Pitch

This section contains the outline drawing, signal assignment map (see Section 8, "Revision History," Table 71 for the 19 x 19 mm, 0.8 mm pitch signal assignments), and MAPBGA ground/power ID by ball grid location for the 473 19 x 19 mm, 0.8 mm pitch package.

5.2.1 Production Package Outline Drawing–19 x 19 mm 0.8 mm

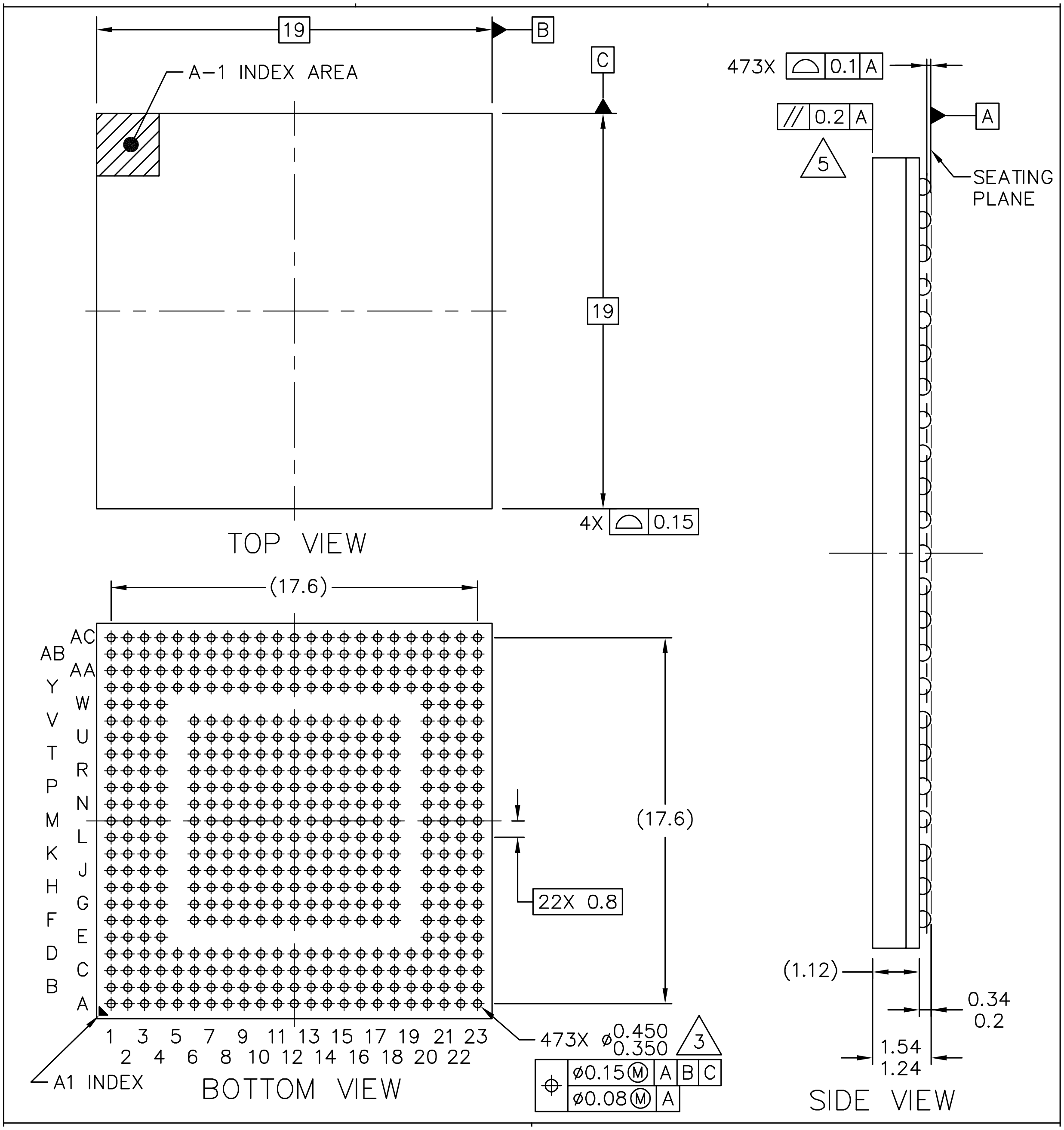

Figure 87. Production Package: Case 1931—0.8 mm Pitch

Table 68. 19 x 19 BGA No Connects[1]

Signal	Ball Location
NC	N7
NC	P7
NC	U21

1 These contacts are not used and must be floated by the user.

5.2.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location	Signal ID	Ball Location
A0	Y6	CKIL	E21
A1	AC5	CLKO	C20
A10	V15	CLKSS	H17
A11	AB3	COMPARE	A20
A12	AA3	CONTRAST	N21
A13	Y3	CS0	U17
A14	Y15	CS1	Y22
A15	Y14	CS2	Y18
A16	V14	CS3	Y19
A17	Y13	CS4	Y20
A18	V13	CS5	AA21
A19	Y12	CSI_D10	K21
A2	AB5	CSI_D11	K22
A20	V12	CSI_D12	K23
A21	Y11	CSI_D13	L20
A22	V11	CSI_D14	L18
A23	Y10	CSI_D15	L21
A24	Y9	CSI_D4	J20
A25	Y8	CSI_D5	J21
A3	AA5	CSI_D6	L17
A4	Y5	CSI_D7	J22
A5	AC4	CSI_D8	J23
A6	AB4	CSI_D9	K20
A7	AA4	CSI_HSYNC	H22
A8	Y4	CSI_MCLK	H20
A9	AC3	CSI_PIXCLK	H23
ATA_CS0	E1	CSI_VSYNC	H21
ATA_CS1	G4	CSPI1_MISO	N2
ATA_DIOR	E3	CSPI1_MOSI	N1
ATA_DIOW	H6	CSPI1_SCLK	M4
ATA_DMACK	E2	CSPI1_SPI_RDY	M1
$\overline{\text{ATA\_RESET}}$	F3	CSPI1_SS0	M2
BATT_LINE	F6	CSPI1_SS1	N6
BCLK	W20	CSPI1_SS2	M3
BOOT_MODE0	F17	CSPI2_MISO	B4
BOOT_MODE1	C21	CSPI2_MOSI	D5

6 Product Differences

The locations that provide the differences between silicon Revision 2.0, 1.2, and previous versions are given in Table 72. The differences between the MCIMX31/MCIMX31L and the MCIMX31C/MCIMX31LC are outlined in Table 73.

Table 72. Silicon Differentiation by Location within the Data Sheet

Item	Location	Silicon 1.2 and Previous	Silicon 2.0
Ordering Information	Section 1.2, "Ordering Information	Table 1	Table 1
Feature Differences	Table 1.2.1, "Feature Differences Between Mask Sets," on page 3	N/A	Table 1.2.1
Operating Ranges	Table 4.1, "Chip-Level Conditions," on page 10	Table 8, "Operating Ranges," on page 13	Table 8, and Table 9, "Specific Operating Ranges for Silicon Revision 2.0," on page 14
Power-up Sequences	Section 4.2.1, "Powering Up	Figure 2, "Power-Up Sequence for Silicon Revisions 1.2 and Previous," on page 20	Figure 3, "Option 1 Power-Up Sequence (Silicon Revision 2.0)," on page 21
Power-down Sequences	Section 4.2.2, "Powering Down	—	—

Table 73. Product Differentiation

Item	Location	MCIMX31/MCIMX31L	MCIMX31C/MCIMX31LC
Device ordering information	Table 1, "Ordering Information," on page 3	See Table 1.	See Table 1.
Thermal simulation values	Table 6, "Thermal Resistance Data—14 × 14 mm Package," on page 11 and Table 7, "Thermal Resistance Data—19 × 19 mm Package," on page 11	See Table 6 and Table 7.	See Table 7.
Core overdrive operating voltages	Table 8, "Operating Ranges," on page 13	Capability to operate in overdrive voltages.	Not capable of overdrive operating voltages.
Fuse_VDD	Table 8, "Operating Ranges," on page 13 and Table 9, "Specific Operating Ranges for Silicon Revision 2.0," on page 14	Fusebox read Supply Voltage 1.65 min, 1.95 max.	In read mode, FUSE_VDD should be floated.
Ambient operating temperature range	Table 13, "Current Consumption for –40×C to 85×C, for Silicon Revision 2.0," on page 17, and Table 14, "Current Consumption for 0×C to 70×C, for Silicon Revision 2.0," on page 18	0°C min, 70°C max –40°C min, 85°C max	–40°C min, 85°C max
Current consumption values	Table 13, "Current Consumption for –40×C to 85×C, for Silicon Revision 2.0," on page 17	Typical value changes for State Retention, Doze, and Wait. See Table.	Typical value changes for State Retention, Doze, and Wait. See Table.
DPLL maximum output freq range	Table 31, "DPLL Specifications," on page 37	MPLL and SPLL = 532 MHz	MPLL and SPLL = 400 MHz