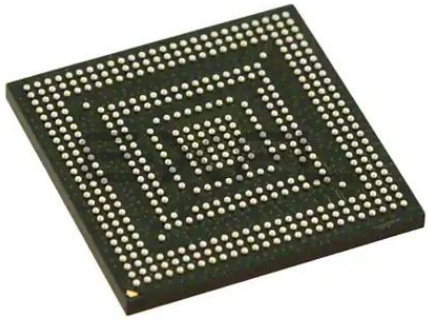

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31vkn5br2

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31.

Table 1. Ordering Information

Part Number	Silicon Revision[1, 2, 3,4]	Device Mask	Operating Temperature Range (°C)	Package[5]
MCIMX31VKN5	1.15	2L38W and 3L38W	0 to 70	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LVKN5	1.15	2L38W and 3L38W	0 to 70	
MCIMX31VKN5B	1.2	M45G	0 to 70	
MCIMX31LVKN5B	1.2	M45G	0 to 70	
MCIMX31VKN5C	2.0	M91E	0 to 70	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LVKN5C	2.0	M91E	0 to 70	
MCIMX31CVKN5C	2.0	M91E	–40 to 85	
MCIMX31LCVKN5C	2.0	M91E	–40 to 85	
MCIMX31VMN5C	2.0	M91E	0 to 70	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LVMN5C	2.0	M91E	0 to 70	

1 Information on reading the silicon revision register can be found in the IC Identification (IIM) chapter of the Reference Manual, see Section 7, "Product Documentation."

2 Errata and fix information of the various mask sets can be found in the standard MCIMX31 Chip Errata, see Section 7, "Product Documentation."

3 Changes in output buffer characteristics can be found in the I/O Setting Exceptions and Special Pad Descriptions table in the Reference Manual, see Section 7, "Product Documentation."

4 JTAG functionality is not tested nor guaranteed at -40°C.

5 Case 1581 and 1931 are RoHS compliant, lead-free, MSL = 3, and solders at 260°C.

1.2.1 Feature Differences Between Mask Sets

The following is a summary of differences between silicon Revision 2.0, mask set M91E, and previous revisions of silicon. A complete list of these differences is given in Table 72.

- Extended operating temperature range is available: –40°C to 85°C
- Supply current information changes, as shown in Table 13 and Table 14
- FUSE_VDD supply voltage is floated or grounded during read operation
- No restriction on PLL versus core supply voltage
- Operating frequency as shown in Table 8.

2.2 Module Inventory

Table 3 shows an alphabetical listing of the modules in the multimedia applications processor. For extended descriptions of the modules, see the reference manual. A cross-reference is provided to the electrical specifications and timing information for each module with external signal connections.

Table 3. Digital and Analog Modules

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
1-Wire®	1-Wire Interface	Connectivity Peripheral	The 1-Wire module provides bi-directional communication between the ARM11 core and external 1-Wire devices.	4.3.4/26
ATA	Advanced Technology (AT) Attachment	Connectivity Peripheral	The ATA block is an AT attachment host interface. It is designed to interface with IDE hard disc drives and ATAPI optical disc drives.	4.3.5/27
AUDMUX	Digital Audio Multiplexer	Multimedia Peripheral	The AUDMUX interconnections allow multiple, simultaneous audio/voice/data flows between the ports in point-to-point or point-to-multipoint configurations.	4.3.6/36
CAMP	Clock Amplifier Module	Clock	The CAMP converts a square wave/sinusoidal input into a rail-to-rail square wave. The output of CAMP feeds the predivider.	4.3.3/25
CCM	Clock Control Module	Clock	The CCM provides clock, reset, and power management control for the MCIMX31.	—
CSPI	Configurable Serial Peripheral Interface (x 3)	Connectivity Peripheral	The CSPI is equipped with data FIFOs and is a master/slave configurable serial peripheral interface module, capable of interfacing to both SPI master and slave devices.	4.3.7/36
DPLL	Digital Phase Lock Loop	Clock	The DPLLs produce high-frequency on-chip clocks with low frequency and phase jitters. **Note:** External clock sources provide the reference frequencies.	4.3.8/37
ECT	Embedded Cross Trigger	Debug	The ECT is composed of three CTIs (Cross Trigger Interface) and one CTM (Cross Trigger Matrix—key in the multi-core and multi-peripheral debug strategy.	—
EMI	External Memory Interface	Memory Interface (EMI)	The EMI includes • Multi-Master Memory Interface (M3IF) • Enhanced SDRAM Controller (ESDCTL) • NAND Flash Controller (NFC) • Wireless External Interface Module (WEIM)	— 4.3.9.3/46, 4.3.9.1/38, 4.3.9.2/41
EPIT	Enhanced Periodic Interrupt Timer	Timer Peripheral	The EPIT is a 32-bit “set and forget” timer which starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention.	—
ETM	Embedded Trace Macrocell	Debug/Trace	The ETM (from ARM, Ltd.) supports real-time instruction and data tracing by way of ETM auxiliary I/O port.	4.3.10/54
FIR	Fast InfraRed Interface	Connectivity Peripheral	This FIR is capable of establishing a 0.576 Mbit/s, 1.152 Mbit/s or 4 Mbit/s half duplex link via a LED and IR detector. It supports 0.576 Mbit/s, 1.152 Mbit/s medium infrared (MIR) physical layer protocol and 4Mbit/s fast infrared (FIR) physical layer protocol defined by IrDA, Rev. 1.4.	4.3.11/55

Table 31. DPLL Specifications (continued)

Parameter	Min	Typ	Max	Unit	Comments
Phase lock time	—	—	100	µs	In addition to the frequency
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ < 50 kHz
Maximum allowed PLL supply voltage ripple	—	—	20	mV	50 kHz < $F_{modulation}$ < 300 kHz
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ > 300 kHz
PLL output clock phase jitter	—	—	5.2	ns	Measured on CLKO pin
PLL output clock period jitter	—	—	420	ps	Measured on CLKO pin

1 The user or board designer must take into account that the use of a frequency other than 26 MHz would require adjustment to the DPTC–DVFS table, which is incorporated into operating system code.

2 The PLL reference frequency must be ≤ 35 MHz. Therefore, for frequencies between 35 MHz and 70 MHz, program the predivider to divide by 2 or more. If the CKIH frequency is above 70 MHz, program the predivider to 3 or more. For PD bit description, see the reference manual.

4.3.9 EMI Electrical Specifications

This section provides electrical parametrics and timings for EMI module.

4.3.9.1 NAND Flash Controller Interface (NFC)

The NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 23, Figure 24, Figure 25, and Figure 26 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 32 lists the timing parameters.

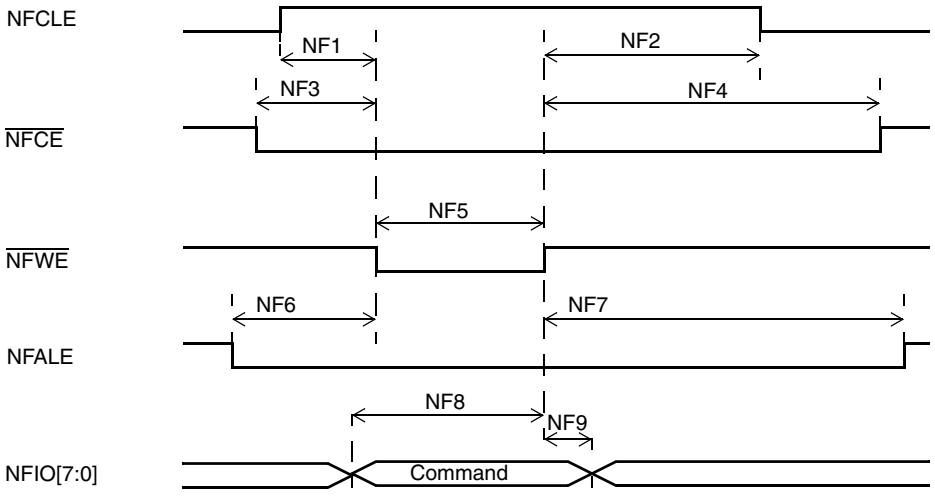

Figure 23. Command Latch Cycle Timing Diagram

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.3.9.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 27 depicts the timing of the WEIM module, and Table 33 lists the timing parameters.

Table 40. ETM TRACECLK Timing Parameters

ID	Parameter	Min	Max	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 41 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 41 lists the timing parameters.

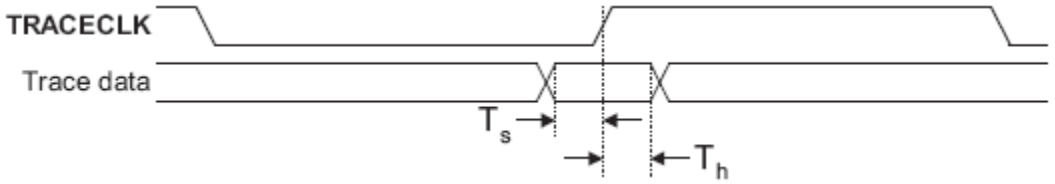

Figure 41. Trace Data Timing Diagram

Table 41. ETM Trace Data Timing Parameters

ID	Parameter	Min	Max	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.3.10.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 41.

4.3.11 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) that are defined by IrDA® (Infrared Data Association). Refer to http://www.IrDA.org for details on FIR and MIR protocols.

4.3.12 Fusebox Electrical Specifications

Table 42. Fusebox Timing Characteristics

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	Program time for eFuse[1]	$t_{program}$	125	—	—	µs

1 The program length is defined by the value defined in the epm_pgm_length[2:0] bits of the IIM module. The value to program is based on a 32 kHz clock source (4 * 1/32 kHz = 125 µs).

4.3.14 IPU—Sensor Interfaces

4.3.14.1 Supported Camera Sensors

Table 44 lists the known supported camera sensors at the time of publication.

Table 44. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI–SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors not validated at time of publication.

4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

NOTE

HSP_CLK is the High-Speed Port Clock, which is the input to the Image Processing Unit (IPU). Its frequency is controlled by the Clock Control Module (CCM) settings. The HSP_CLK frequency must be greater than or equal to the AHB clock frequency.

The SCREEN_WIDTH, SCREEN_HEIGHT, H_SYNC_WIDTH, V_SYNC_WIDTH, BGXP, BGYP and V_SYNC_WIDTH_L parameters are programmed via the SDC_HOR_CONF, SDC_VER_CONF, SDC_BG_POS Registers. The FW and FH parameters are programmed for the corresponding DMA channel. The DISP3_IF_CLK_PER_WR, HSP_CLK_PERIOD and DISP3_IF_CLK_CNT_D parameters are programmed via the DI_DISP3_TIME_CONF, DI_HSP_CLK_PER and DI_DISP_ACC_CC Registers.

Figure 49 depicts the synchronous display interface timing for access level, and Table 48 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

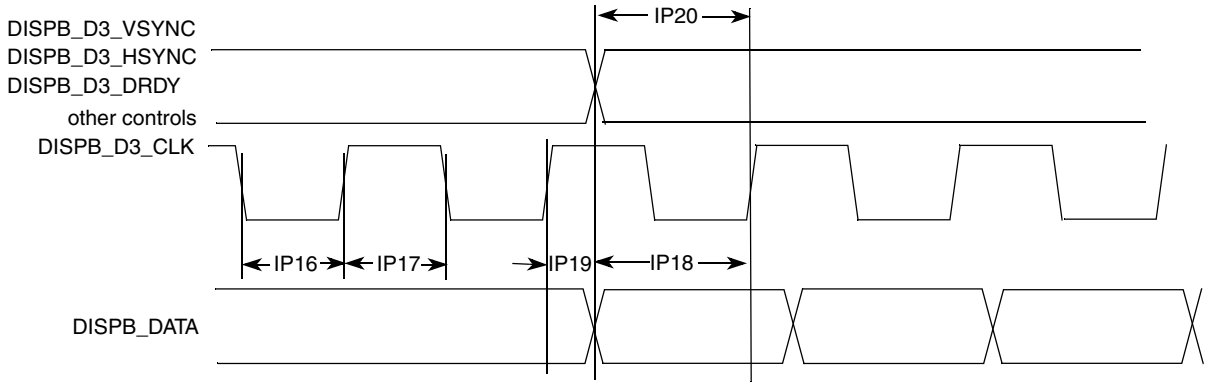

Figure 49. Synchronous Display Interface Timing Diagram—Access Level

Table 48. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min	Typ[1]	Max	Units
IP16	Display interface clock low time	Tckl	Tdicd–Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–3.5	Tdicp–Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd–3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

4.3.15.4.2 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics."

4.3.15.5 Asynchronous Interfaces

4.3.15.5.1 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock. The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) of by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals changes only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k) and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK. In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode. In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 52, Figure 53, Figure 54, and Figure 55. These timing images correspond to active-low DISPB_D#_CS, DISPB_D#_WR and DISPB_D#_RD signals.

Additionally, the IPU allows a programmable pause between two burst. The pause is defined in the HSP_CLK cycles. It allows to avoid timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

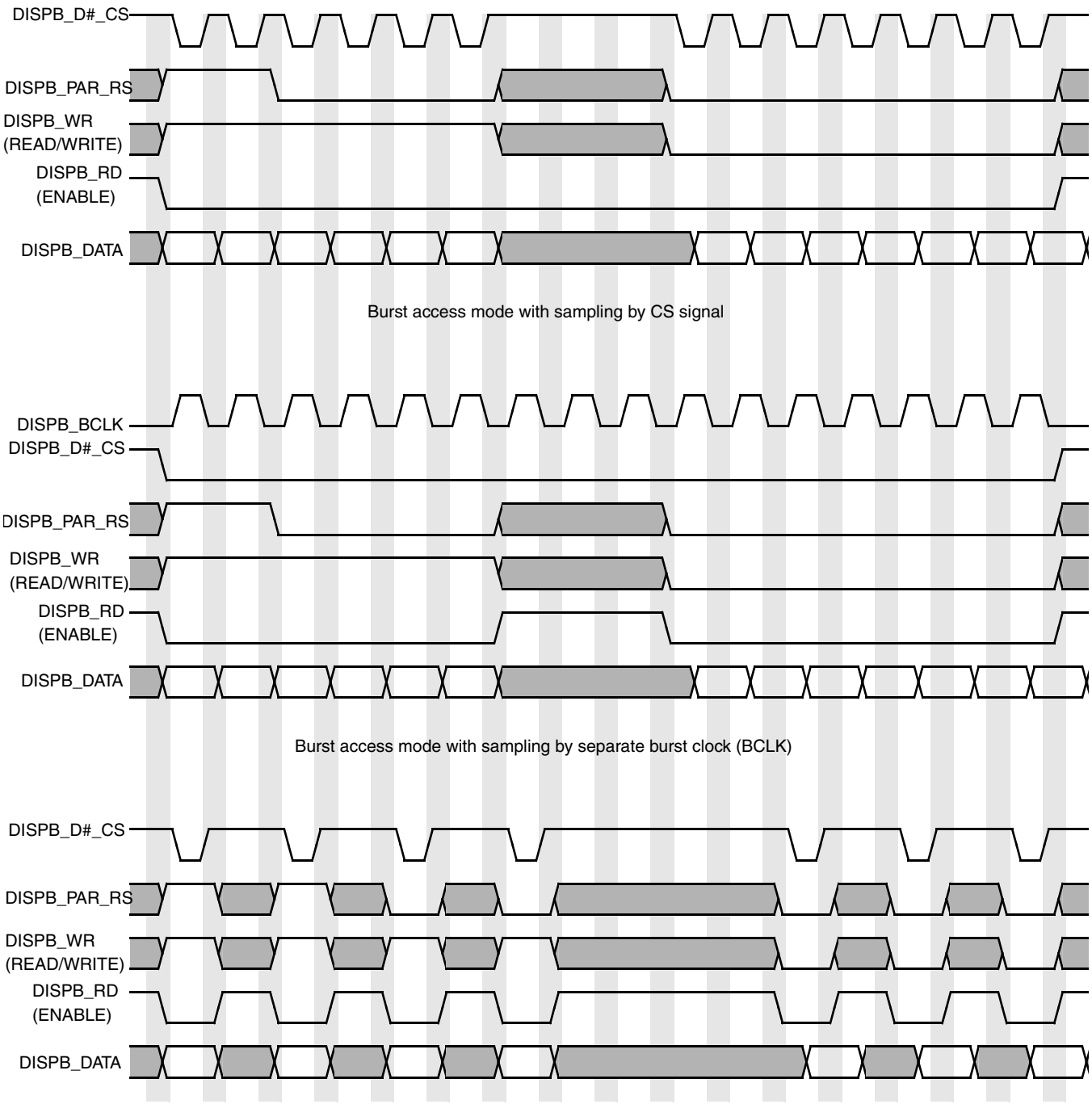

Figure 54. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

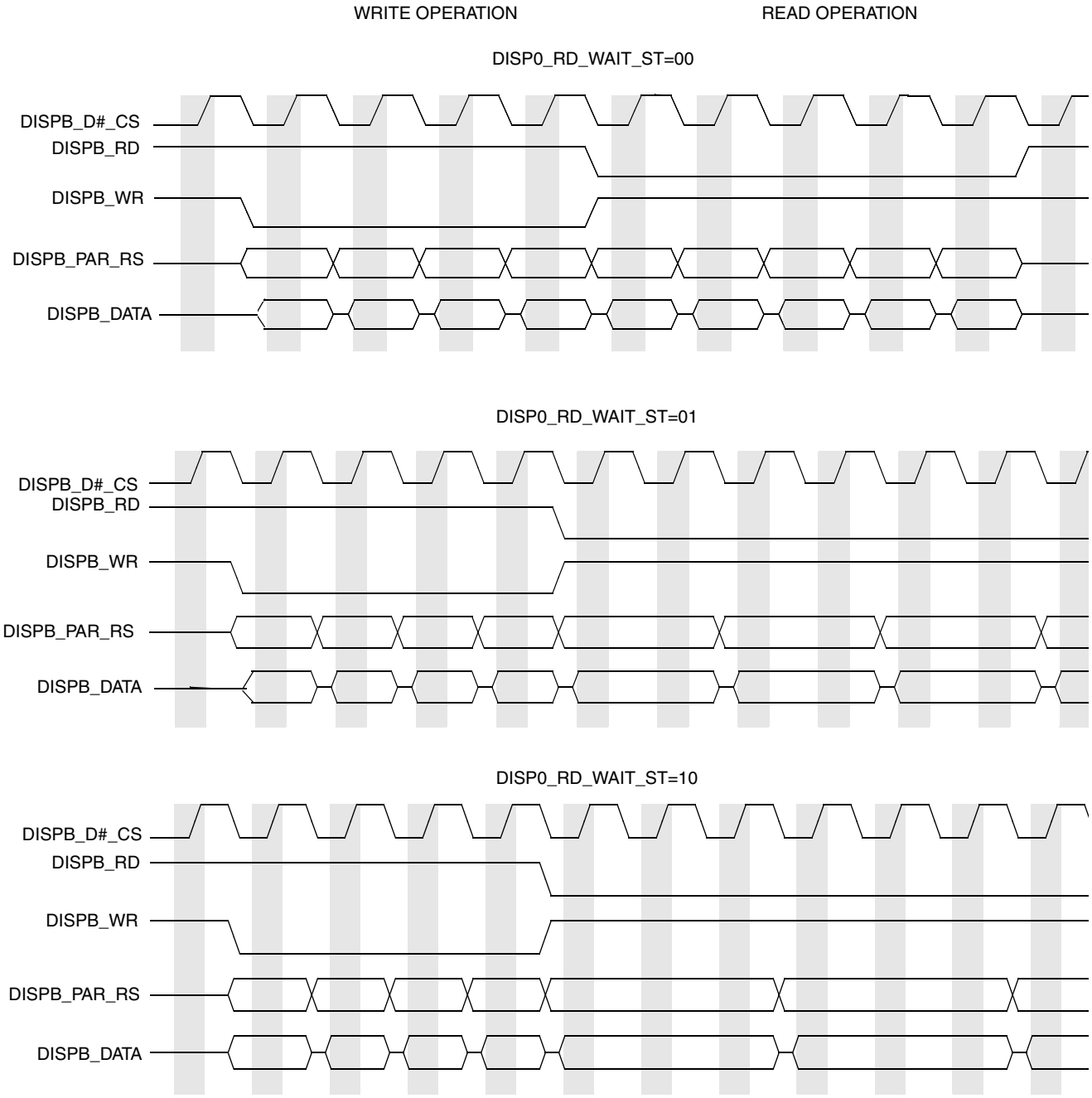

Figure 56. Parallel Interface Timing Diagram—Read Wait States

4.3.15.5.2 Parallel Interfaces, Electrical Characteristics

Figure 57, Figure 59, Figure 58, and Figure 60 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 50 lists the timing parameters at display access level. All timing images are based on active low control signals (signals polarity is controlled via the DI_DISP_SIG_POL Register).

4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 76 and Table 58 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

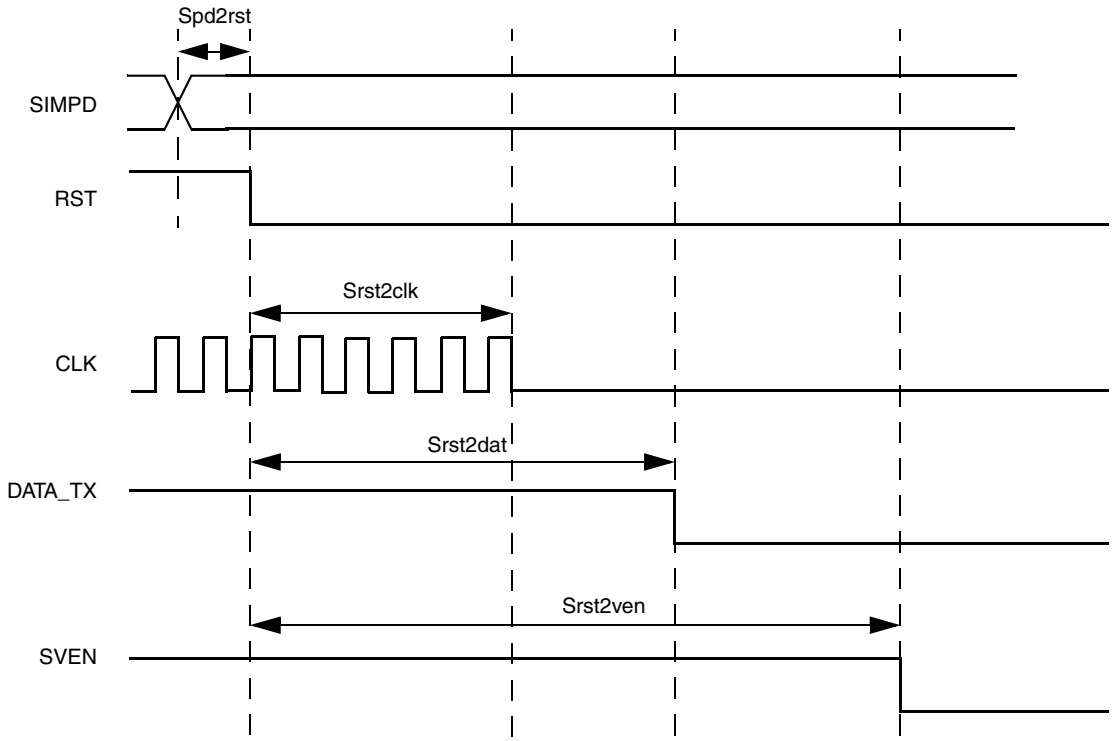

Figure 76. SmartCard Interface Power Down AC Timing

Table 58. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9*1/FCKIL	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8*1/FCKIL	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7*1/FCKIL	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9*1/FCKIL	25	ns

4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 77 depicts the SJC test clock input timing. Figure 78 depicts the SJC boundary scan timing, Figure 79 depicts the SJC test access port, Figure 80 depicts the SJC TRST timing, and Table 59 lists the SJC timing parameters.

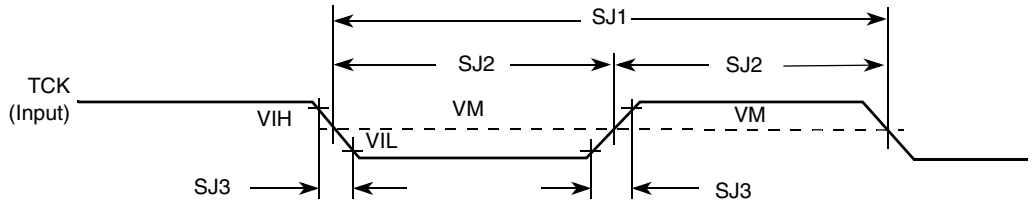

Figure 77. Test Clock Input Timing Diagram

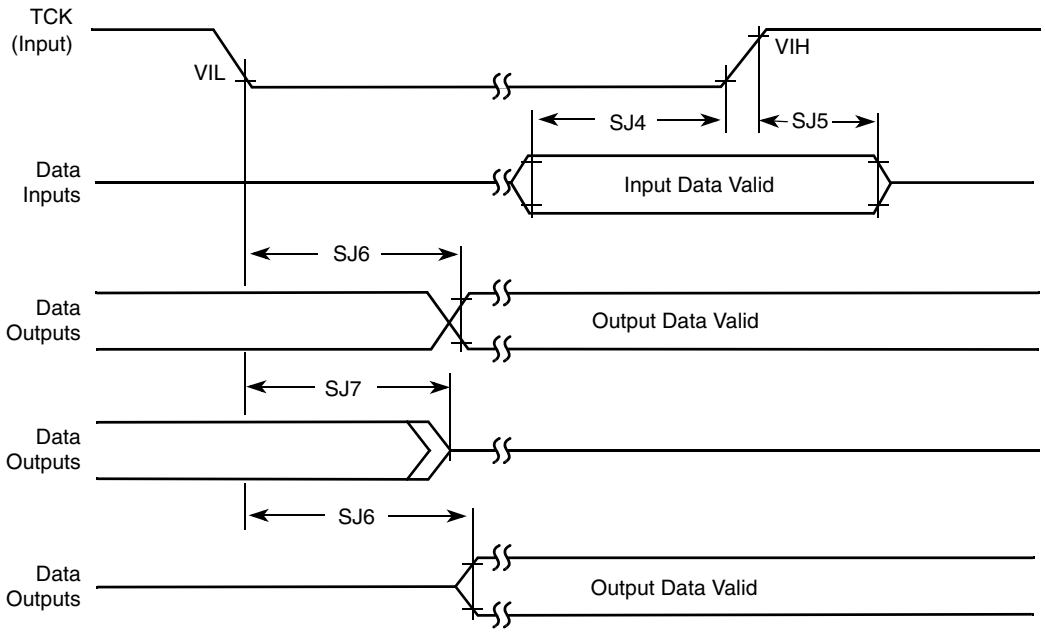

Figure 78. Boundary Scan (JTAG) Timing Diagram

Table 61. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

4.3.22.4 SSI Receiver Timing with External Clock

Figure 84 depicts the SSI receiver timing with external clock, and Table 63 lists the timing parameters.

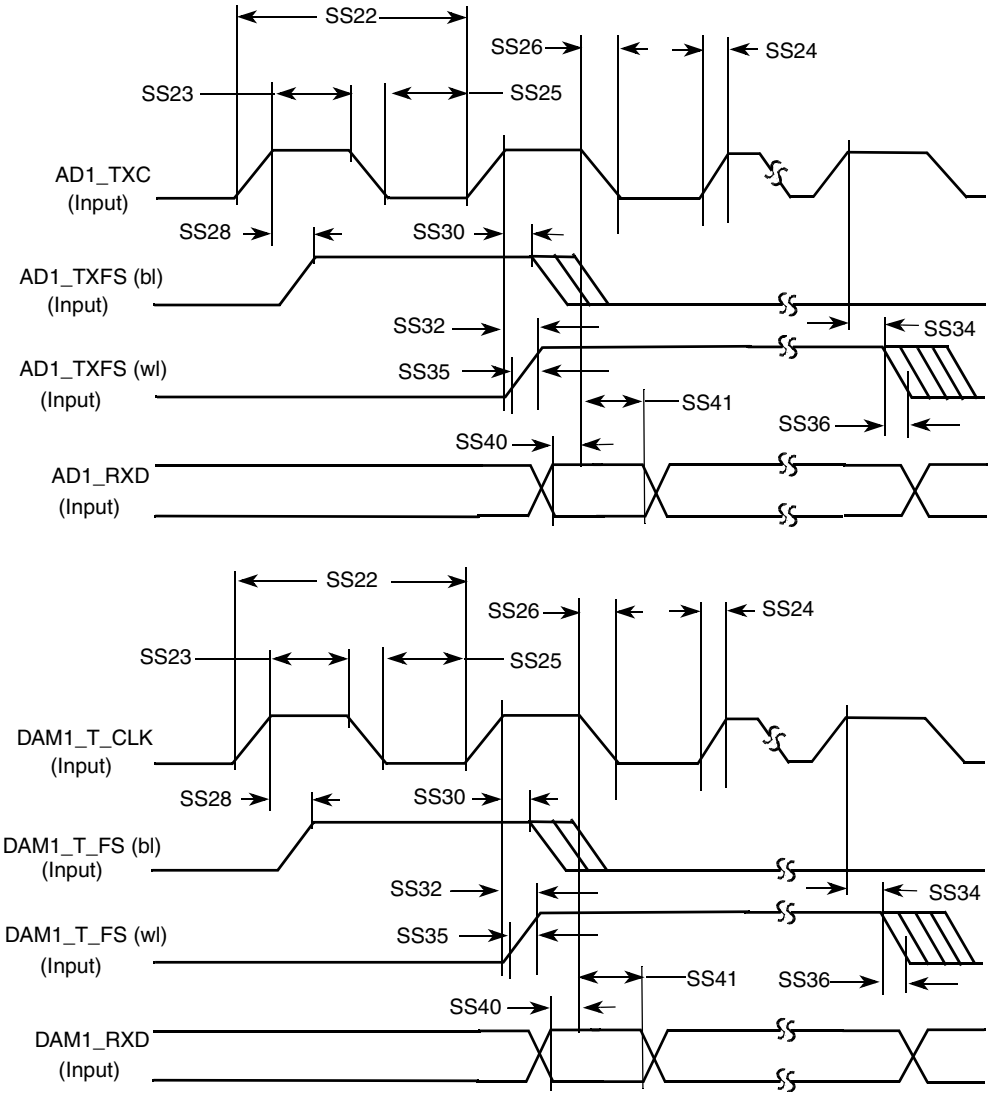

Figure 84. SSI Receiver with External Clock Timing Diagram

Table 63. SSI Receiver with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns

Table 63. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 85 depicts the USB ULPI timing diagram, and Table 64 lists the timing parameters.

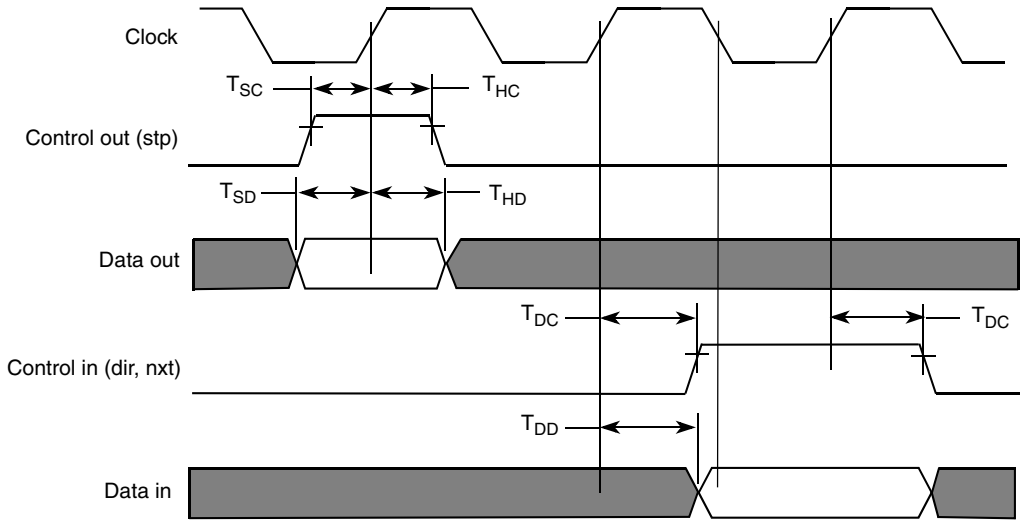

Figure 85. USB ULPI Interface Timing Diagram

Table 64. USB ULPI Interface Timing Specification[1]

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	T_{SC}, T_{SD}	6	—	ns
Hold time (control in, 8-bit data in)	T_{HC}, T_{HD}	0	—	ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	—	9	ns

1 Timing parameters are given as viewed by transceiver side.

5.1.2 MAPBGA Signal Assignment–14 × 14 mm 0.5 mm

See Section 8, "Revision History," Figure 70 for the 0.5 mm 14 × 14 MAPBGA signal assignments.

5.1.3 Connection Tables–14 x 14 mm 0.5 mm

Table 65 shows the device connection list for power and ground, alpha-sorted. Table 66 shows the device connection list for signals.

5.1.3.1 Ground and Power ID Locations–14 x 14 mm 0.5 mm

Table 65. 14 x 14 MAPBGA Ground/Power ID by Ball Grid Location

GND/PWR ID	Ball Location
FGND	AB24
FUSE_VDD	AC24
FVCC	AA24
GND	A1, A2, A25, A26, B1, B2, B25, B26, C1, C2, C24, C25, C26, D1, D25, E22, E24, F21, L12, M11, M12, M13, M14, M15, M16, N12, N13, N14, N15, N16, P12, P13, P14, P15, P16, R12, R13, R14, R15, R16, T12, T13, V17, AC2, AC26, AD1, AD2, AD24, AD25, AD26, AE1, AE2, AE24, AE25, AE26, AF1, AF2, AF25, AF26
IOQVDD	Y6
MGND	T15
MVCC	V15
NVCC1	G19, G21, K18
NVCC2	Y17, Y18, Y19, Y20
NVCC3	L9, M9, N11
NVCC4	L18, L19
NVCC5	E5, F6, G7
NVCC6	J15, J16, K15
NVCC7	N18, P18, R18, T18
NVCC8	J12, J13
NVCC9	J17
NVCC10	P9, P11, R11, T11
NVCC21	Y14, Y15, Y16
NVCC22	W7, Y7, Y8, Y9, Y10, Y11, Y12, Y13, AA6
QVCC	J14, L13, L14, L15, L16, M18, U18, V10, V11, V12, V13
QVCC1	J10, J11, K9, L11
QVCC4	N9, R9, T9, U9
SGND	T14
SVCC	V14
UVCC	V16
UGND	T16

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
SDCLK	AA21
$\overline{\text{SDCLK}}$	AE20
SDQS0	AD16
SDQS1	AE12
SDQS2	AD11
SDQS3	AD8
SDWE	AF20
SER_RS	T25
SFS3	R6
SFS4	F3
SFS5	A3
SFS6	T3
SIMPD0	G17
SJC_MOD	A20
SRST0	C19
SRX0	B21
SRXD3	R3
SRXD4	C3
SRXD5	B4
SRXD6	R7
STX0	F17
STXD3	R1
STXD4	B3
STXD5	C5
STXD6	T1
SVEN0	A21
TCK	B19
TDI	F16
TDO	A19
TMS	G16

Signal ID	Ball Location
TXD1	F10
TXD2	C13
USB_BYP	A9
USB_OC	C10
USB_PWR	B10
USBH2_CLK	N1
USBH2_DATA0	M1
USBH2_DATA1	M3
USBH2_DIR	N7
USBH2_NXT	N6
USBH2_STP	M2
USBOTG_CLK	G10
USBOTG_DATA0	F9
USBOTG_DATA1	B8
USBOTG_DATA2	G9
USBOTG_DATA3	A7
USBOTG_DATA4	C8
USBOTG_DATA5	B7
USBOTG_DATA6	F8
USBOTG_DATA7	A6
USBOTG_DIR	B9
USBOTG_NXT	A8
USBOTG_STP	C9
VPG0	G25
VPG1	J20
VSTBY	F26
VSYNC0	N24
VSYNC3	R26
WATCHDOG_RST	A24
WRITE	R25

5.2.2 MAPBGA Signal Assignment–19 × 19 mm 0.8 mm

See Table 71 for the 19 × 19 mm, 0.8 mm pitch signal assignments/ball map.

5.2.3 Connection Tables–19 x 19 mm 0.8 mm

Table 67 shows the device connection list for power and ground, alpha-sorted followed by Table 68, which shows the no-connects. Table 69 shows the device connection list for signals.

5.2.3.1 Ground and Power ID Locations—19 x 19 mm 0.8 mm

Table 67. 19 x 19 BGA Ground/Power ID by Ball Grid Location

GND/PWR ID	Ball Location
FGND	U16
FUSE_VDD	T15
FVCC	T16
GND	A1, A2, A3, A21, A22, A23, B1, B2, B22, B23, C1, C2, C22, C23, D22, D23, J12, J13, K10, K11, K12, K13, K14, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14, R12, Y1, Y23, AA1, AA2, AA22, AA23, AB1, AB2, AB21, AB22, AB23, AC1, AC2, AC21, AC22, AC23
IOQVDD	T8
MGND	U14
MVCC	U15
NVCC1	G15, G16, H16, J17
NVCC2	N16, P16, R15, R16, T14
NVCC3	K7, K8, L7, L8
NVCC4	H14, J15, K15
NVCC5	G9, G10, H8, H9
NVCC6	G11, G12, G13, H12
NVCC7	H15, J16, K16, L16, M16
NVCC8	H10, H11, J11
NVCC9	G14
NVCC10	P8, R7, R8, R9, T9
NVCC21	T11, T12, T13, U11
NVCC22	T10, U7, U8, U9, U10, V6, V7, V8, V9, V10
QVCC	H13, J14, L15, M15, N9, N15, P9, P15, R10, R11, R13, R14
QVCC1	J8, J9, J10, K9
QVCC4	L9, M7, M8, N8
SGND	U13
SVCC	U12
UVCC	P18
UGND	P17

Table 68. 19 x 19 BGA No Connects[1]

Signal	Ball Location
NC	N7
NC	P7
NC	U21

1 These contacts are not used and must be floated by the user.

5.2.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location
A0	Y6
A1	AC5
A10	V15
A11	AB3
A12	AA3
A13	Y3
A14	Y15
A15	Y14
A16	V14
A17	Y13
A18	V13
A19	Y12
A2	AB5
A20	V12
A21	Y11
A22	V11
A23	Y10
A24	Y9
A25	Y8
A3	AA5
A4	Y5
A5	AC4
A6	AB4
A7	AA4
A8	Y4
A9	AC3
ATA_CS0	E1
ATA_CS1	G4
ATA_DIOR	E3
ATA_DIOW	H6
ATA_DMACK	E2
$\overline{\text{ATA\_RESET}}$	F3
BATT_LINE	F6
BCLK	W20
BOOT_MODE0	F17
BOOT_MODE1	C21

Signal ID	Ball Location
CKIL	E21
CLKO	C20
CLKSS	H17
COMPARE	A20
CONTRAST	N21
CS0	U17
CS1	Y22
CS2	Y18
CS3	Y19
CS4	Y20
CS5	AA21
CSI_D10	K21
CSI_D11	K22
CSI_D12	K23
CSI_D13	L20
CSI_D14	L18
CSI_D15	L21
CSI_D4	J20
CSI_D5	J21
CSI_D6	L17
CSI_D7	J22
CSI_D8	J23
CSI_D9	K20
CSI_HSYNC	H22
CSI_MCLK	H20
CSI_PIXCLK	H23
CSI_VSYNC	H21
CSPI1_MISO	N2
CSPI1_MOSI	N1
CSPI1_SCLK	M4
CSPI1_SPI_RDY	M1
CSPI1_SS0	M2
CSPI1_SS1	N6
CSPI1_SS2	M3
CSPI2_MISO	B4
CSPI2_MOSI	D5

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
EB1	W21
ECB	Y21
FPSHIFT	M23
GPIO1_0	C19
GPIO1_1	G17
GPIO1_2	B20
LD7	T20
LD8	R17
LD9	U23
M_GRANT	U18
M_REQUEST	T17
MA10	Y2
MCUPG	See VPG0
NFALE	T2
$\overline{\text{NFCE}}$	R4
NFCLE	T1
NFRB	R3
$\overline{\text{NFRE}}$	T4
$\overline{\text{NFWE}}$	T3
$\overline{\text{NFWP}}$	P6
OE	T18
PAR_RS	P22
PC_BVD1	G2
PC_BVD2	H4
$\overline{\text{PC\_CD1}}$	J3
$\overline{\text{PC\_CD2}}$	H1
PC_POE	J6
PC_PWRON	K6
PC_READY	H2
PC_RST	F1
$\overline{\text{PC\_RW}}$	G3
PC_VS1	H3
PC_VS2	G1
$\overline{\text{PC\_WAIT}}$	J4
$\overline{\text{POR}}$	F21
POWER_FAIL	F20
PWMO	F2
RAS	AA19
READ	N18
$\overline{\text{RESET\_IN}}$	F22
RI_DCE1	D10
RI_DTE1	B11
RTCK	D15
RTS1	B9
RTS2	B12
RW	V18

Signal ID	Ball Location
LD17	W23
LD2	R21
LD3	R20
LD4	T23
LD5	T22
LD6	T21
SCK6	R2
SCLK0	B19
SD_D_CLK	M21
SD_D_I	M20
SD_D_IO	M18
SD0	AC18
SD1	AA17
SD1_CLK	K2
SD1_CMD	K3
SD1_DATA0	K4
SD1_DATA1	J1
SD1_DATA2	J2
SD1_DATA3	L6
SD10	AB14
SD11	AC14
SD12	AA13
SD13	AB13
SD14	AC13
SD15	AA12
SD16	AC12
SD17	AA11
SD18	AB11
SD19	AC11
SD2	AB17
SD20	AA10
SD21	AB10
SD22	AC10
SD23	AC9
SD24	AA9
SD25	AC8
SD26	AB8
SD27	AC7
SD28	AA8
SD29	AB7
SD3	AC17
SD30	AA7
SD31	AC6
SD4	AA16
SD5	AC16
SD6	AA15