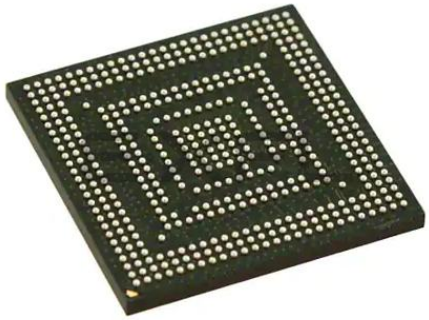

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31vkn5c

7 Supply voltage is considered “overdrive” for voltages above 3.1 V. Operation time in overdrive—whether switching or not—must be limited to a cumulative duration of 1 year (8,760 hours) or less to sustain the maximum operating voltage without significant device degradation—for example, 20% (average 4.8 hours out of 24 hours per day) duty cycle for 5-year rated equipment. Operation at 3.3 V that exceeds a cumulative 3,504 hours may cause non-operation whenever supply voltage is reduced to 1.8 V; degradation may render the device too slow or inoperable. Below 3.1 V, duty cycle restrictions may apply for equipment rated above 5 years.

8 For normal operating conditions, PLLs’ and core supplies must maintain the following relation: PLL ≥ Core – 100 mV. In other words, for a 1.6 V core supply, PLL supplies must be set to 1.5 V or higher. This restriction is no longer necessary on mask set M91E. PLL supplies may be set independently of core supply. PLL voltage must not be altered after power up, otherwise the PLL will be unstable and lose lock. To minimize inducing noise on the PLL supply line, source the voltage from a low-noise, dedicated supply. PLL parameters in Table 31, "DPLL Specifications," on page 37, are guaranteed over the entire specified voltage range.

9 Fusebox read supply voltage applies to silicon Revisions 1.2 and previous.

10 In read mode, FUSE_VDD can be floated or grounded for mask set M91E (silicon Revision 2.0).

11 Fuses might be inadvertently blown if written to while the voltage is below this minimum.

12 The temperature range given is for the consumer version. Please refer to Table 1 for extended temperature range offerings and the associated part numbers.

Table 9. Specific Operating Ranges for Silicon Revision 2.0

Symbol	Parameter	Min	Max	Units
FUSE_VDD	Fusebox read Supply Voltage[1]	—	—	V
	Fusebox write (program) Supply Voltage[2]	3.0	3.3	V

1 In read mode, FUSE_VDD should be floated or grounded.

2 Fuses might be inadvertently blown if written to while the voltage is below the minimum.

Table 10 provides information for interface frequency limits. For more details about clocks characteristics, see Section 4.3.8, “DPLL Electrical Specifications,” and Section 4.3.3, “Clock Amplifier Module (CAMP) Electrical Characteristics.”

Table 10. Interface Frequency

ID	Parameter	Symbol	Min	Typ	Max	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz
2	CKIL Frequency[1]	f_{CKIL}	32	32.768	38.4	kHz
3	CKIH Frequency[2]	f_{CKIH}	15	26	75	MHz

1 CKIL must be driven by an external clock source to ensure proper start-up and operation of the device. CKIL is needed to clock the internal reset synchronizer, the watchdog, and the real-time clock.

2 DPTC functionality, specifically the voltage/frequency relation table, is dependent on CKIH frequency. At the time of publication, standard tables used by Freescale OSs provided for a CKIH frequency of 26 MHz only. Any deviation from this frequency requires an update to the OS. For more details, refer to the particular OS user's guide documentation.

Table 11 shows the fusebox supply current parameters.

Table 11. Fusebox Supply Current Parameters

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	eFuse Program Current.[1] Current to program one eFuse bit: efuse_pgm = 3.0 V	$I_{program}$	—	35	60	mA
2	eFuse Read Current[2] Current to read an 8-bit eFuse word vdd_fusebox = 1.875 V	I_{read}	—	5	8	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word, and only applies to Silicon Rev. 1.2 and previous.

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31 (worst-case scenario)

4.2.1 Powering Up

The Power On Reset ($\overline{\text{POR}}$) pin must be kept asserted (low) throughout the power up sequence. Power up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{\text{POR}}$. Figure 2 shows the power-up sequence for silicon Revisions 1.2 and previous. Figure 3 and Figure 4 show the power-up sequence for silicon Revision 2.0.

NOTE

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

Table 30. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	30	—	ns
CS3	SCLK Rise or Fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	SSx pulse width	t_{CSLH}	25	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	25	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	25	—	ns
CS7	Data Out Setup Time	t_{Smosi}	5	—	ns
CS8	Data Out Hold Time	t_{Hmosi}	5	—	ns
CS9	Data In Setup Time	t_{Smiso}	6	—	ns
CS10	Data In Hold Time	t_{Hmiso}	5	—	ns
CS11	$\overline{\text{SPI\_RDY}}$ Setup Time[1]	t_{SRDY}	—	—	ns

[1] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.3.8 DPLL Electrical Specifications

The three PLL's of the MCIMX31 (MCU, USB, and Serial PLL) are all based on same DPLL design. The characteristics provided herein apply to all of them, except where noted explicitly. The PLL characteristics are provided based on measurements done for both sources—external clock source (CKIH), and FPM (Frequency Pre-Multiplier) source.

4.3.8.1 Electrical Specifications

Table 31 lists the DPLL specification.

Table 31. DPLL Specifications

Parameter	Min	Typ	Max	Unit	Comments
CKIH frequency	15	26[1]	75[2]	MHz	—
CKIL frequency (Frequency Pre-multiplier (FPM) enable mode)	—	32; 32.768, 38.4	—	kHz	FPM lock time ≈ 480 µs.
Predivision factor (PD bits)	1	—	16	—	—
PLL reference frequency range after Predivider	15	—	35	MHz	15 ≤ CKIH frequency/PD ≤ 35 MHz 15 ≤ FPM output/PD ≤ 35 MHz
PLL output frequency range: MPLL and SPLL UPLL	 52 190	—	 532 240	MHz	—
Maximum allowed reference clock phase noise.	—	—	± 100	ps	—
Frequency lock time (FOL mode or non-integer MF)	—	—	398	—	Cycles of divided reference clock.

Table 31. DPLL Specifications (continued)

Parameter	Min	Typ	Max	Unit	Comments
Phase lock time	—	—	100	µs	In addition to the frequency
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ < 50 kHz
Maximum allowed PLL supply voltage ripple	—	—	20	mV	50 kHz < $F_{modulation}$ < 300 kHz
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ > 300 kHz
PLL output clock phase jitter	—	—	5.2	ns	Measured on CLKO pin
PLL output clock period jitter	—	—	420	ps	Measured on CLKO pin

1 The user or board designer must take into account that the use of a frequency other than 26 MHz would require adjustment to the DPTC–DVFS table, which is incorporated into operating system code.

2 The PLL reference frequency must be ≤ 35 MHz. Therefore, for frequencies between 35 MHz and 70 MHz, program the predivider to divide by 2 or more. If the CKIH frequency is above 70 MHz, program the predivider to 3 or more. For PD bit description, see the reference manual.

4.3.9 EMI Electrical Specifications

This section provides electrical parametrics and timings for EMI module.

4.3.9.1 NAND Flash Controller Interface (NFC)

The NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 23, Figure 24, Figure 25, and Figure 26 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 32 lists the timing parameters.

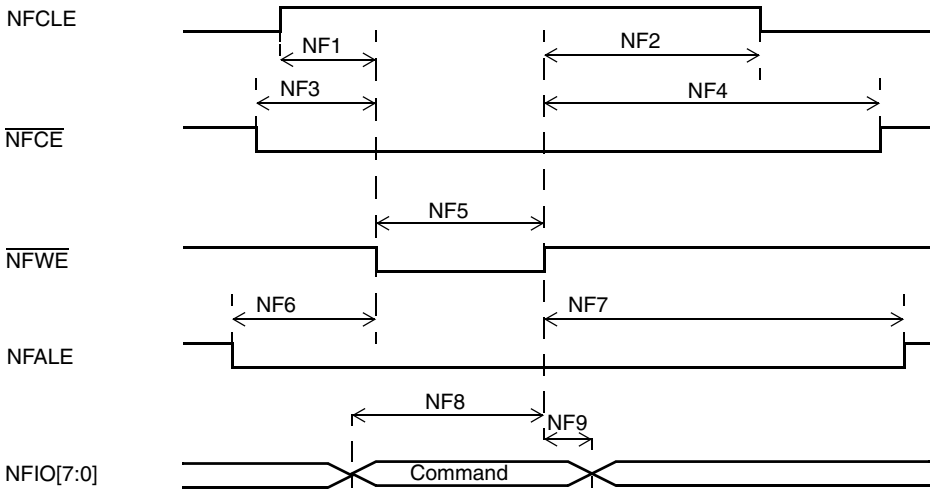


Figure 23. Command Latch Cycle Timing Diagram

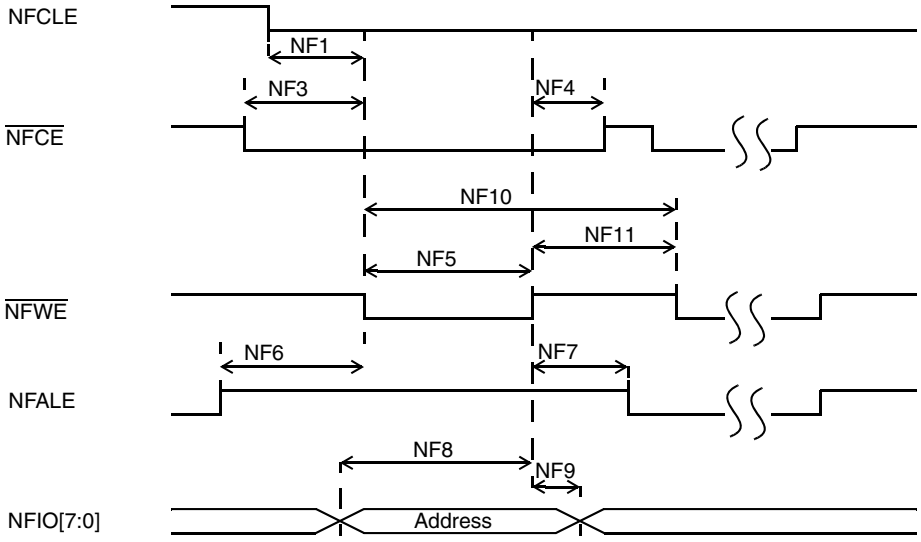


Figure 24. Address Latch Cycle Timing Diagram

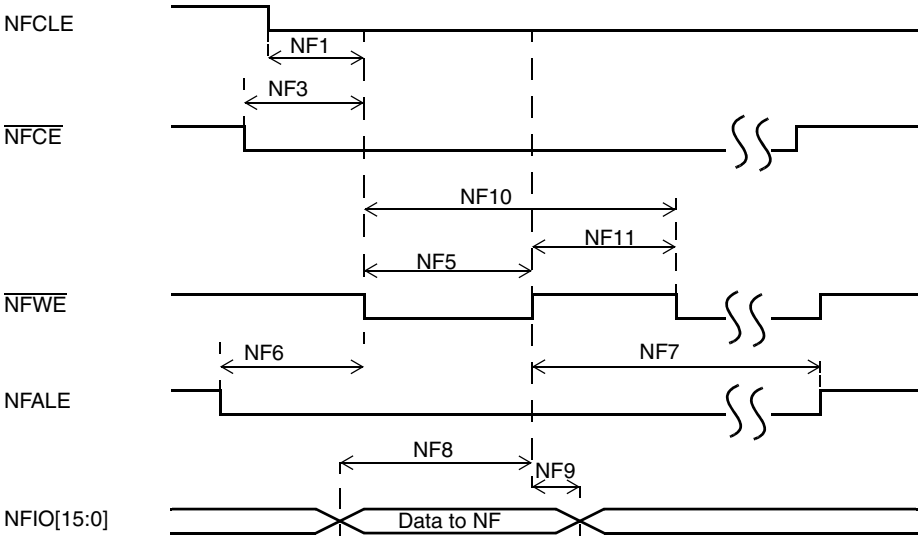


Figure 25. Write Data Latch Cycle Timing Diagram

NOTE

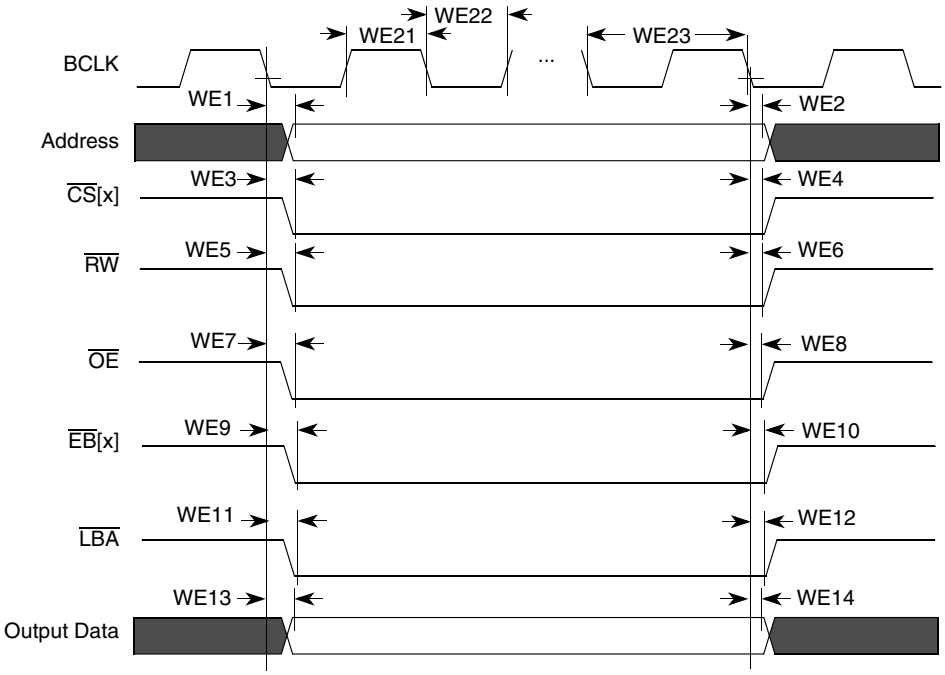
High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.3.9.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 27 depicts the timing of the WEIM module, and Table 33 lists the timing parameters.

WEIM Outputs Timing



WEIM Inputs Timing

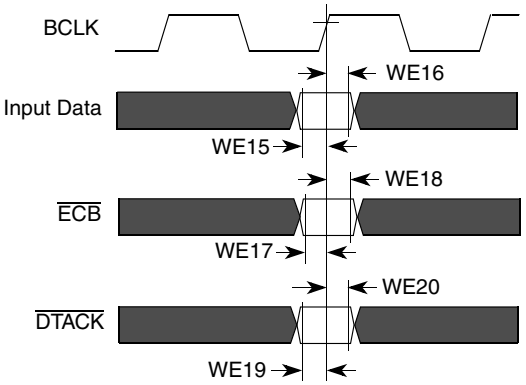


Figure 27. WEIM Bus Timing Diagram

Table 33. WEIM Bus Timing Parameters

ID	Parameter	Min	Max	Unit
WE1	Clock fall to Address Valid	–0.5	2.5	ns
WE2	Clock rise/fall to Address Invalid	–0.5	5	ns
WE3	Clock rise/fall to $\overline{CS}$[x] Valid	–3	3	ns
WE4	Clock rise/fall to $\overline{CS}$[x] Invalid	–3	3	ns
WE5	Clock rise/fall to $\overline{RW}$ Valid	–3	3	ns
WE6	Clock rise/fall to $\overline{RW}$ Invalid	–3	3	ns
WE7	Clock rise/fall to $\overline{OE}$ Valid	–3	3	ns

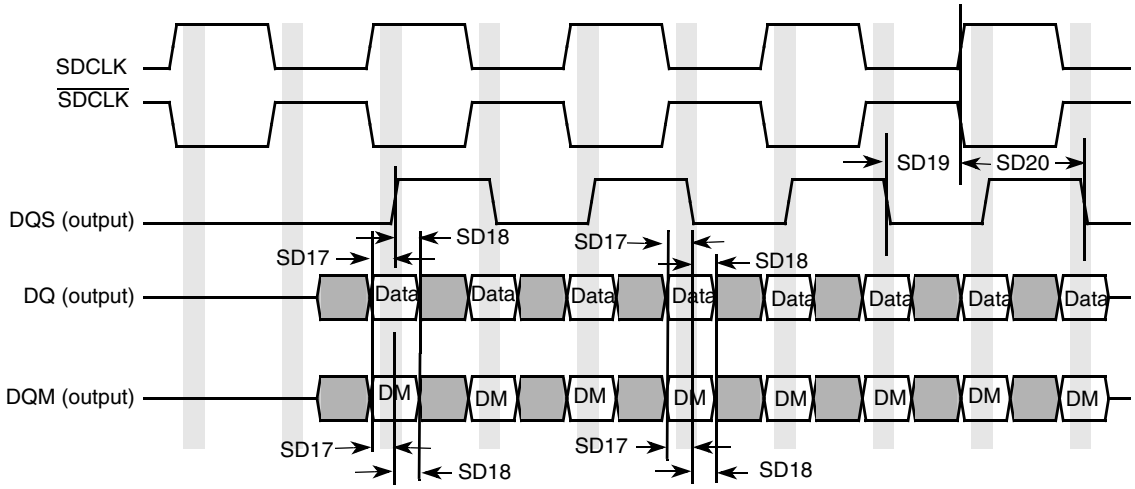


Figure 38. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 38. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min	Max	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 38 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.15.4.2 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics."

4.3.15.5 Asynchronous Interfaces

4.3.15.5.1 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock. The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) of by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals changes only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k) and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK. In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode. In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 52, Figure 53, Figure 54, and Figure 55. These timing images correspond to active-low DISPB_D#_CS, DISPB_D#_WR and DISPB_D#_RD signals.

Additionally, the IPU allows a programmable pause between two burst. The pause is defined in the HSP_CLK cycles. It allows to avoid timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

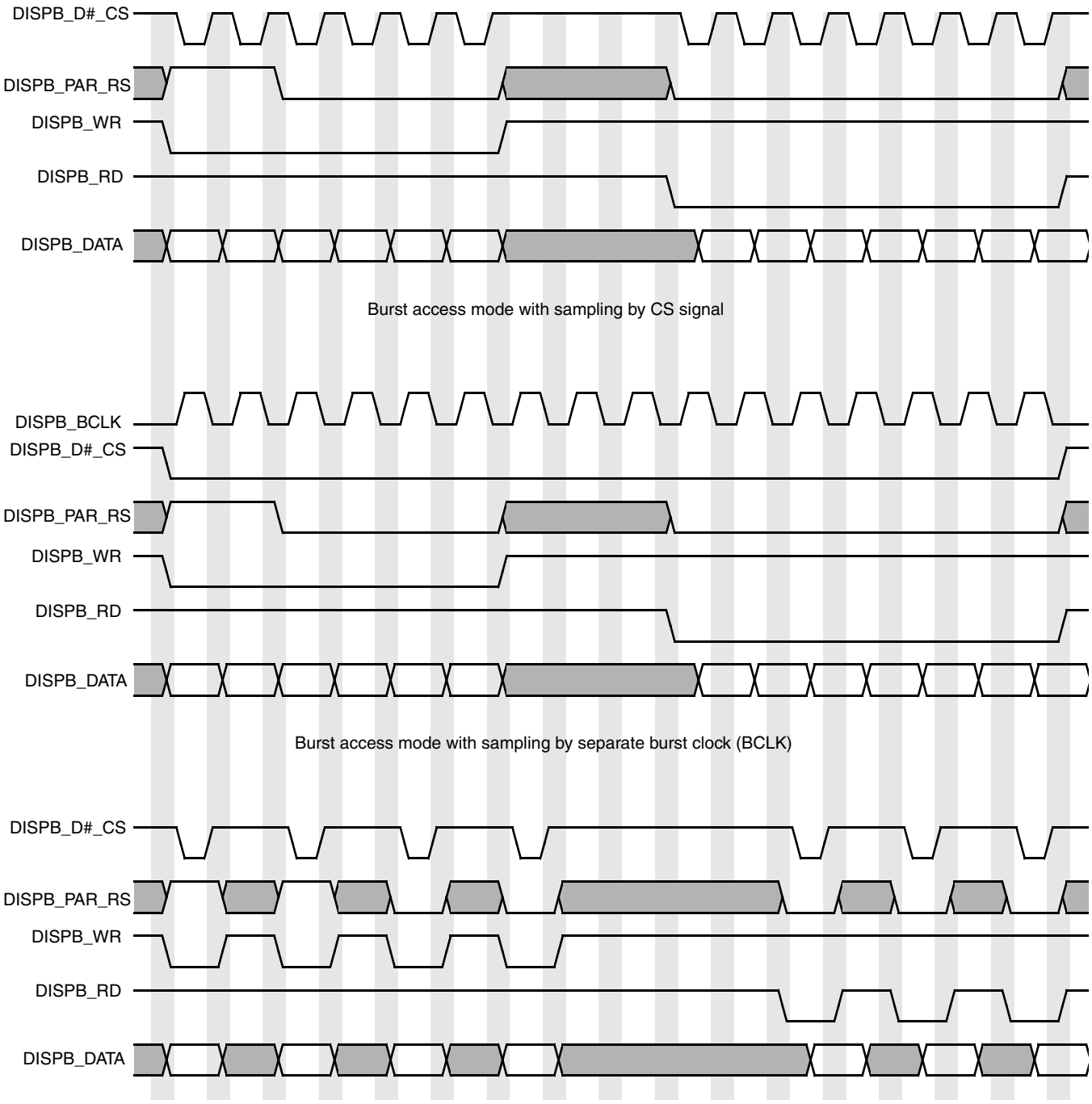


Figure 52. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram

4.3.15.5.4 Serial Interfaces, Electrical Characteristics

Figure 65 depicts timing of the serial interface. Table 51 lists the timing parameters at display access level.

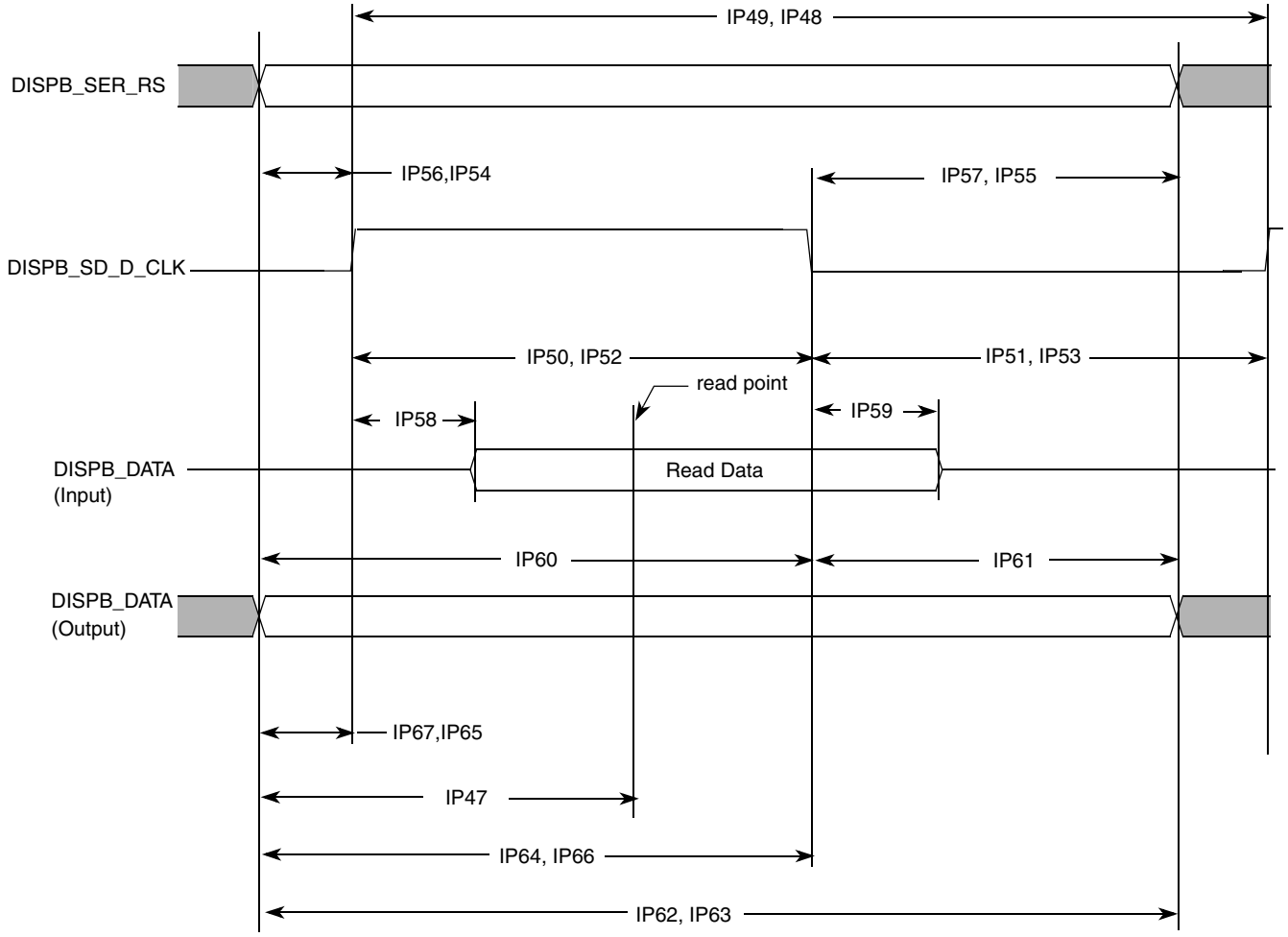


Figure 65. Asynchronous Serial Interface Timing Diagram

Table 51. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr–Tdicur–1.5	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.5	Tdicpr–Tdicdr+ Tdicur	Tdicpr–Tdicdr+Tdicur+1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

4.3.16 Memory Stick Host Controller (MSHC)

Figure 66, Figure 67, and Figure 68 depict the MSHC timings, and Table 52 and Table 53 list the timing parameters.

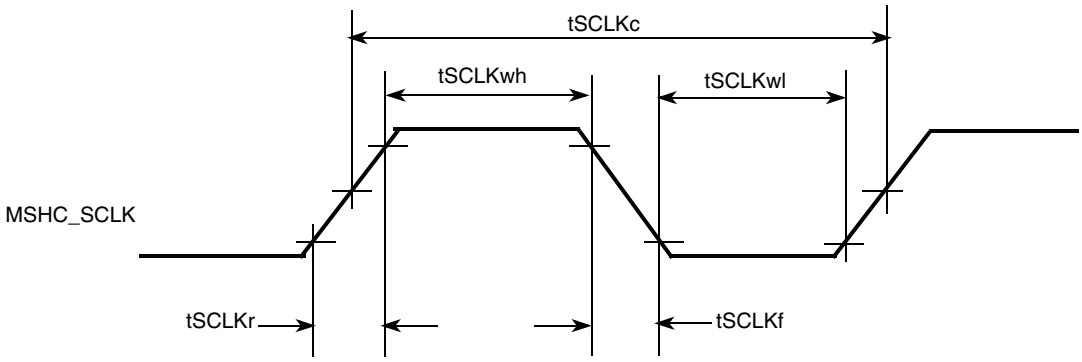


Figure 66. MSHC_CLK Timing Diagram

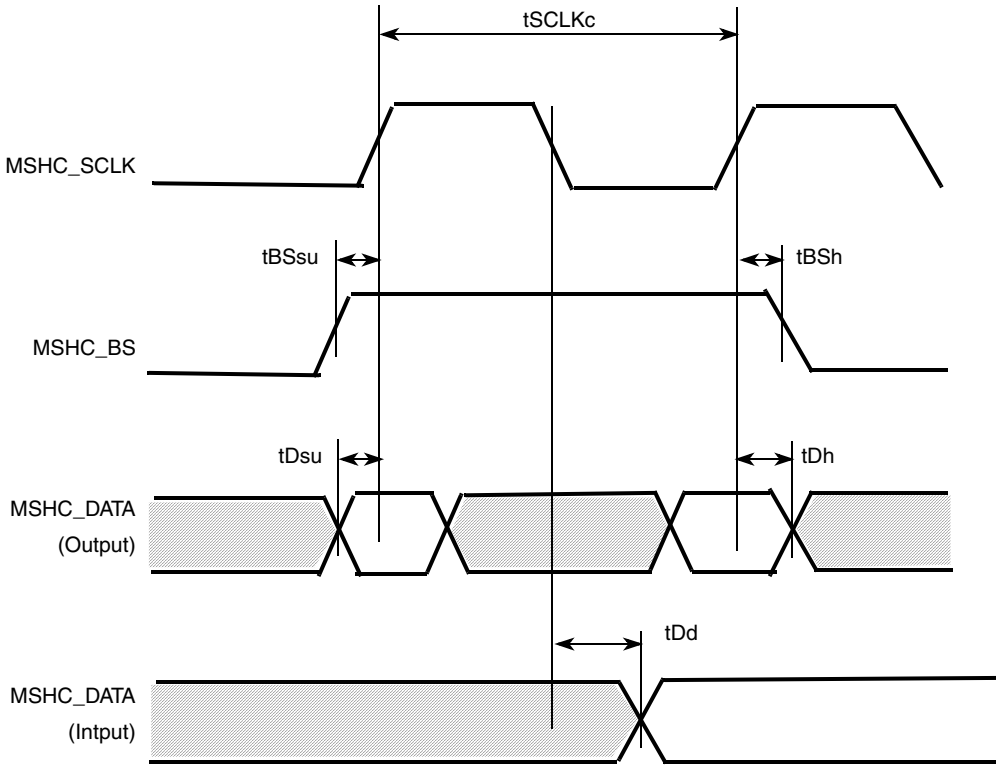


Figure 67. Transfer Operation Timing Diagram (Serial)

4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 76 and Table 58 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

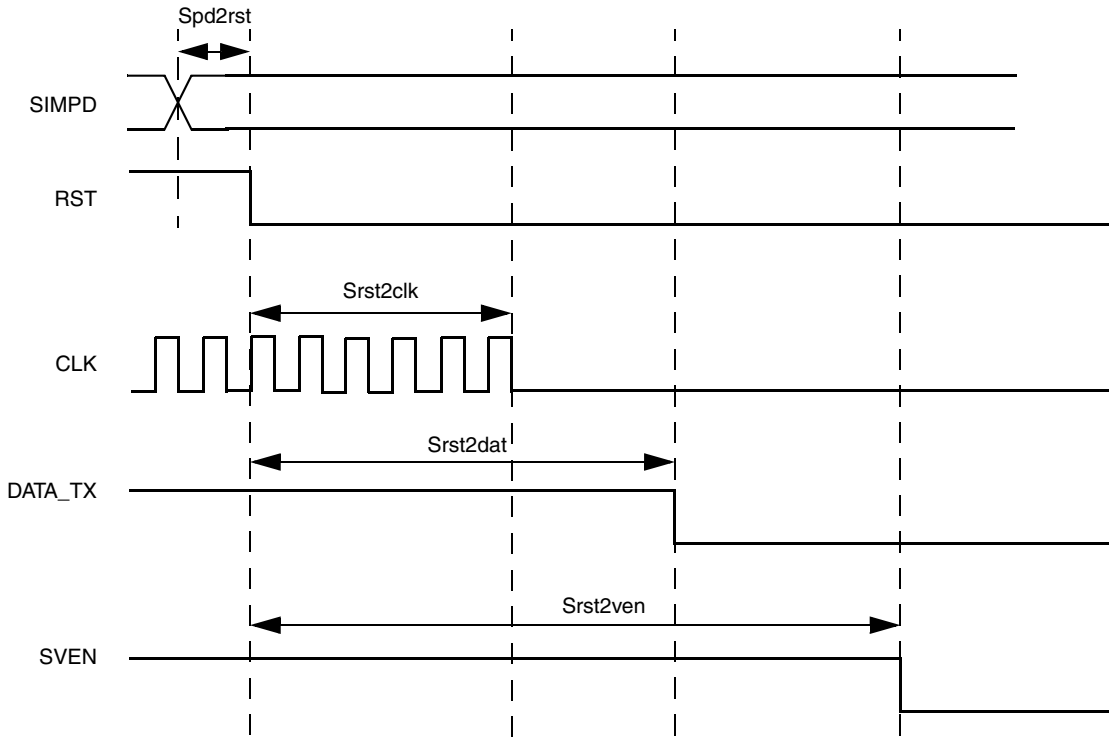
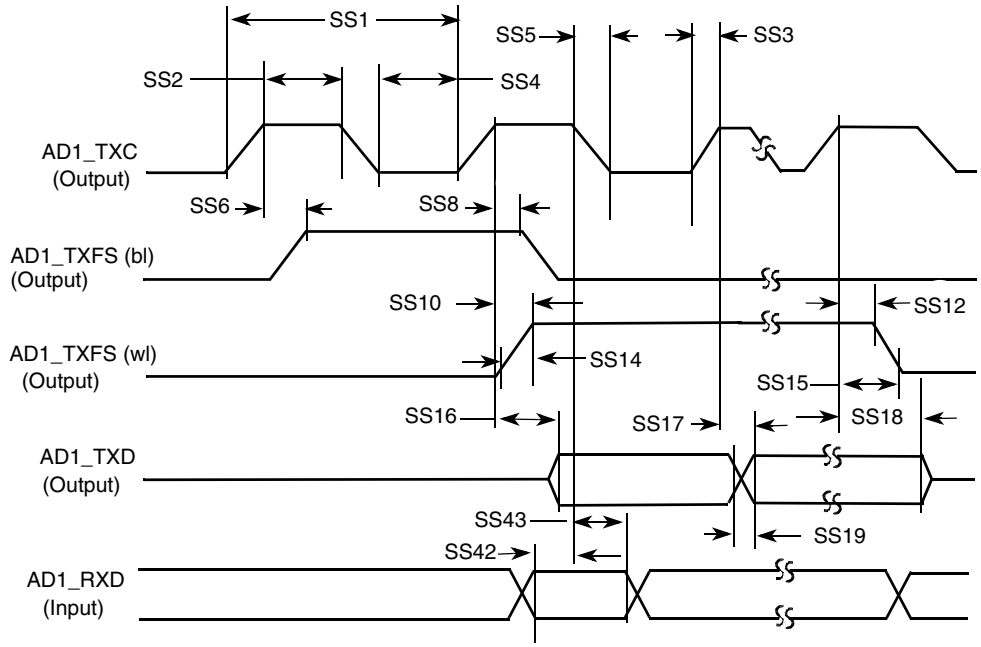


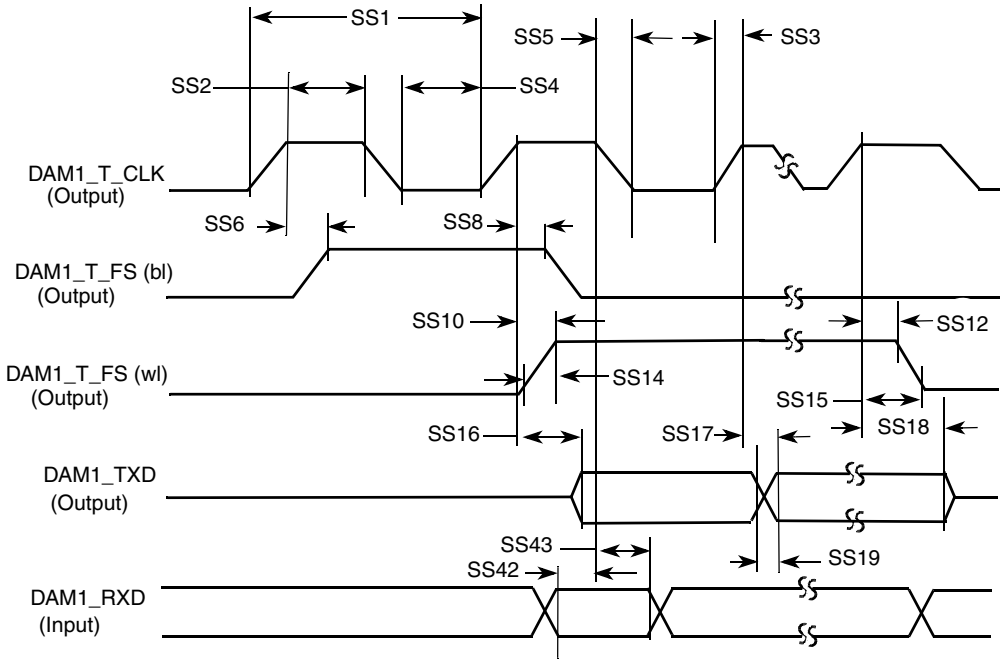
Figure 76. SmartCard Interface Power Down AC Timing

Table 58. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9*1/FCKIL	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8*1/FCKIL	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7*1/FCKIL	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9*1/FCKIL	25	ns



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 81. SSI Transmitter with Internal Clock Timing Diagram

5.1.2 MAPBGA Signal Assignment–14 × 14 mm 0.5 mm

See Section 8, "Revision History," Figure 70 for the 0.5 mm 14 × 14 MAPBGA signal assignments.

5.1.3 Connection Tables–14 x 14 mm 0.5 mm

Table 65 shows the device connection list for power and ground, alpha-sorted. Table 66 shows the device connection list for signals.

5.1.3.1 Ground and Power ID Locations–14 x 14 mm 0.5 mm

Table 65. 14 x 14 MAPBGA Ground/Power ID by Ball Grid Location

GND/PWR ID	Ball Location
FGND	AB24
FUSE_VDD	AC24
FVCC	AA24
GND	A1, A2, A25, A26, B1, B2, B25, B26, C1, C2, C24, C25, C26, D1, D25, E22, E24, F21, L12, M11, M12, M13, M14, M15, M16, N12, N13, N14, N15, N16, P12, P13, P14, P15, P16, R12, R13, R14, R15, R16, T12, T13, V17, AC2, AC26, AD1, AD2, AD24, AD25, AD26, AE1, AE2, AE24, AE25, AE26, AF1, AF2, AF25, AF26
IOQVDD	Y6
MGND	T15
MVCC	V15
NVCC1	G19, G21, K18
NVCC2	Y17, Y18, Y19, Y20
NVCC3	L9, M9, N11
NVCC4	L18, L19
NVCC5	E5, F6, G7
NVCC6	J15, J16, K15
NVCC7	N18, P18, R18, T18
NVCC8	J12, J13
NVCC9	J17
NVCC10	P9, P11, R11, T11
NVCC21	Y14, Y15, Y16
NVCC22	W7, Y7, Y8, Y9, Y10, Y11, Y12, Y13, AA6
QVCC	J14, L13, L14, L15, L16, M18, U18, V10, V11, V12, V13
QVCC1	J10, J11, K9, L11
QVCC4	N9, R9, T9, U9
SGND	T14
SVCC	V14
UVCC	V16
UGND	T16

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
CSPI3_SCLK	E1
CSPI3_SPI_RDY	G6
CTS1	B11
CTS2	G13
D0	AB2
D1	Y3
D10	Y1
D11	U7
D12	W2
D13	V3
D14	W1
D15	U6
D2	AB1
D3	W6
D3_CLS	R20
D3_REV	T26
D3_SPL	U25
D4	AA2
D5	V7
D6	AA1
D7	W3
D8	Y2
D9	V6
DCD_DCE1	B12
DCD_DTE1	B13
$\overline{DE}$	C18
DQM0	AE19
DQM1	AD19
DQM2	AA20
DQM3	AE18
DRDY0	N26
DSR_DCE1	A11
DSR_DTE1	A12
DTR_DCE1	C11
DTR_DCE2	F12
DTR_DTE1	C12
DVFS0	E25
DVFS1	G24
EB0	W21
EB1	Y24
ECB	AD23
FPSHIFT	N21
GPIO1_0	F18
GPIO1_1	B23
GPIO1_2	C20
LD7	W25

Signal ID	Ball Location
GPIO1_3	F25
GPIO1_4	F19
GPIO1_5 (PWR RDY)	B24
GPIO1_6	A23
GPIO3_0	K21
GPIO3_1	H26
HSYNC	N25
I2C_CLK	J24
I2C_DAT	H25
IOIS16	J3
KEY_COL0	C15
KEY_COL1	B17
KEY_COL2	G15
KEY_COL3	A17
KEY_COL4	C16
KEY_COL5	B18
KEY_COL6	F15
KEY_COL7	A18
KEY_ROW0	F13
KEY_ROW1	B15
KEY_ROW2	C14
KEY_ROW3	A15
KEY_ROW4	G14
KEY_ROW5	B16
KEY_ROW6	F14
KEY_ROW7	A16
L2PG	See VPG1
LBA	AE22
LCS0	P26
LCS1	P21
LD0	T24
LD1	U26
LD10	V24
LD11	Y25
LD12	Y26
LD13	V21
LD14	AA25
LD15	W24
LD16	AA26
LD17	V20
LD2	T21
LD3	V25
LD4	T20
LD5	V26
LD6	U24
SCK6	T2

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
LD8	U21
LD9	W26
M_GRANT	Y21
M_REQUEST	AC25
MA10	AC1
MCUPG	See VPG0
NFALE	V1
$\overline{\text{NFCE}}$	T6
NFCLE	U3
NFRB	U1
$\overline{\text{NFRE}}$	V2
$\overline{\text{NFWE}}$	T7
$\overline{\text{NFWP}}$	U2
OE	AB25
PAR_RS	R21
PC_BVD1	H2
PC_BVD2	K6
$\overline{\text{PC\_CD1}}$	L7
$\overline{\text{PC\_CD2}}$	K1
PC_POE	J7
PC_PWRON	K3
PC_READY	J2
PC_RST	H1
$\overline{\text{PC\_RW}}$	G2
PC_VS1	J1
PC_VS2	K7
$\overline{\text{PC\_WAIT}}$	L6
$\overline{\text{POR}}$	H24
POWER_FAIL	E26
PWMO	G1
RAS	AF19
READ	P20
$\overline{\text{RESET\_IN}}$	J21
RI_DCE1	F11
RI_DTE1	G12
RTCK	C17
RTS1	G11
RTS2	B14
RW	AB22
RXD1	A10
RXD2	A13
SCK3	R2
SCK4	C4
SCK5	D3
SDCKE0	AD21
SDCKE1	AF21

Signal ID	Ball Location
SCLK0	B22
SD_D_CLK	P24
SD_D_I	N20
SD_D_IO	P25
SD0	AD18
SD1	AE17
SD1_CLK	M7
SD1_CMD	L2
SD1_DATA0	M6
SD1_DATA1	L1
SD1_DATA2	L3
SD1_DATA3	K2
SD10	AE15
SD11	AE14
SD12	AD14
SD13	AA14
SD14	AE13
SD15	AD13
SD16	AA13
SD17	AD12
SD18	AA12
SD19	AE11
SD2	AA19
SD20	AE10
SD21	AA11
SD22	AE9
SD23	AA10
SD24	AE8
SD25	AD10
SD26	AE7
SD27	AA9
SD28	AA8
SD29	AD9
SD3	AA18
SD30	AE6
SD31	AA7
SD4	AD17
SD5	AA17
SD6	AE16
SD7	AA16
SD8	AD15
SD9	AA15
SDBA0	AD7
SDBA1	AE5
TRSTB	B20
TTM_PAD	U20

5.2 MAPBGA Production Package—473 19 x 19 mm, 0.8 mm Pitch

This section contains the outline drawing, signal assignment map (see Section 8, "Revision History," Table 71 for the 19 x 19 mm, 0.8 mm pitch signal assignments), and MAPBGA ground/power ID by ball grid location for the 473 19 x 19 mm, 0.8 mm pitch package.

5.2.1 Production Package Outline Drawing–19 x 19 mm 0.8 mm

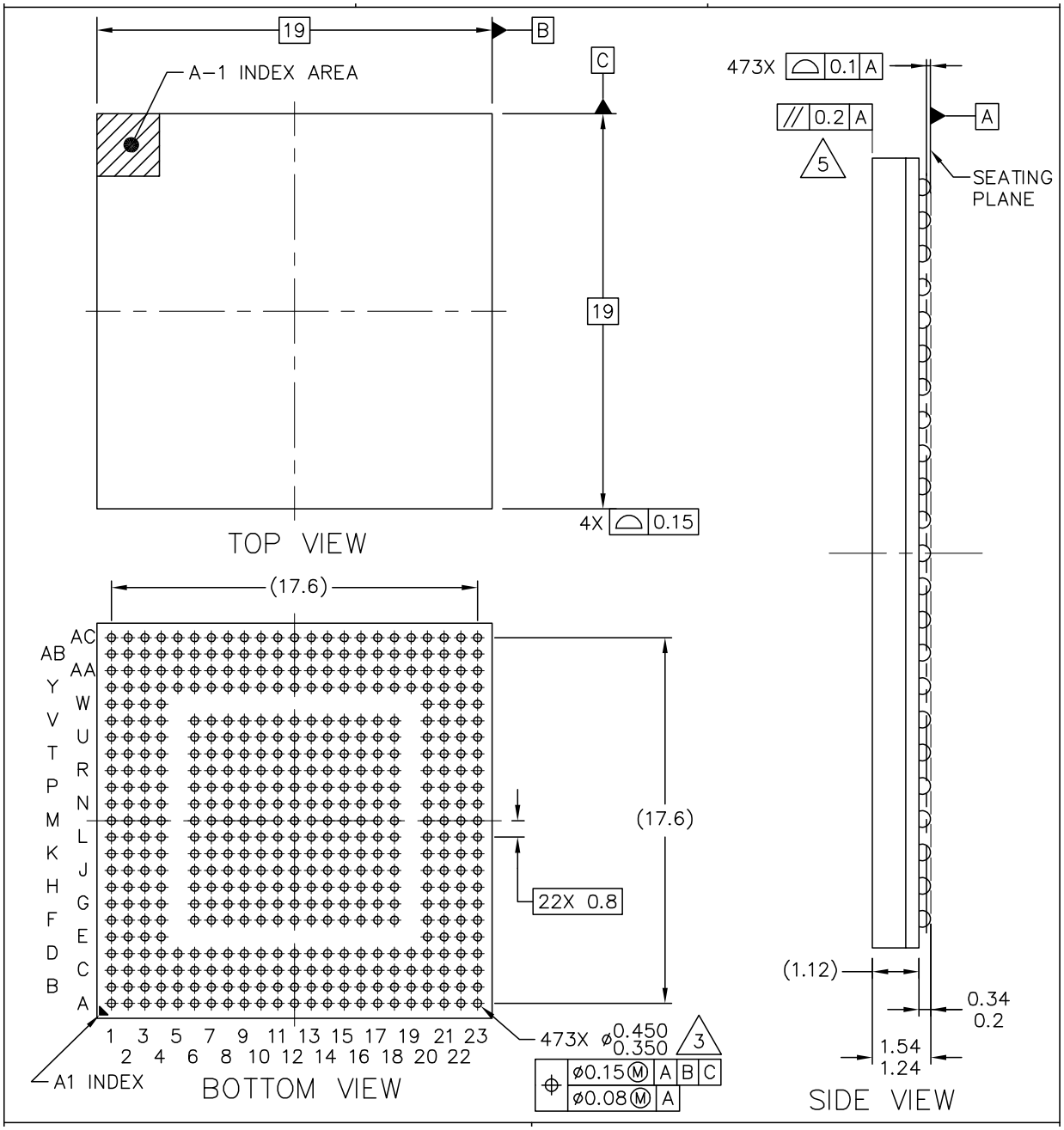


Figure 87. Production Package: Case 1931—0.8 mm Pitch

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
EB1	W21
ECB	Y21
FPSHIFT	M23
GPIO1_0	C19
GPIO1_1	G17
GPIO1_2	B20
LD7	T20
LD8	R17
LD9	U23
M_GRANT	U18
M_REQUEST	T17
MA10	Y2
MCUPG	See VPG0
NFALE	T2
$\overline{\text{NFCE}}$	R4
NFCLE	T1
NFRB	R3
$\overline{\text{NFRE}}$	T4
$\overline{\text{NFWE}}$	T3
$\overline{\text{NFWP}}$	P6
OE	T18
PAR_RS	P22
PC_BVD1	G2
PC_BVD2	H4
$\overline{\text{PC\_CD1}}$	J3
$\overline{\text{PC\_CD2}}$	H1
PC_POE	J6
PC_PWRON	K6
PC_READY	H2
PC_RST	F1
$\overline{\text{PC\_RW}}$	G3
PC_VS1	H3
PC_VS2	G1
$\overline{\text{PC\_WAIT}}$	J4
$\overline{\text{POR}}$	F21
POWER_FAIL	F20
PWMO	F2
RAS	AA19
READ	N18
$\overline{\text{RESET\_IN}}$	F22
RI_DCE1	D10
RI_DTE1	B11
RTCK	D15
RTS1	B9
RTS2	B12
RW	V18

Signal ID	Ball Location
LD17	W23
LD2	R21
LD3	R20
LD4	T23
LD5	T22
LD6	T21
SCK6	R2
SCLK0	B19
SD_D_CLK	M21
SD_D_I	M20
SD_D_IO	M18
SD0	AC18
SD1	AA17
SD1_CLK	K2
SD1_CMD	K3
SD1_DATA0	K4
SD1_DATA1	J1
SD1_DATA2	J2
SD1_DATA3	L6
SD10	AB14
SD11	AC14
SD12	AA13
SD13	AB13
SD14	AC13
SD15	AA12
SD16	AC12
SD17	AA11
SD18	AB11
SD19	AC11
SD2	AB17
SD20	AA10
SD21	AB10
SD22	AC10
SD23	AC9
SD24	AA9
SD25	AC8
SD26	AB8
SD27	AC7
SD28	AA8
SD29	AB7
SD3	AC17
SD30	AA7
SD31	AC6
SD4	AA16
SD5	AC16
SD6	AA15